DS100BR111 Ultra Low Power 10.3 Gbps 1-Lane Repeater with Input Equalization and Output De-Emphasis

1 Features

- Two Channel Repeaters for up to 10.3 Gbps
  - DS100BR210 : 2x Unidirectional Channels
  - DS100BR111 : 1x Bidirectional Lane
- 10G-KR Bi-directional Interface Compatibility
  - Allows for Back-channel Communication and Training
- Low 65 mW/channel (Typical) Power Consumption, with Option to Power Down Unused Channels
- Advanced Signal Conditioning Features
  - Receive Equalization up to +36 dB
  - Transmit De-emphasis up to -12 dB
  - Transmit VOD Control: 700 to 1300 mVp-p
  - Low Residual DJ at 10.3 Gbps
- Programmable Via Pin Selection, EEPROM, or SMBus Interface
- Single Supply Voltage: 2.5 V or 3.3 V
- Flow-thru Pinout in 4 mm × 4 mm 24-pin Leadless WQFN Package
- 5 kV HBM ESD Rating
- -40 to 85°C Operating Temperature Range

2 Applications

- High-speed Active Copper Cable Modules and FR-4 Backplane in Communication Systems
- 10GE, 10G-KR, FC, SAS, SATA 3/6 Gbps (with OOB Detection), InfiniBand, CPRI, RXAUI and many others

3 Description

The DS100BR111 is an extremely low power, high performance repeater designed to support serial links with data rates up to 10.3 Gbps. The DS100BR111 pinout is configured as one bidirectional lane (one transmit, one receive channel). The DS100BR111 inputs feature a powerful 4-stage continuous time linear equalizer (CTLE) to provide a boost of up to +36 dB at 5 GHz and open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect mediums such as board traces or twin-axial copper cables. The transmitter features a programmable output de-emphasis driver with up to -12 dB and can drive output voltage levels from 700 mVp-p to 1300 mVp-p.

When configured as a 10G-KR repeater, the DS100BR111 allows the KR host and the end point to optimize the full link by adjusting transmit and receive equalizer coefficients using back-channel communication techniques specified by the 802.3ap Ethernet standard.

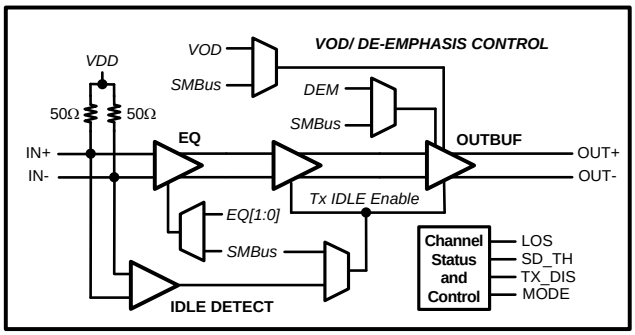
The programmable settings can be applied via pin control, SMBus protocol, or an external EEPROM. In the EEPROM mode, the configuration information is automatically loaded on power up, thereby eliminating the need for an external microprocessor or software driver.

Device Information(1)

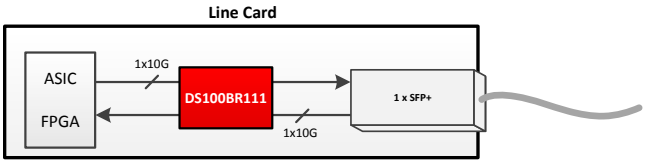
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS100BR111	WQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2013) to Revision F	Page
• Added, updated, or renamed the following sections: Device Information Table, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information*	1

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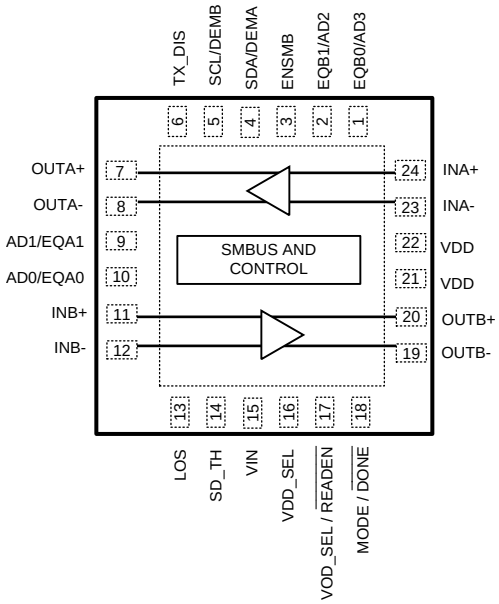
6 Pin Configuration and Functions

24-Pin
RTW Package
Top View



(1) The center DAP on the package bottom is the device GND connection. This pad must be connected to GND through multiple (minimum of 4) vias to ensure optimal electrical and thermal performance.

Pin Functions(1)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
DIFFERENTIAL HIGH SPEED I/O's			
INA+, INA- , INB+, INB-	24, 23 11, 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50 Ω termination resistors connect both INx+ and INx- to VDD. Compatible with AC coupled CML inputs.
OUTA+, OUTA-, OUTB+, OUTB-	7, 8 20, 19	O, CML	Inverting and non-inverting 50 Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs.
CONTROL PINS			
ENSMB	3	I, 4-LEVEL, LVCMOS	System Management Bus (SMBus) Enable Pin High = Register Access SMBus Slave Mode Float = Read External EEPROM (SMBus Master Mode) Tie 1 kΩ to GND = Pin Mode

(1) LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not ensured. Unless the "Float" level is desired, 4-Level input pins require a minimum 1 kΩ resistor to GND, VDD (in 2.5 V mode), or VIN (in 3.3 V mode). Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

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Pin Functions[1] (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
ENSMB = Float or 1 (SMBus MODES)			
SCL	5	I, 2-LEVEL, LVCMOS, O, Open Drain	Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete ($\overline{\text{ALL_DONE}}$ = 0). External 2 kΩ to 5 kΩ pull-up resistor to VDD (2.5 V mode) or VIN (3.3 V mode) recommended as per SMBus interface standards[2]
SDA	4	I, 2-LEVEL, LVCMOS, O, Open Drain	In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD (2.5 V mode) or VIN (3.3 V mode) recommended as per SMBus interface standards[2]
AD0-AD3	10, 9, 2, 1	I, 4-LEVEL, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. There are 16 addresses supported by these pins. Pins must be tied Low or High when used to define the device SMBus address. [3]
$\overline{\text{READEN}}$	17	I, 2-LEVEL, LVCMOS	ENSMB = Float: When using SMBus Master Mode, a logic low on this pin starts the load from the external EEPROM. ENSMB = 1: When using SMBus Slave Mode, the VOD_SEL/$\overline{\text{READEN}}$ pin must be tied Low for the AD[3:0] to be active. If this pin is tied High or left floating, an address of 0xB0 will be used for the DS100BR111.
$\overline{\text{DONE}}$	18	O, 2-LEVEL, LVCMOS	When using an External EEPROM (ENSMB = Float), Valid Register Load Status Output High = External EEPROM load failed or incomplete Low = External EEPROM load passed
ENSMB = 0 (PIN MODE)			
EQA0, EQA1 EQB0, EQB1	10, 9 1, 2	I, 4-LEVEL, LVCMOS	EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. EQA[1:0] controls the A channel, and EQB[1:0] controls the B channel. The pins are only active when ENSMB = 0. When ENSMB = 1, the SMBus registers provide independent control of each channel, and the EQB0/B1 pins are converted to SMBus AD2/AD3 inputs. See Table 3 for additional information.
DEMA, DEMB	4, 5	I, 4-LEVEL, LVCMOS	DEMA and DEMB control the level of de-emphasis for the output driver when in 10G mode. DEMA controls the A channel, and DEMB controls the B channel. The pins are only active when ENSMB = 0. When ENSMB = 1, the SMBus registers provide independent control of each channel, and the DEM pins are converted to SMBus SCL and SDA pins. See Table 4 for additional information.
VOD_SEL	17	I, 4-LEVEL, LVCMOS	VOD Select High = 10G-KR Mode (VOD = 1.1 Vpp or 1.3 Vpp) Float = (VOD = 1.0 Vpp) 20 kΩ to GND = (VOD = 1.2 Vpp) 1 kΩ to GND = (VOD = 700 mVpp) See [3][4] for additional notes. See Table 2 for additional information.
MODE	18	I, 4-LEVEL, LVCMOS	Controls Device Mode of Operation High= 10GbE Mode, Continuous Talk (Output Always On) Float = 10G-KR Mode, Slow OOB 20 kΩ to GND = eSATA Mode, Fast OOB, Auto Low Power on 100 µs of inactivity. SD stays active. 1 kΩ to GND = SAS Mode, Fast OOB

(2) SCL and SDA pins can be tied either to 3.3 V or 2.5 V, regardless of whether the device is operating in 2.5 V mode or 3.3 V mode.
(3) Setting VOD_SEL = High in SMBus Mode will force the SMBus Address = 0xB0
(4) DS100BR111 OUTA is limited to 700 mVpp in pin mode.

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Pin Functions[1] (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)			
TX_DIS	6	I, 2-LEVEL, LVCMOS	High = OUTA Enabled, OUTB Disabled Low = OUTA and OUTB Enabled
LOS	13	O, Open Drain	Indicates Loss of Signal (Default is LOS on INA). Can be modified via SMBus registers.
SD_TH	14	I, 4-LEVEL, LVCMOS	The SD_TH pin controls LOS threshold setting Assert (mVpp), Deassert (mVpp) High = 190 mVpp, 130 mVpp Float = 180 mVpp, 110 mVpp (Default) 20 kΩ to GND = 160 mVpp, 100 mVpp 1 kΩ to GND = 210 mVpp, 150 mVpp[5]
VDD_SEL	16	I, FLOAT	Enables the 3.3 V to 2.5 V internal regulator Low = 3.3 V Operation Float = 2.5 V Operation
POWER			
VDD	21, 22	Power	Power supply pins When in 2.5 V mode, connect to 2.5 V supply. When in 3.3 V mode, do not connect to any supply voltage. Should be used to attach external decoupling to device, 100 nF recommended. See *Power Supply Recommendations* for additional information.
VIN	15	Power	VIN = 3.3 V ± 10% (input to internal LDO regulator) When in 2.5 V mode, VIN pin must be left floating. See *Power Supply Recommendations* for additional information.
GND	DAP	Power	Ground pad (DAP - die attach pad).

(5) Using values less than the default level can extend the time required to detect LOS and are not recommended.

7 Specifications

7.1 Absolute Maximum Ratings[(1)(2)]

	MIN	MAX	UNIT
Supply Voltage (VDD)	-0.5	+2.75	V
Supply Voltage (VIN)	-0.5	+4.0	V
LVCMOS Input/Output Voltage	-0.5	+4.0	V
CML Input Voltage	-0.5	(VDD+0.5)	V
CML Input Current	-30	+30	mA
Junction Temperature		125	°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied.
(2) For soldering specifications, see SNOA549.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage Temperature Range		-40	+125	°C
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	-5	5	kV
		Machine model (MM), STD - JESD22-A115-A		100	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]		1250	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[(1)]

	MIN	TYP	MAX	UNIT
Supply Voltage (2.5 V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3 V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V

(1) The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

7.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CURRENT						
IDD	Supply Current	TX_DIS = Low, EQ = ON VOD_SEL = Float (1000 mVpp)		50	63	mA
		Auto Low Power Mode TX_DIS = Low, MODE = 20 kΩ VID CHA and CHB = 0.0 V VOD_SEL = Float (1000 mVpp)		12	15	
		TX_DIS = High		25	35	
LVCMOS DC SPECIFICATIONS						
V_{IH25}	High Level Input Voltage, 2-Level LVCMOS	2.5 V Supply Mode	2.0		VDD	V
V_{IH33}	High Level Input Voltage, 2-Level LVCMOS	3.3 V Supply Mode	2.0		VIN	V
V_{IL}	Low Level Input Voltage, 2-Level LVCMOS		GND		0.7	V

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Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	I_{OH} = -4.0 mA (1)	2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
I_{IN}	Input Leakage Current	Vinput = 0 V or VDD VDD_SEL = Float	-15		+15	µA
		Vinput = 0 V or VIN VDD_SEL = Low	-15		+15	
I_{IN-P}	Input Leakage Current 4-Level Input (2)	Vinput = 0 V or VDD - 0.05 V VDD_SEL = Float Vinput = 0 V or VIN - 0.05 V VDD_SEL = Low	-160		+80	µA
CML RECEIVER INPUTS						
V_{TX}	Source Transmit Launch Differential Signal Level	Default power-up conditions ENSMB = 0 or 1	190	800	1600	mVp-p
RL_{RX-IN}	RX return loss	SDD11 @ 4.1 GHz		-12		dB
		SDD11 @ 11.1 GHz		-8		
		SCD11 @ 11.1 GHz		-10		
HIGH SPEED TRANSMITTER OUTPUTS						
V_{OD1}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = Low (700 mVpp setting) DE = Low	500	650	800	mVp-p
V_{OD2}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = Float (1000 mVpp setting) DE = Low	800	1000	1100	
V_{OD3}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = 20 kΩ to GND (1200 mVpp) DE = Low	950	1150	1350	
V_{OD_DE1}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = Float (1000 mVpp) DE = Float		-3		dB
V_{OD_DE2}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = Float (1000 mVpp) DE = 20 kΩ to GND		-6		dB

(1) VOH only applies to the $\overline{\text{DONE}}$ pin; LOS, SCL, and SDA are open-drain outputs that have no internal pull-up capability. $\overline{\text{DONE}}$ is a full LVCMOS output with pull-up and pull-down capability.
(2) Input is held to a maximum of 50 mV below VDD or VIN to simulate the use of a 1 kΩ resistor on the input.

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Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD_DE3}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50 Ω to GND VOD_SEL = Float (1000 mVpp) DE = High		-9		dB
V_{CM-AC}	Output Common-Mode Voltage	AC Common Mode Voltage DE = 0 dB, VOD ≤ 1000 mVpp		4.5		mV (rms)
V_{CM-DC}	Output DC Common-Mode Voltage	DC Common Mode Voltage	0	1.1	1.9	V
V_{IDLE}	TX IDLE Output Voltage	VID = 0 mVp-p			30	mV
$RL_{TX-DIFF}$	TX return loss	SDD22 @ 4.1 GHz		-13		dB
		SDD22 @ 11.1 GHz		-9		
		SCC22 @ 2.5 GHz		-22		
		SCC22 @ 11.1 GHz		-10		
$Delta_Z_M$	Transmitter Termination Mismatch	DC, I_{FORCE} = ± 100 µA (3)		2.5%		
$T_{R/F}$	Transmitter Rise and Fall Time	Measurement points at 20% - 80% (4)		38		ps
T_{PD}	Propagation Delay	Measured at 50% crossing EQ = 0x00		230		ps
T_{CCSK}	Channel to Channel Skew	T = 25°C, VDD = 2.5 V		7		ps
T_{PPSK}	Part to Part Skew	T = 25°C, VDD = 2.5 V		20		ps
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to transition to idle after differential signal	VIN = 1 Vpp, 10 Gbps EQ = 0x00, DE = 0 dB		6.5		ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to transition to valid differential signal after idle	VIN = 1 Vpp, 10 Gbps EQ = 0x00, DE = 0 dB		3.2		ns
$T_{ENV_DISTORT}$	Active OOB timing distortion, input active time vs. output active time			3.3		ns
OUTPUT JITTER SPECIFICATIONS (5)						
R_J	Random Jitter	No Media Source Amplitude = 700 mVpp, PRBS15 pattern, 10.3125 Gbps VOD = Default, EQ = minimum, DE = 0 dB		0.3		ps (rms)
D_{J1}	Deterministic Jitter			0.09		UI
EQUALIZATION						
D_{JE1}	Residual Deterministic Jitter	10.3125 Gbps 8 meter 30AWG Cable on Input Source = 700 mVpp, PRBS15 pattern EQ = 0x0F		0.27		UI
D_{JE2}	Residual Deterministic Jitter	10.3125 Gbps 30" 4-mil FR4 on Inputs Source = 700 mVpp, PRBS15 pattern EQ = 0x16		0.17		UI
DE-EMPHASIS						
D_{JD1}	Residual Deterministic Jitter	10.3125 Gbps 10” 4 mil stripline FR4 on Outputs Source = 700 mVpp, PRBS15 pattern EQ = Min, VOD = 1200 mVpp, DE = -3.5 dB		0.13		UI

(3) Force ±100 µA on output, measure ΔV on the Output and calculate impedance. Mismatch is the percentage difference of OUTn+ and OUTn- impedance driving the same logic state.
(4) Default VOD used for testing. DE = -1.5 dB level used to compensate for fixture attenuation.
(5) Typical jitter reported is determined by jitter decomposition software on the DSA8200 Oscilloscope.

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7.5 Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL BUS INTERFACE DC SPECIFICATIONS (1)						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	See (2)	-200		+200	µA
C_I	Capacitance for SDA and SCL	See (2) (3) (4)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3 V, See (2) (3) (5)		2000		Ω
		Pullup V_{DD} = 2.5 V, See (2) (3) (5)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = Float (Master Mode) (1)	280	400	520	kHz
T_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
$T_{SU:STA}$	Repeated Start Condition Setup Time		0.6			µs
$T_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$T_{HD:DAT}$	Data Hold Time		0			ns
$T_{SU:DAT}$	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	See (6)	0.6		50	µs
t_F	Clock/Data Fall Time	See (6)			300	ns
t_R	Clock/Data Rise Time	See (6)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	See (4) (6)			500	ms

(1) EEPROM interface requires 1 MHz capable EEPROM device.
(2) Recommended value.
(3) Recommended maximum capacitance load per bus segment is 400 pF.
(4) Ensured by design and characterization. Parameter not tested in production.
(5) Maximum termination voltage should be identical to the device supply voltage.
(6) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

7.6 Timing Requirements — LOS and ENABLE / DISABLE Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{LOS_OFF}	Input IDLE to Active RX_LOS response time	See (1)		0.035		µs
T_{LOS_ON}	Input Active to IDLE RX_LOS response time	See (1)		0.4		µs
T_{OFF}	TX Disable assert Time TX_DIS = High to Output OFF	See (1)		0.005		µs
T_{ON}	TX Disable negateTime TX_DIS = Low to Output ON	See (1)		0.150		µs
T_{LP_EXIT}	Auto Low Power Exit ALP to Normal Operation	See (1)		150		ns
T_{LP_ENTER}	Auto Low Power Enter Normal Operation to Auto Low Power	See (1)		100		µs

(1) Parameter not tested in production.

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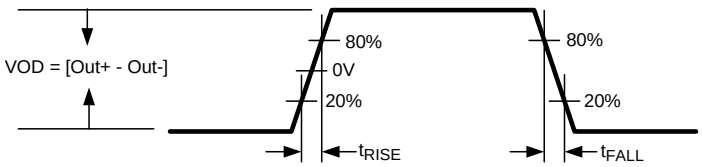

Figure 1. Output Rise and Fall Transition Times

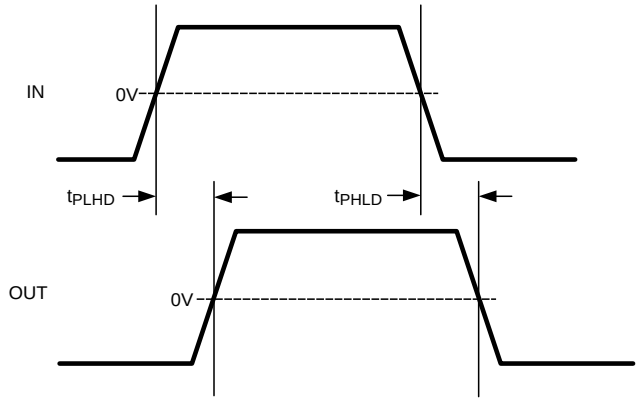

Figure 2. Propagation Delay Timing Diagram

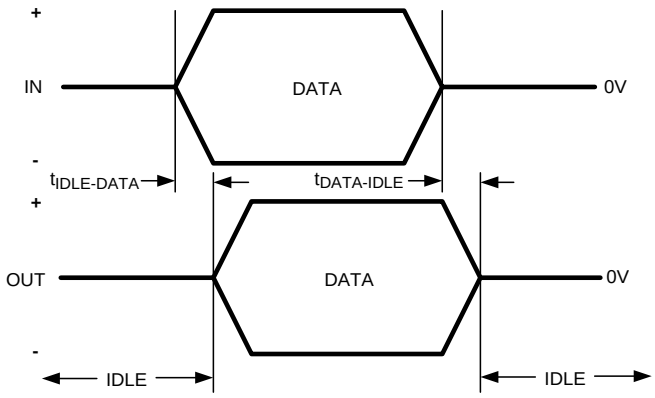

Figure 3. Transmit Idle-Data and Data-Idle Response Time

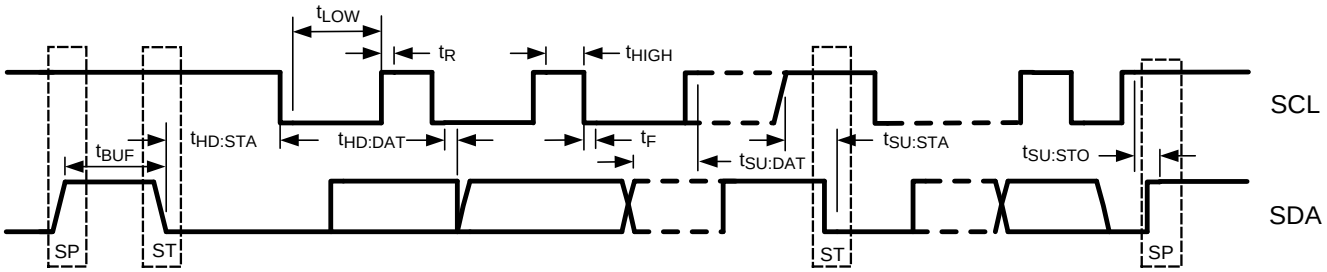

Figure 4. SMBus Timing Parameters

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7.7 Typical Characteristics

The following data was collected at 25°C.

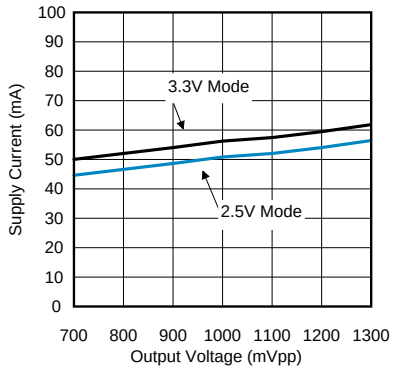
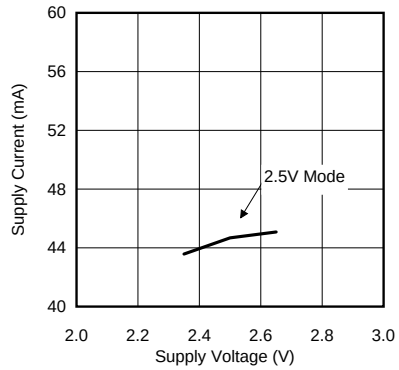


Figure 5. Supply Current vs. Output Voltage Setting



VOD = 700 mVpp

Figure 6. Supply Current vs. Supply Voltage

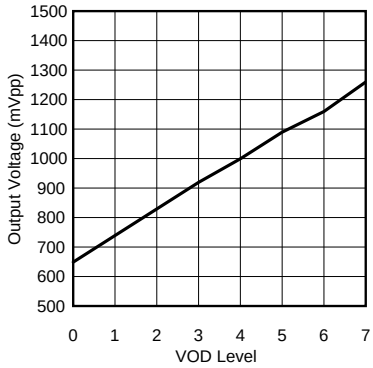


Figure 7. Output Voltage vs. Output Voltage Setting

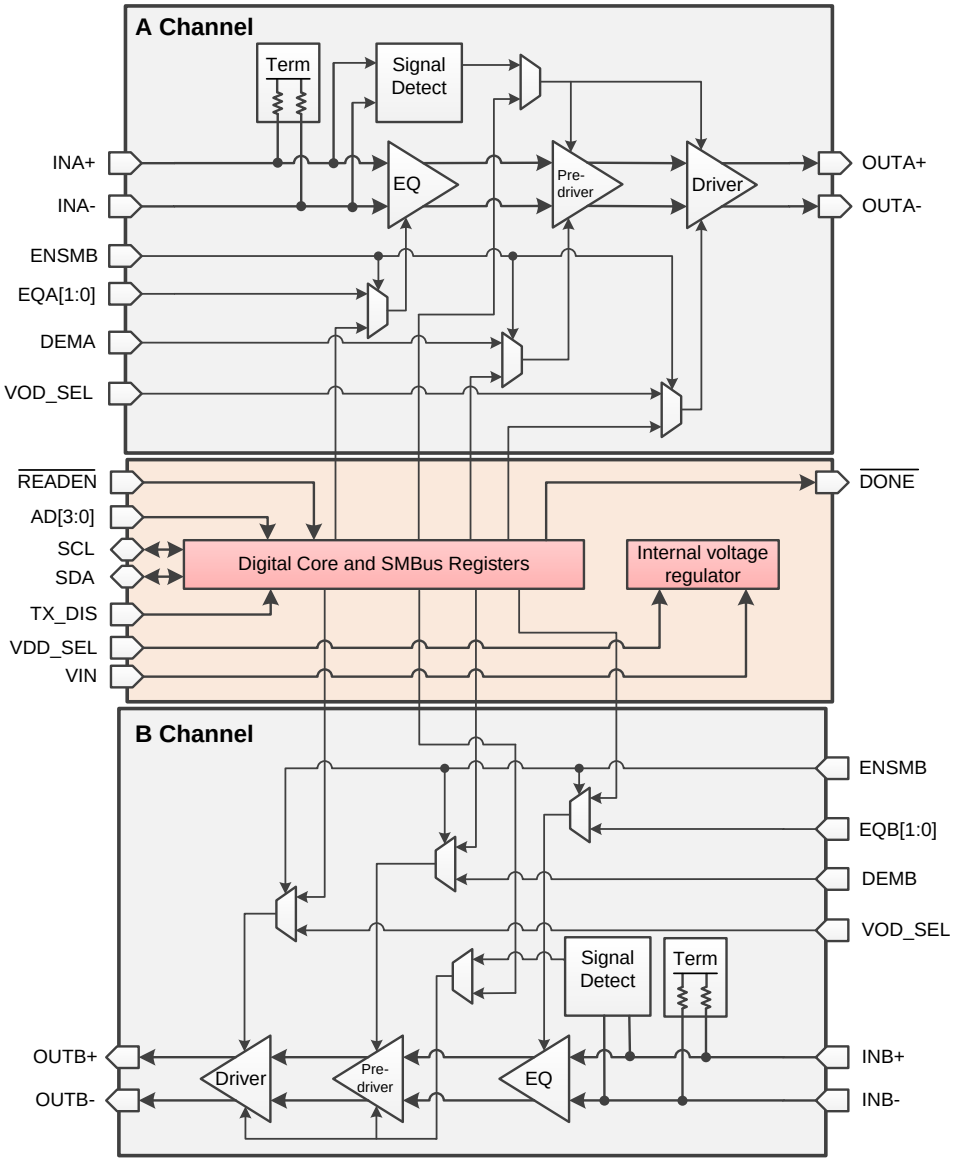
8 Detailed Description

8.1 Overview

The DS100BR111 is a high performance bidirectional 1-lane repeater optimized for 10G-KR and SAS/SATA operation, where its programmable equalization and de-emphasis compensate for lossy FR-4 printed circuit board backplanes or balanced cables. The DS100BR111 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1), and SMBus Master Mode (ENSMB = Float) to load register information from external EEPROM.

Each channel has a signal detector circuit that monitors the input signal amplitude. When the input signal level is below the detector's de-assert level, the output is disabled. When input signal level exceeds the detector's assert level, the output is enabled. The signal detector circuit is used to support the OOB signaling used in SAS and SATA.

8.2 Functional Block Diagram



Note: This diagram is representative of device signal flow only.

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8.3 Feature Description

8.3.1 4-Level Control Pin Settings

The 4-level input pins use a resistor divider to set the four valid control levels and provide a wider range of control settings when ENSMB = 0. There is an internal 30-kΩ pull-up and a 60-kΩ pull-down connected to the package pin. These resistors, together with the external resistor connection, combine to achieve the desired voltage level. By using the 1-kΩ pull-down, 20-kΩ pull-down, no connect, or 1-kΩ pull-up, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4–Level Control Pin Settings Table

		RESULTING PIN VOLTAGE	
LEVEL	**SETTING**	**3.3 V MODE**	**2.5 V MODE**
0	Tie 1 kΩ to GND	0.10 V	0.08 V
R	Tie 20 kΩ to GND	1/3 x V_{IN}	1/3 x V_{DD}
F	Float (leave pin open)	2/3 x V_{IN}	2/3 x V_{DD}
1	Tie 1 kΩ to V_{IN} or V_{DD}	V_{IN} - 0.05 V	V_{DD} - 0.04 V

Typical 4-Level Input Thresholds:

- Internal Threshold between 0 and R = 0.2 * V_{IN} or V_{DD}
- Internal Threshold between R and F = 0.5 * V_{IN} or V_{DD}
- Internal Threshold between F and 1 = 0.8 * V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5-V regulator, the 1-kΩ pull-up / pull-down resistors are recommended. If several four level inputs require the same setting, it is possible to combine two or more 1-kΩ resistors into a single lower value resistor. As an example, combining two inputs with a single 500-Ω resistor is a valid way to save board space.

8.4 Device Functional Modes

8.4.1 Pin Control Mode

When in Pin Mode (ENSMB = 0), equalization, de-emphasis, and VOD (output amplitude) can be selected via external pin control for both the A-channel and B-channel. Equalization and de-emphasis can be programmed by pin selection for each side independently. For further device control, the VOD_SEL and MODE pins are available to improve DS100BR111 performance depending on design applications. The receiver electrical idle detect threshold is also adjustable via the SD_TH pin. Pin control mode is ideal in situations where neither MCU or EEPROM is available to access the device via SMBus SDA and SCL lines.

8.4.2 SMBus Slave Mode

When in Slave SMBus Mode (ENSMB = 1), equalization, de-emphasis, and VOD (output amplitude) are all programmable on an individual channel basis. Upon assertion of ENSMB, the EQx, DEMx, and VODx settings are controlled by SMBus immediately. It is important to note that SMBus settings can only be changed from their defaults after asserting Register Enable by setting Reg 0x06[3] = 1. The EQx, DEMx, and VODx pins are subsequently converted to AD0-AD3 SMBus address inputs. The other external control pins (TX_DIS, MODE, and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set. If the user overrides a pin control, the input voltage level of that control pin is ignored until ENSMB is driven low (Pin Mode). In the event that channels are powered down via the TX_DIS pin, register setting states are not affected.

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Device Functional Modes (continued)

Table 2. Signal Detect Threshold Level (1)

LEVEL	SD_TH (Pin 14)	SMBus REG BIT [3:2] and [1:0]	TYPICAL ASSERT LEVEL (mVpp)	TYPICAL DE-ASSERT LEVEL (mVpp)
1	0	10	210	150
2	R	01	160	100
3	F (Default)	00	180	110
4	1	11	190	130

(1) Typical assert and de-assert levels were measured with VDD = 2.5 V, 25°C, and 010101 pattern at 8 Gbps.

8.4.3 SMBus Master Mode

When in SMBus Master Mode (ENSMB = Float), the equalization, de-emphasis, and VOD (output amplitude) for multiple devices can be loaded via external EEPROM. By asserting a Float condition on the ENSMB pin, an external EEPROM writes register settings to each device in accordance with its SMBus slave address. The settings programmable by external EEPROM provide only a subset of all the register bits available via SMBus Slave Mode, and the bit-mapping between SMBus Slave Mode registers and EEPROM addresses can be referenced in Table 6. Once the EEPROM successfully finishes loading each device's register settings, the device reverts back to SMBus Slave Mode and releases SDA and SCL control to an external master MCU. If the EEPROM fails to load settings to a particular device, for example due to an invalid or blank hex file, the device waits indefinitely in an unknown state where access to the SMBus lines is not possible.

8.4.4 Signal Conditioning Settings

Equalization, de-emphasis, and VOD settings accessible via the pin controls are chosen to meet the needs of most high speed applications. For additional levels and flexibility in EQ, de-emphasis, and VOD programming, these settings can be controlled via the SMBus registers. Each control pin input has a total of four possible voltage level settings. In pin mode, Table 3 shows the 16 EQ settings available, and Table 4 shows the 16 de-emphasis and VOD combination settings available. Note that when in pin mode, only 16 of a possible 256 EQ programmable levels can be accessed by setting the EQx[1:0] pins. In addition, each pin setting applied to the VOD_SEL and DEMx pin input programs a fixed combination of VOD and de-emphasis. In order to access all 256 EQ levels and control both VOD and de-emphasis settings independently, SMBus register access must be used.

Table 3. Equalizer Settings

EQUALIZATION BOOST RELATIVE TO DC					
LEVEL	EQA1 EQB1	EQA0 EQB0	EQ — 8 bits [7:0]	dB BOOST at 5 GHz	SUGGESTED MEDIA (1)
1	0	0	0000 0000 = 0x00	2.5	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	6.5	FR4 5 inch trace
3	0	F	0000 0010 = 0x02	9	FR4 10 inch trace
4	0	1	0000 0011 = 0x03	11.5	FR4 15 inch trace
5	R	0	0000 0111 = 0x07	14	FR4 20 inch trace
6	R	R	0001 0101 = 0x15	15	FR4 25 inch trace
7	R	F	0000 1011 = 0x0B	17	FR4 25 inch trace
8	R	1	0000 1111 = 0x0F	19	7m 30 AWG Cable
9	F	0	0101 0101 = 0x55	20	FR4 30 inch trace

(1) Settings are approximate and will change based on PCB material, trace dimensions, and driver waveform characteristics. Optimal EQ settings should be determined via simulation and prototype verification.

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Table 3. Equalizer Settings (continued)

EQUALIZATION BOOST RELATIVE TO DC					
LEVEL	EQA1 EQB1	EQA0 EQB0	EQ — 8 bits [7:0]	dB BOOST at 5 GHz	SUGGESTED MEDIA (1)
10	F	R	0001 1111 = 0x1F	23	8m 30 AWG Cable FR4 35 inch trace
11	F	F	0010 1111 = 0x2F	25	10m 30 AWG Cable
12	F	1	0011 1111 = 0x3F	27	10m to 12m, Cable
13	1	0	1010 1010 = 0xAA	30	
14	1	R	0111 1111 = 0x7F	31	
15	1	F	1011 1111 = 0xBF	33	
16	1	1	1111 1111 = 0xFF	34	

Table 4. De-Emphasis and Output Voltage Settings (1)

LEVEL	VOD_SEL (2) (3)	DEMA/B	SMBus REGISTER DEM Level	SMBus REGISTER VOD LEVEL	VOD (mVpp)	DEM (dB)
1	0	0	000	000	700	0
2	0	F	010	000	700	-3.5
3	0	R	011	000	700	-6
4	0	1	101	000	700	-9
5	F	0	000	011	1000	0
6	F	F	010	011	1000	-3.5
7	F	R	011	011	1000	-6
8	F	1	101	011	1000	-9
9	R	0	000	101	1200	-0
10	R	F	010	101	1200	-3.5
11	R	R	011	101	1200	-6
12	R	1	101	101	1200	-9
13	1	0	000	100	1100	0
14	1	F	001	100	1100	-1.5
15	1	R	001	110	1300	-1.5
16	1	1	010	110	1300	-3.5

(1) The DS100BR111 VOD for OUTPUT A is limited to 700 mVpp in pin mode (ENSMB=0). With ENSMB = 1 or Float, the VOD for OUTPUT A can be adjusted with SMBus register 0x23 [4:2] as shown in Table 9.
(2) When VOD_SEL is in the Logic 1 state (1 kΩ resistor to VIN or VDD), the DS100BR111 will support 10G-KR back-channel communication using pin control.
(3) In SMBus Mode, if VOD_SEL is in the Logic 1 state (1 kΩ resistor to VIN or VDD), the DS100BR111 AD0-AD3 pins are internally forced to 0.

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8.5 Programming

8.5.1 System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible with the SMBus 2.0 physical layer specification. Tie ENSMB = 1 kΩ to VDD (2.5 V mode) or VIN (3.3 V mode) to enable SMBus Slave Mode and allow access to the configuration registers.

The DS100BR111 uses AD[3:0] inputs in both SMBus Modes. These AD[3:0] pins are the user set SMBus slave address inputs and have internal pull-downs. Based on the SMBus 2.0 specification, the DS100BR111 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). When AD[3:0] pins are left floating or pulled low, AD[3:0] = 0000'b, and the device default address byte is 0xB0. The device supports up to 16 address bytes, as shown in Table 5.

Table 5. Device Slave Address Bytes

AD[3:0] SETTINGS	FULL SLAVE ADDRESS BYTE (7-Bit ADDRESS + WRITE BIT)	7-Bit SLAVE ADDRESS (HEX)
0000	B0	58
0001	B2	59
0010	B4	5A
0011	B6	5B
0100	B8	5C
0101	BA	5D
0110	BC	5E
0111	BE	5F
1000	C0	60
1001	C2	61
1010	C4	62
1011	C6	63
1100	C8	64
1101	CA	65
1110	CC	66
1111	CE	67

The SDA and SCL pins are 3.3 V tolerant, but are not 5 V tolerant. An external pull-up resistor is required on the SDA and SCL line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading, and speed.

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8.5.2 Transfer Of Data Via the SMBus

During normal operation, the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

- **START:** A High-to-Low transition on SDA while SCL is High indicates a message START condition.
- **STOP:** A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.
- **IDLE:** If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH}, then the bus will transfer to the IDLE state.

8.5.3 SMBus Transactions

The device supports WRITE and READ transactions. See Table 9 for register address, type (Read/Write, Read Only), default value, and function information.

8.5.4 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification):

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

Once the WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

8.5.5 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification):

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

Once the READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see Table 9 for more information.

8.5.6 EEPROM Programming

The DS100BR111 supports reading directly from an external EEPROM device by implementing SMBus Master mode. When used in SMBus Master mode, the DS100BR111 will read directly from a specific location in the external EEPROM. When designing a system that uses external EEPROM, the following guidelines should be followed:

- Set the DS100BR111 in SMBus Master Mode.
  - ENSMB (Pin 3) = Float
- The external EEPROM device must support 1 MHz operation.
- The external EEPROM device address byte must be 0xA0.
- Set the AD[3:0] inputs for SMBus address byte. When AD[3:0] = 0000'b, the device address byte is 0xB0.
- The device address can be set with the use of the AD[3:0] input up to 16 different addresses. Use the example below to set each of the SMBus addresses.
  - AD[3:0] = 0001'b, the device address byte is 0xB2
  - AD[3:0] = 0010'b, the device address byte is 0xB4
  - AD[3:0] = 0011'b, the device address byte is 0xB6
  - AD[3:0] = 0100'b, the device address byte is 0xB8
- The master implementation in the DS100BR111 supports multiple devices reading from one EEPROM. When tying multiple devices to the SDA and SCL pins, use these guidelines:
  - Use adjacent SMBus addresses for the 4 devices
  - Use a pull-up resistor on SDA; value = 4.7 kΩ
  - Use a pull-up resistor on SCL: value = 4.7 kΩ
  - Daisy-chain $\overline{\text{READEN}}$ (Pin 17) and $\overline{\text{DONE}}$ (Pin 18) from one device to the next device in the sequence.
    1. Tie $\overline{\text{READEN}}$ of the 1st device in the chain (U1) to GND
    2. Tie $\overline{\text{DONE}}$ of U1 to $\overline{\text{READEN}}$ of U2
    3. Tie $\overline{\text{DONE}}$ of U2 to $\overline{\text{READEN}}$ of U3
    4. Tie $\overline{\text{DONE}}$ of U3 to $\overline{\text{READEN}}$ of U4
    5. Optional: Tie $\overline{\text{DONE}}$ of U4 to a LED to show each of the devices have been loaded successfully

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8.5.6.1 Master EEPROM Programming

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS100BR111 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the same SMBus line. There is a CRC enable flag to enable or disable CRC checking. There is a MAP bit to flag the presence of an address map that specifies the configuration data start address in the EEPROM. If the MAP bit is not present, the configuration data start address immediately follows the 3-byte base header. A bit to indicate an EEPROM size > 256 bytes is necessary to address the EEPROM properly. There are 37 bytes of data size for each DS100BR111 device. For more details about EEPROM programming and Master mode, refer to SNLA228.

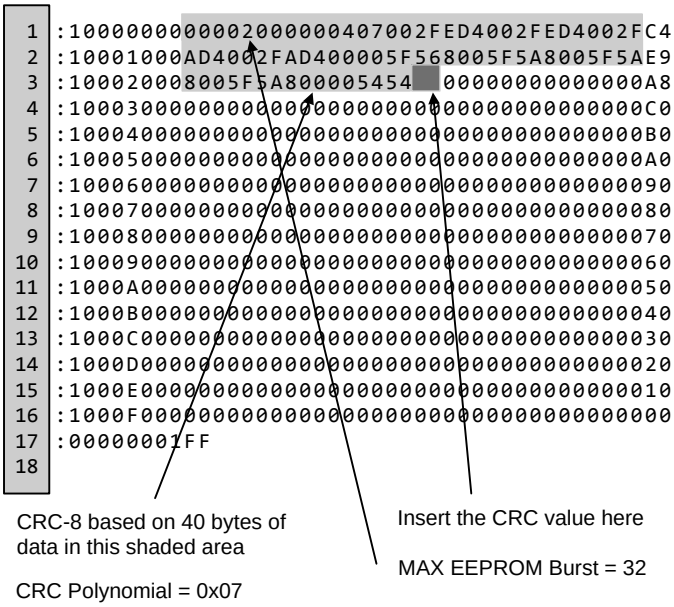

Figure 8. Typical EEPROM Data Set

NOTE

The maximum EEPROM size supported is 8 kbits (1024 x 8 bits).

The CRC-8 calculation is performed for each device on the first 3 bytes of header information plus the 37 bytes of data for the DS100BR111 or 40 bytes in total. The result of this calculation is placed immediately after the DS100BR111 data in the EEPROM which ends with "5454". The CRC-8 in the DS100BR111 uses a polynomial = $x^8 + x^2 + x + 1$.

There are two pins that provide unique functions in SMBus Master mode:

- $\overline{\text{DONE}}$
- $\overline{\text{READEN}}$

When the DS100BR111 is powered up in SMBus Master mode, it reads its configuration from the external EEPROM when the $\overline{\text{READEN}}$ pin goes low. When the DS100BR111 is finished reading its configuration from the external EEPROM, it drives the $\overline{\text{DONE}}$ pin low. In applications where there is more than one DS100BR111 on the same SMBus, bus contention can result if more than one DS100BR111 tries to take control of the SMBus at the same time. The $\overline{\text{READEN}}$ and $\overline{\text{DONE}}$ pins prevent this bus contention. The system should be designed so that the $\overline{\text{READEN}}$ pin from one DS100BR111 in the system is driven low on power-up. This DS100BR111 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When the first DS100BR111 is finished reading its configuration, it will drive the $\overline{\text{DONE}}$ pin low. This pin should be

connected to the $\overline{\text{READEN}}$ pin of another DS100BR111. When this second DS100BR111 senses its $\overline{\text{READEN}}$ pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its $\overline{\text{DONE}}$ pin low. By connecting the $\overline{\text{DONE}}$ pin of each DS100BR111 to the $\overline{\text{READEN}}$ pin of the next DS100BR111, each DS100BR111 can read its initial configuration from the EEPROM without causing bus contention.

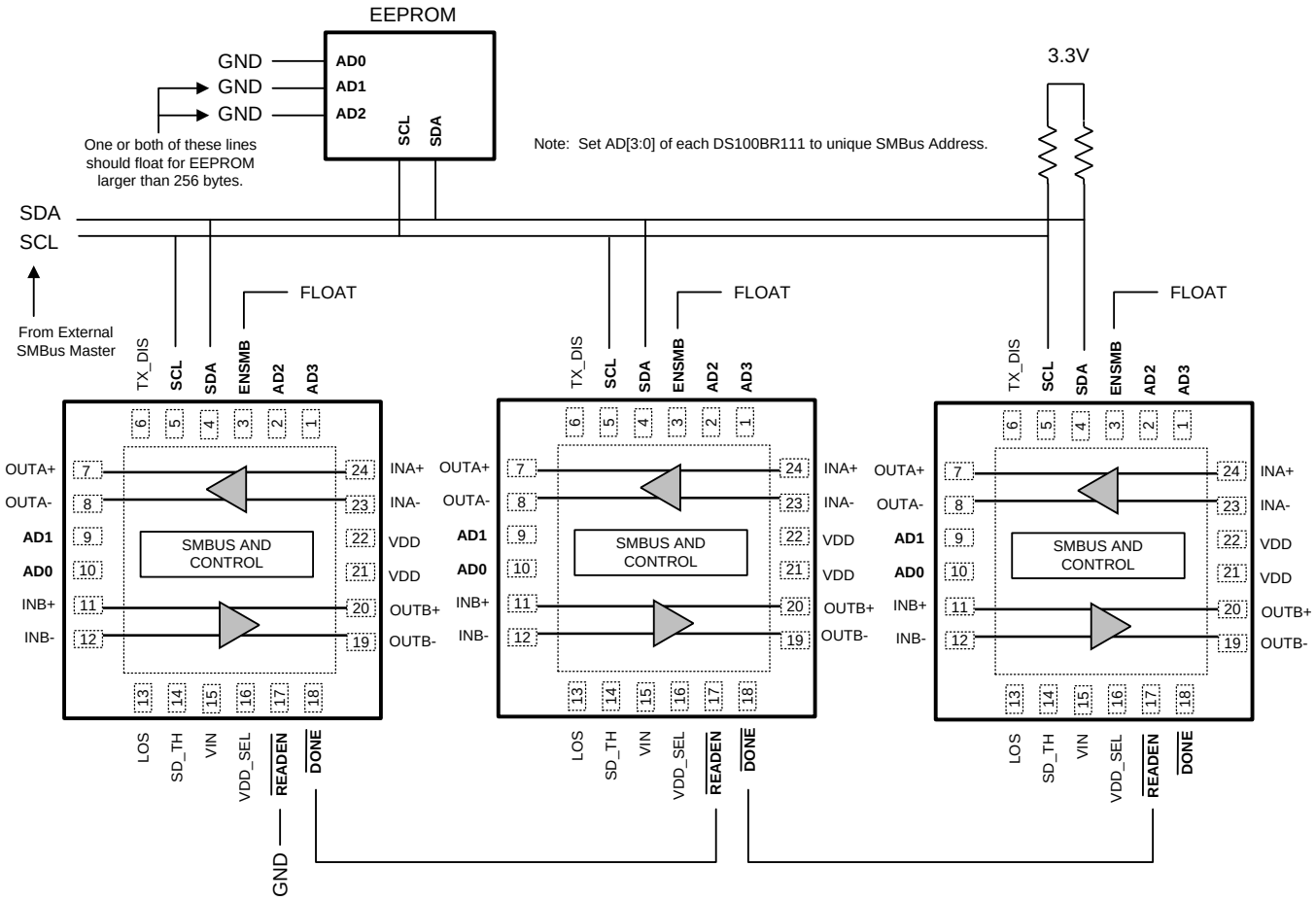

Figure 9. Typical Multi-device EEPROM Connection Diagram

8.5.6.2 EEPROM Address Mapping

A detailed EEPROM Address Mapping for a single device is shown in Table 6. For instances where multiple devices are written to EEPROM, the device starting address definitions align starting with Byte 0x03. A register map overview for a multi-device EEPROM address map is shown in Table 7.

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Table 6. Single Device with Default Value

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x00	CRC_EN	Address Map Present	EEPROM > 256 Bytes	Reserved	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x01	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x02	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x03	Cont_talk_EN_CHA	Cont_talk_EN_CHB	Reserved	Reserved	Reserved	Sel_LOS	Reserved	Reserved
SMBus Register			0x01[7]	0x01[6]	0x01[5]	0x01[4]	0x01[3]	0x01[2]	0x01[1]	0x01[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x04	Ovrd_LOS	LOS_Value	PWDN_Inputs	PWDN_Osc	Reserved	eSATA En CHA	eSATA En CHB	Ovrd TX_DIS
SMBus Register			0x02[5]	0x02[4]	0x02[3]	0x02[2]	0x02[0]	0x04[7]	0x04[6]	0x04[5]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x05	TX_DIS CHA	TX_DIS CHB	Reserved	EQ Stage 4 CHB	EQ Stage 4 CHA	Reserved	Ovrd IDLE_TH	Reserved
SMBus Register			0x04[4]	0x04[3]	0x04[2]	0x04[1]	0x04[0]	0x06[4]	0x08[6]	0x08[5]
Default Value	0x04		0	0	0	0	0	1	0	0
Description		0x06	Ovrd IDLE	Reserved	Ovrd Out_Mode	Ovrd DEM	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x08[4]	0x08[3]	0x08[2]	0x08[1]	0x08[0]	0x0B[6]	0x0B[5]	0x0B[4]
Default Value	0x07		0	0	0	0	0	1	1	1
Description		0x07	Reserved	Reserved	Reserved	Reserved	CHA_Idle_Auto	CHA_Idle_Sel	Reserved	Reserved
SMBus Register			0x0B[3]	0x0B[2]	0x0B[1]	0x0B[0]	0x0E[5]	0x0E[4]	0x0E[3]	0x0E[2]
Default Value	0x00		0	0	0	0	0	0	0	0

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Table 6. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x08	CHA_EQ[7]	CHA_EQ[6]	CHA_EQ[5]	CHA_EQ[4]	CHA_EQ[3]	CHA_EQ[2]	CH0_EQ[1]	CH0_EQ[0]
SMBus Register			0x0F[7]	0x0F[6]	0x0F[5]	0x0F[4]	0x0F[3]	0x0F[2]	0x0F[1]	0x0F[0]
Default Value	0x2F		0	0	1	0	1	1	1	1
Description		0x09	CHA_Sel SCP	CHA_Out Mode	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x10[7]	0x10[6]	0x10[5]	0x10[4]	0x10[3]	0x10[2]	0x10[1]	0x10[0]
Default Value	0xED		1	1	1	0	1	1	0	1
Description		0x0A	CHA_DEM[2]	CHA_DEM[1]	CHA_DEM[0]	Reserved	CHA_Idle_ThA[1]	CHA_Idle_ThA[0]	CHA_Idle_ThD[1]	CHA_Idle_ThD[0]
SMBus Register			0x11[2]	0x11[1]	0x11[0]	0x12[7]	0x12[3]	0x12[2]	0x12[1]	0x12[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x0B	CHB_Idle_Auto	CHB_Idle_Sel	Reserved	Reserved	CHB_EQ[7]	CHB_EQ[6]	CHB_EQ[5]	CHB_EQ[4]
SMBus Register			0x15[5]	0x15[4]	0x15[3]	0x15[2]	0x16[7]	0x16[6]	0x16[5]	0x16[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x0C	CHB_EQ[3]	CHB_EQ[2]	CHB_EQ[1]	CHB_EQ[0]	CHB_Sel SCP	CHB_Out Mode	Reserved	Reserved
SMBus Register			0x16[3]	0x16[2]	0x16[1]	0x16[0]	0x17[7]	0x17[6]	0x17[5]	0x17[4]
Default Value	0xFE		1	1	1	1	1	1	1	0
Description		0x0D	Reserved	Reserved	Reserved	Reserved	CHB_DEM[2]	CHB_DEM[1]	CHB_DEM[0]	Reserved
SMBus Register			0x17[3]	0x17[2]	0x17[1]	0x17[0]	0x18[2]	0x18[1]	0x18[0]	0x19[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x0E	CHB_Idle_ThA[1]	CHB_Idle_ThA[0]	CHB_Idle_ThD[1]	CHB_Idle_ThD[0]	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x19[3]	0x19[2]	0x19[1]	0x19[0]	0x1C[5]	0x1C[4]	0x1C[3]	0x1C[2]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1D[7]	0x1D[6]	0x1D[5]	0x1D[4]	0x1D[3]	0x1D[2]	0x1D[1]	0x1D[0]
Default Value	0x2F		0	0	1	0	1	1	1	1

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Table 6. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1E[7]	0x1E[6]	0x1E[5]	0x1E[4]	0x1E[3]	0x1E[2]	0x1E[1]	0x1E[0]
Default Value	0xAD		1	0	1	0	1	1	0	1
Description		0x11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1F[2]	0x1F[1]	0x1F[0]	0x20[7]	0x20[3]	0x20[2]	0x20[1]	0x20[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x12	Reserved	CHA_VOD[2]	CHA_VOD[1]	CHA_VOD[0]	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x23[5]	0x23[4]	0x23[3]	0x23[2]	0x24[7]	0x24[6]	0x24[5]	0x24[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x24[3]	0x24[2]	0x24[1]	0x24[0]	0x25[7]	0x25[6]	0x25[5]	0x25[4]
Default Value	0xFA		1	1	1	1	1	0	1	0
Description		0x14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x25[3]	0x25[2]	0x25[1]	0x25[0]	0x26[2]	0x26[1]	0x26[0]	0x27[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x15	Reserved	Reserved	Reserved	Reserved	Ovrd_Fast IDLE	hi_idle_th_CHA	hi_idle_th_CHB	fast_idle_CHA
SMBus Register			0x27[3]	0x27[2]	0x27[1]	0x27[0]	0x28[6]	0x28[5]	0x28[4]	0x28[3]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x16	fast_idle_CHB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x28[2]	0x28[1]	0x28[0]	0x2B[5]	0x2B[4]	0x2B[3]	0x2B[2]	0x2C[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2C[6]	0x2C[5]	0x2C[4]	0x2C[3]	0x2C[2]	0x2C[1]	0x2C[0]	0x2D[7]
Default Value	0x5F		0	1	0	1	1	1	1	1

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Table 6. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x18	Reserved	Reserved	CHB_VOD[2]	CHB_VOD[1]	CHB_VOD[0]	Reserved	Reserved	Reserved
SMBus Register			0x2D[6]	0x2D[5]	0x2D[4]	0x2D[3]	0x2D[2]	0x2D[1]	0x2D[0]	0x2E[2]
Default Value	0x5A		0	1	0	1	1	0	1	0
Description		0x19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2E[1]	0x2E[0]	0x2F[7]	0x2F[3]	0x2F[2]	0x2F[1]	0x2F[0]	0x32[5]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x1A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x32[4]	0x32[3]	0x32[2]	0x33[7]	0x33[6]	0x33[5]	0x33[4]	0x33[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x33[2]	0x33[1]	0x33[0]	0x34[7]	0x34[6]	0x34[5]	0x34[4]	0x34[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x34[2]	0x34[1]	0x34[0]	0x35[2]	0x35[1]	0x35[0]	0x36[7]	0x36[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x36[2]	0x36[1]	0x36[0]	0x39[5]	0x39[4]	0x39[3]	0x39[2]	0x3A[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x1E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3A[6]	0x3A[5]	0x3A[4]	0x3A[3]	0x3A[2]	0x3A[1]	0x3A[0]	0x3B[7]
Default Value	0x5F		0	1	0	1	1	1	1	1
Description		0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3B[6]	0x3B[5]	0x3B[4]	0x3B[3]	0x3B[2]	0x3B[1]	0x3B[0]	0x3C[2]
Default Value	0x5A		0	1	0	1	1	0	1	0

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Table 6. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3C[1]	0x3C[0]	0x3D[7]	0x3D[3]	0x3D[2]	0x3D[1]	0x3D[0]	0x40[5]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x21	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x40[4]	0x40[3]	0x40[2]	0x41[7]	0x41[6]	0x41[5]	0x41[4]	0x41[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x22	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x41[2]	0x41[1]	0x41[0]	0x42[7]	0x42[6]	0x42[5]	0x42[4]	0x42[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x23	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x42[2]	0x42[1]	0x42[0]	0x43[2]	0x43[1]	0x43[0]	0x44[7]	0x44[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x44[2]	0x44[1]	0x44[0]	0x47[3]	0x47[2]	0x47[1]	0x47[0]	0x48[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x48[6]	0x4C[7]	0x4C[6]	0x4C[5]	0x4C[4]	0x4C[3]	0x4C[0]	0x59[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5A[7]	0x5A[6]	0x5A[5]	0x5A[4]	0x5A[3]	0x5A[2]	0x5A[1]	0x5A[0]
Default Value	0x54		0	1	0	1	0	1	0	0
Description		0x27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5B[7]	0x5B[6]	0x5B[5]	0x5B[4]	0x5B[3]	0x5B[2]	0x5B[1]	0x5B[0]
Default Value	0x54		0	1	0	1	0	1	0	0

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Table 7. Multi-Device EEPROM Address Map Overview(1)

	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Header	0	CRC EN	Address Map	EEPROM > 256 Bytes	Reserved	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	2	EE Burst[7]	EE Burst[6]	EE Burst[5]	EE Burst[4]	EE Burst[3]	EE Burst[2]	EE Burst[1]	EE Burst[0]
Device 0 Info	3	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	4	EE AD0 [7]	EE AD0 [6]	EE AD0 [5]	EE AD0 [4]	EE AD0 [3]	EE AD0 [2]	EE AD0 [1]	EE AD0 [0]
Device 1 Info	5	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	6	EE AD1 [7]	EE AD1 [6]	EE AD1 [5]	EE AD1 [4]	EE AD1 [3]	EE AD1 [2]	EE AD1 [1]	EE AD1 [0]
Device 2 Info	7	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	8	EE AD2 [7]	EE AD2 [6]	EE AD2 [5]	EE AD2 [4]	EE AD2 [3]	EE AD2 [2]	EE AD2 [1]	EE AD2 [0]
Device 3 Info	9	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	10	EE AD3 [7]	EE AD3 [6]	EE AD3 [5]	EE AD3 [4]	EE AD3 [3]	EE AD3 [2]	EE AD3 [1]	EE AD3 [0]
Device 0 Addr 3	11	RES	RES	RES	RES	RES	Sel_LOS	RES	RES
Device 0 Addr 4	12	Ovrd_LOS	LOS_Value	PWDN Inp	PWDN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 0 Addr 38	46	RES	RES	RES	RES	RES	RES	RES	RES
Device 0 Addr 39	47	RES	RES	RES	RES	RES	RES	RES	RES
Device 1 Addr 3	48	RES	RES	RES	RES	RES	Sel_LOS	RES	RES
Device 1 Addr 4	49	Ovrd_LOS	LOS_Value	PWDN Inp	PWDN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 1 Addr 38	83	RES	RES	RES	RES	RES	RES	RES	RES
Device 1 Addr 39	84	RES	RES	RES	RES	RES	RES	RES	RES
Device 2 Addr 3	85	RES	RES	RES	RES	RES	Sel_LOS	RES	RES
Device 2 Addr 4	86	Ovrd_LOS	LOS_Value	PWDN Inp	PWDN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS

(1) (a) CRC EN = 1; Address Map = 1
(b) EEPROM > 256 Bytes = 0
(c) COUNT[3:0] = 0011'b
(d) Note: Multiple DS100BR111 devices may point at the same address space if they have identical programming values.

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Table 7. Multi-Device EEPROM Address Map Overview[1] (continued)

	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device 2 Addr 38	120	RES	RES	RES	RES	RES	RES	RES	RES
Device 2 Addr 39	121	RES	RES	RES	RES	RES	RES	RES	RES
Device 3 Addr 3	122	RES	RES	RES	RES	RES	Sel_LOS	RES	RES
Device 3 Addr 4	123	Ovrd_LOS	LOS_Value	PWDN Inp	PWDN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 3 Addr 38	157	RES	RES	RES	RES	RES	RES	RES	RES
Device 3 Addr 39	158	RES	RES	RES	RES	RES	RES	RES	RES

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Table 8. Multi DS100BR111 EEPROM Data

EEPROM ADDRESS	ADDRESS (HEX)	EEPROM DATA	COMMENTS
0	00	0x43	CRC_EN = 0, Address Map = 1, Device Count = 3 (Devices 0, 1, 2, and 3)
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x30	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x0B	Device 3 Address Location
11	0B	0x00	Begin Device 0 and Device 3 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x2F	Default EQ CHA
17	11	0xED	
18	12	0x40	
19	13	0x02	Default EQ CHB
20	14	0xFE	Default EQ CHB
21	15	0xD4	
22	16	0x00	
23	17	0x2F	
24	18	0xAD	
25	19	0x40	
26	1A	0x02	BR111 CHA VOD = 700 mVpp
27	1B	0xFA	
28	1C	0xD4	
29	1D	0x00	
30	1E	0x00	
31	1F	0x5F	
32	20	0x5A	BR111 CHB VOD = 1000 mVpp
33	21	0x80	
34	22	0x05	
35	23	0xF5	
36	24	0xA8	
37	25	0x00	
38	26	0x5F	
39	27	0x5A	
40	28	0x80	
41	29	0x05	
42	2A	0xF5	
43	2B	0xA8	
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

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Table 8. Multi DS100BR111 EEPROM Data (continued)

EEPROM ADDRESS	ADDRESS (HEX)	EEPROM DATA	COMMENTS
47	2F	0x54	End Device 0 and Device 3 - Address Offset 39
48	30	0x00	Begin Device 1 and Device 2 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x2F	Default EQ CHA
54	36	0xED	
55	37	0x40	
56	38	0x02	Default EQ CHB
57	39	0xFE	Default EQ CHB
58	3A	0xD4	
59	3B	0x00	
60	3C	0x2F	
61	3D	0xAD	
62	3E	0x40	
63	3F	0x02	BR111 CHA VOD = 700 mVpp
64	40	0xFA	
65	41	0xD4	
66	42	0x00	
67	43	0x00	
68	44	0x5F	
69	45	0x5A	BR111 CHB VOD = 1000 mVpp
70	46	0x80	
71	47	0x05	
72	48	0xF5	
73	49	0xA8	
74	4A	0x00	
75	4B	0x5F	
76	4C	0x5A	
77	4D	0x80	
78	4E	0x05	
79	4F	0xF5	
80	50	0xA8	
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 1 and Device 2 - Address Offset 39

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8.6 Register Maps

Table 9. SMBus Slave Mode Register Map

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x00	Device ID	7	Reserved	R/W	0x00		Set bit to 0
		6:3	SMBus Address [3:0]	R			SMBus strap observation
		2	EEPROM Reading Done	R			1 = EEPROM Done Loading 0 = EEPROM Loading
		1:0	Reserved	RWSC			Set bits to 0
0x01	Control 1	7:6	Idle Control	R/W	0x00	Yes	Continuous Talk Control (Output Always On) [7]: Continuous talk ENABLE (Channel A) [6]: Continuous talk ENABLE (Channel B)
		5:3	Reserved				Set bits to 0
		2	LOS Select				LOS Monitor Selection 1 = Use LOS from CH B 0 = Use LOS from CH A
		1:0	Reserved				Set bits to 0
0x02	Control 2	7:6	Reserved	R/W	0x00		Set bits to 0
		5	LOS override			Yes	1 = LOS pin override enable 0 = Use Normal Signal Detection
		4	LOS override value			Yes	1 = Normal Operation 0 = Output LOS
		3	PWDN Inputs			Yes	1 = PWDN 0 = Normal Operation
		2	PWDN Oscillator			Yes	
		1	Reserved				Set bit to 0
		0	Reserved			Yes	Set bit to 0
0x03	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x04	Control 3	7:6	eSATA Mode Enable	R/W	0x00	Yes	[7] Channel A (1) [6] Channel B (1)
		5	TX_DIS Override Enable				1 = Override Use Reg 0x04[4:3] 0 = Normal Operation - uses pin
		4	TX_DIS Value Channel A				1 = Channel A TX Disabled 0 = Channel A TX Enabled
		3	TX_DIS Value Channel B				1 = Channel B TX Disabled 0 = Channel B TX Enabled
		2	Reserved				Set bit to 0
		1:0	EQ Stage 4 Limiting Control				[1]: Channel B - EQ Stage 4 Limiting On/Off [0]: Channel A - EQ Stage 4 Limiting On/Off Setting this control bit turns on added voltage gain compared to normal operating range. If the bits are set to 1 (On), the EQ will act as a limiting amplifier, resulting in reduction of overall linear gain characteristics. Turning these bits On is not recommended for 10G-KR applications.
0x05	Reserved	7:0	Reserved	R/W	0x00		Reserved

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Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x06	Slave Register Control	7	Disable EEPROM CFG	R/W	0x10		Disable Master Mode EEPROM Configuration
		6:5	Reserved				Set bits to 0
		4	Reserved			Yes	Set bit to 1
		3	Register Enable				1 = Enable SMBus Slave Mode Register Control 0 = Disable SMBus Slave Mode Register Control **Note: In order to change VOD, DEM, and EQ of the channels in slave mode, this bit must be set to 1.**
		2:1	Reserved				Set bits to 0
		0	Reserved				Set bit to 0
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Set bit to 0
		6	Reset Registers				1 = Self clearing reset for SMBus registers (register settings return to default values)
		5	Reset SMBus Master				1 = Self clearing reset to SMBus master state machine
		4:0	Reserved				Set bits to 0 0001'b
0x08	Pin Override	7	Reserved	R/W	0x00		Set bit to 0
		6	Override Idle Threshold			Yes	1 = Override by Channel - see Reg 0x13 and 0x19 0 = SD_TH pin control
		5	Reserved			Yes	Set bit to 0
		4	Override IDLE			Yes	1 = Force IDLE by Channel - see Reg 0x0E and 0x15 0 = Normal Operation
		3	Reserved			Yes	Set bit to 0 Note: For all applications operating > 8Gbps, users must set this bit to 1 and enable all channels manually.
		2	Override Output Mode				1 = Enable Output Mode control for individual outputs. See register locations 0x10[6] and 0x17[6]. 0 = Disable - Outputs are kept in the normal mode of operation allowing VOD and DE adjustments.
		1	Override DEM			Yes	Override De-emphasis (ignore rate)
		0	Reserved			Yes	Set bit to 0
0x09-0x0A	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x0B	Reserved	7	Reserved	R/W	0x70		Reserved
		6:0	Reserved			Yes	Reserved
0x0C	CH A Analog Override 1	7:0	Reserved	R/W	0x00		Set bits to 0x00
0x0D	CH A Reserved	7:0	Reserved	R/W	0x00		Set bits to 0x00.

Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x0E	CH A Idle Control	7:6	Reserved	R/W	0x00		Set bits to 0
		5	Idle Auto			Yes	1 = Allow IDLE Select control in bit 4 0 = Automatic IDLE detect (Must set 0x08[4] = 1 to override pin-select control)
		4	Idle Select			Yes	1 = Output is muted (electrical IDLE) 0 = Output is on (Must set 0x08[4] = 1 to override pin-select control)
		3:2	Reserved			Yes	Set bits to 0
		1:0	Reserved				Set bits to 0
0x0F	CH A EQ Setting	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Boost Default to 24 dB See Table 3 for Information
0x10	CH A Control 1	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Output Mode			Yes	1 = Normal operation 0 = 10G-KR operation
		5:3	Reserved			Yes	Set bits to 101'b
		2:0	Reserved			Yes	Set bits to 101'b
0x11	CH A Control 2	7:5	Reserved	R	0x82		Set bits to 100'b
		4:3	Reserved	R/W			Set bits to 0
		2:0	DEM [2:0]			Yes	De-Emphasis 000'b = -0.0 dB 001'b = -1.5 dB 010'b = -3.5 dB (Default) 011'b = -6.0 dB 100'b = -8.0 dB 101'b = -9.0 dB 110'b = -10.5 dB 111'b = -12.0 dB
0x12	CH A Idle Threshold	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	IDLE Assert Threshold[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00'b = 180 mVpp (Default) 01'b = 160 mVpp 10'b = 210 mVpp 11'b = 190 mVpp
		1:0	IDLE De-assert Threshold[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00'b = 110 mVpp (Default) 01'b = 100 mVpp 10'b = 150 mVpp 11'b = 130 mVpp
0x13	CH B Analog Override 1	7:0	Reserved	R/W	0x00		Set bits to 0x00
0x14	CH B Reserved	7:0	Reserved	R/W	0x00		Set bits to 0x00

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Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x15	CH B Idle Control	7:6	Reserved	R/W	0x00		Set bits to 0
		5	Idle Auto			Yes	1 = Allow IDLE Select control in bit 4 0 = Automatic IDLE detect (Must set 0x08[4] = 1 to override pin-select control)
		4	Idle Select			Yes	1 = Output is muted (electrical IDLE) 0 = Output is on (Must set 0x08[4] = 1 to override pin-select control)
		3:2	Reserved			Yes	Set bits to 0
		1:0	Reserved				Set bits to 0
0x16	CH B EQ Setting	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Boost Default to 24 dB See Table 3 for Information
0x17	CH B Control 1	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Output Mode			Yes	1 = Normal operation 0 = 10G-KR operation
		5:3	Reserved			Yes	Set bits to 101'b
		2:0	Reserved			Yes	Set bits to 101'b
0x18	CH B Control 2	7:5	Reserved	R	0x82		Set bits to 100'b
		4:3	Reserved	R/W			Set bits to 0
		2:0	DEM [2:0]			Yes	De-Emphasis (Default = -3.5 dB) 000'b = -0.0 dB 001'b = -1.5 dB 010'b = -3.5 dB 011'b = -6.0 dB 100'b = -8.0 dB 101'b = -9.0 dB 110'b = -10.5 dB 111'b = -12.0 dB
0x19	CH B Idle Threshold	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	IDLE Assert Threshold[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00'b = 180 mVpp (Default) 01'b = 160 mVpp 10'b = 210 mVpp 11'b = 190 mVpp
		1:0	IDLE De-assert Threshold[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00'b = 110 mVpp (Default) 01'b = 100 mVpp 10'b = 150 mVpp 11'b = 130 mVpp
0x1A-0x1B	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x1C	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x1D	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x1E	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x1F	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved

Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x20	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x21-0x22	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x23	CH A VOD Control	7:6	Reserved	R/W	0x00		Set bits to 0
		5	Reserved			Yes	Set bit to 0
		4:2	VOD_CHA[2:0]			Yes	VOD Controls for CH A 000'b = 700 mVpp (Default) 001'b = 800 mVpp 010'b = 900 mVpp 011'b = 1000 mVpp 100'b = 1100 mVpp 101'b = 1200 mVpp 110'b = 1300 mVpp
		1:0	Reserved				Set bits to 0
0x24	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x25	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x26	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x27	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x28	Idle Control	7	Reserved	R/W	0x00		Set bit to 0
		6	Override Fast Idle			Yes	1 = Enable Fast IDLE control in Reg 0x28[3:2] 0 = Disable Fast IDLE control in Reg 0x28[3:2].
		5:4	en_hi_idle_th[1:0]			Yes	Enable high SD thresholds (Slow IDLE) [5]: CH A [4]: CH B
		3:2	en_fast_idle[1:0]			Yes	Enable Fast IDLE [3]: CH A [2]: CH B
		1:0	Reserved			Yes	Set bits to 0
0x29-0x2A	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x2B	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x2C	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x2D	CH B VOD Control	7:5	Reserved	R/W	0xAD	Yes	Set bits to 101'b
		4:2	VOD_CHB[2:0]			Yes	VOD Controls for CH B 000'b = 700 mVpp 001'b = 800 mVpp 010'b = 900 mVpp 011'b = 1000 mVpp (Default) 100'b = 1100 mVpp 101'b = 1200 mVpp 110'b = 1300 mVpp
		1:0	Reserved			Yes	Set bits to 01'b
0x2E	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved

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Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x2F	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x30-0x31	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x32	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x33	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x34	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x35	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x36	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x37-0x38	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x39	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x3A	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x3B	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x3C	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x3D	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x3E-0x3F	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x40	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x41	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x42	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x43	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x44	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x45	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x46	Reserved	7:0	Reserved	R/W	0x38		Reserved
0x47	Reserved	7:4	Reserved	R/W	0x00		Reserved
		3:0	Reserved			Yes	Reserved
0x48	Reserved	7:6	Reserved	R/W	0x05	Yes	Reserved
		5:0	Reserved				Reserved
0x49-0x4B	Reserved	7:0	Reserved	R/W	0x00		Reserved

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Register Maps (continued)

Table 9. SMBus Slave Mode Register Map (continued)

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x4C	Reserved	7:3	Reserved	R/W	0x00	Yes	Reserved
		2:1	Reserved				Reserved
		0	Reserved			Yes	Reserved
0x4D-0x50	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x51	Device Information	7:5	Version	R	0x67		011'b
		4:0	Device ID				0 0111'b
0x52-0x55	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x56	Reserved	7:0	Reserved	R/W	0x02		Reserved
0x57	Reserved	7:0	Reserved	R/W	0x14		Reserved
0x58	Reserved	7:0	Reserved	R/W	0x21		Reserved
0x59	Reserved	7:1	Reserved	R/W	0x00		Reserved
		0	Reserved			Yes	Reserved
0x5A	Reserved	7:0	Reserved	R/W	0x54	Yes	Reserved
0x5B	Reserved	7:0	Reserved	R/W	0x54	Yes	Reserved
0x5C-0x61	Reserved	7:0	Reserved	R/W	0x00		Reserved

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Signal Integrity in 10G-KR Applications

When configured in "KR Mode", using either the VOD_SEL and MODE pin setting or SMBus register control, the DS100BR111 is designed to operate transparently within a KR backplane channel environment. Installing a DS100BR111 repeater within the KR backplane channel splits the total channel attenuation into two parts. In other words, operating in "KR Mode" implies that signals will pass through the repeater with a linearized output. Ideally the repeater can be placed near the middle of the channel, maximizing the signal-to-noise ratio across the bidirectional interface.

In order to maximize the 10G-KR solution space, the 802.3ap specification calls for an optimization of the Tx partner signal conditioning coefficients based on feedback from the KR Rx ASIC endpoint. This link optimization sequence is commonly referred to as "link training" and is performed at speed (10.3125 Gbps). Setting the DS100BR111 active CTLE to compensate for the channel loss from each of the KR transmitters will reduce the transmit and receive equalization settings required on the KR physical layer devices. This central location keeps a larger signal-to-noise ratio at all points in the channel, extending the available solution space and increasing the overall margin of almost any channel. Suggested initial settings for the DS100BR111 are given in Table 10 and Table 11. Further adjustments to EQx, DEMx, and VODx settings may optimize signal margin on the link for different system applications.

Table 10. Suggested 10G-KR Initial Device Settings in Pin Mode(1)

CHANNEL SETTINGS	PIN MODE
EQx[1:0]	0, 0
VOD_SEL	1
DEMx	0

(1) For 10G-KR mode with slow idle-to-active response, the MODE pin should be left floating.

Table 11. Suggested 10G-KR Initial Device Settings in SMBus Modes

CHANNEL SETTINGS	SMBus MODES
EQx	0x00
VODx	100'b
DEMx	000'b

The SMBus Slave Mode code example in Table 12 may be used to program the DS100BR111 with the recommended device settings.

Table 12. SMBus 10G-KR Example Sequence

REGISTER	WRITE VALUE	COMMENTS
0x06	0x18	Set SMBus Slave Mode Register Enable.
0x08	0x04	Enable Output Mode Control for individual channel outputs.
0x0F	0x00	Set CHA EQ to 0x00.
0x10	0xAD	Set CHA Output Mode to Linear (10G-KR mode). If link-training is not required, set Reg 0x10 to 0xED.
0x11	0x00	Set CHA DEM to 000'b.
0x16	0x00	Set CHB EQ to 0x00.

Table 12. SMBus 10G-KR Example Sequence (continued)

REGISTER	WRITE VALUE	COMMENTS
0x17	0xAD	Set CHB Output Mode to Linear (10G-KR mode). If link-training is not required, set Reg 0x18 to 0xED.
0x18	0x00	Set CHB DEM to 000'b.
0x23	0x10	Set CHA VOD to 100'b.
0x28	0x00	Leave Idle Control at default levels. For SAS/SATA applications, set Reg 0x28 to 0x4C.
0x2D	0xB1	Set CHB VOD to 100'b.

9.1.2 OOB (Out-of-Band) Functionality in SAS/SATA Applications

For SAS/SATA systems, a low speed OOB (Out-of-Band) communication sequence is used to detect and communicate device capabilities between host ASIC and link partners. These OOB signals, including COMWAKE, COMINIT, COMRESET, and COMSAS, are a series of burst, idle, and negation times transmitted and detected across the SAS/SATA link. These bursts occur at a rapid rate, with the COMWAKE signal having the most stringent requirement of 106.6 ns active followed by 106.6 ns idle. Normally, if the device is set in 10G-KR mode (MODE pin floating), the device goes idle-to-active in approximately 150 ns. If the device is set to SAS mode (MODE pin tied via 1 kΩ to VDD (2.5 V mode) or VIN (3.3 V mode)), the device goes idle-to-active in approximately 3 to 4 ns. This fast idle-to-active time is critical to pass OOB signaling, and when operating in pin mode, the MODE pin should be tied high. If operating in SMBus slave mode, the user can set Reg 0x28 to 0x4C for this faster idle-to-active response.

9.2 Typical Application

The DS100BR111 works to extend the reach possible by using active equalization on the channel, boosting attenuated signals so that they can be more easily recovered at the Rx endpoint. The capability of the repeater can be explored across a range of data rates and ASIC-to-link-partner signaling, as shown in the following test setup connections. Figure 10 through Figure 12 represent typical generic application scenarios for the DS100BR111.

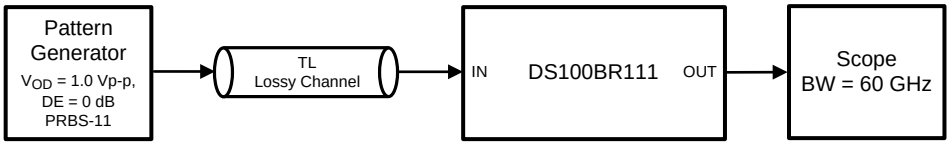

Figure 10. Test Setup Connections Diagram Pre-Channel Only

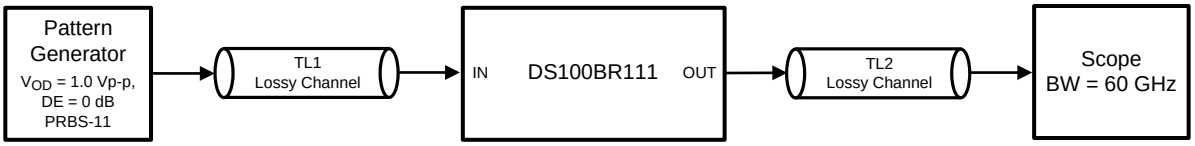

Figure 11. Test Setup Connections Diagram Pre-Channel and Post-Channel, No Tx Source De-emphasis

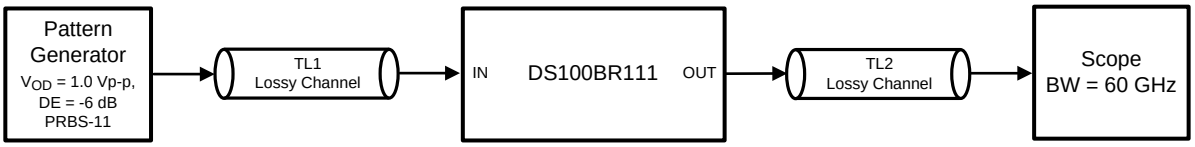

Figure 12. Test Setup Connections Diagram Pre-Channel and Post-Channel, -6 dB Tx Source De-emphasis

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Typical Application (continued)

9.2.1 Design Requirements

As with any high speed design, there are many factors that influence the overall performance. Below are a list of critical areas for consideration during design.

- Use 100 Ω impedance traces. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

9.2.2 Detailed Design Procedure

The DS100BR111 is designed to be placed at an offset location with respect to the overall channel attenuation. In order to optimize performance, the repeater requires optimization to extend the reach of the cable or trace length while also recovering a solid eye opening. To optimize the repeater in a 10G-KR environment, the settings mentioned in Table 10 (for Pin Mode) and Table 11 (for SMBus Modes) are recommended as a default starting point. For a generic 10GbE application where link training is not required, the following settings in Table 13 and Table 14 may be referenced as an initial starting point:

Table 13. Suggested Generic 10GbE Initial Device Settings in Pin Mode (1)

CHANNEL SETTINGS	PIN MODE
EQx[1:0]	0, 0
VOD_SEL	0
DEMx	0

(1) For 10GbE applications, the MODE pin should be tied high.

Table 14. Suggested Generic 10GbE Initial Device Settings in SMBus Modes

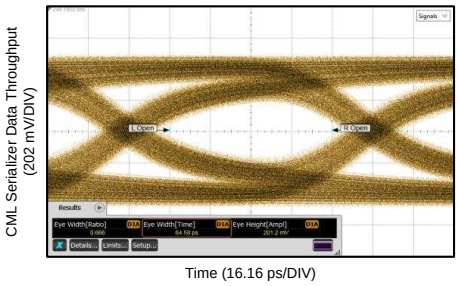
CHANNEL SETTINGS	SMBus MODES
EQx	0x00
VODx	000'b
DEMx	000'b

Examples of the repeater performance are illustrated in the performance curves in the next section.

9.2.3 Application Performance Plots

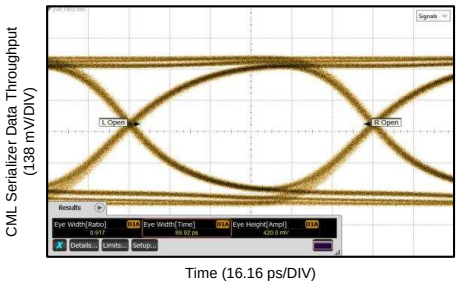
The lab setups referenced in Figure 10 to Figure 12 were used to collect typical performance data on FR4 and cable media. For all measurements, Mode Pin = Float.

9.2.3.1 Equalization Results (Pre-Channel Only)



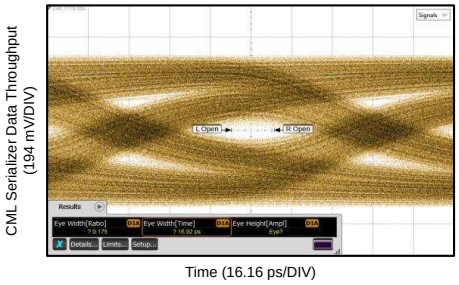
No Repeater Used

Figure 13. TL = 5 Inch 4–Mil FR4 Trace, No Repeater, 8 Gbps



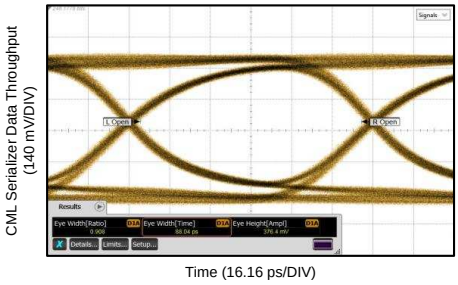
DS100BR111 Settings: EQA = 0x01, DEMA = 000'b, VOD = 000'b

Figure 14. TL = 5 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



No Repeater Used

Figure 15. TL = 10 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps

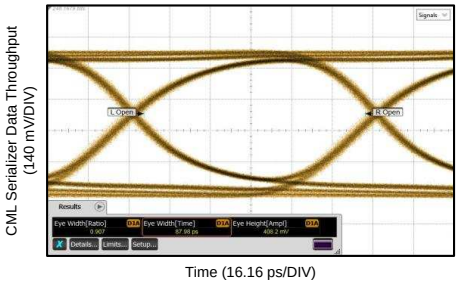


DS100BR111 Settings: EQA = 0x02, DEMA =000'b, VODA = 000'b

Figure 16. TL= 10 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps

No Repeater Used

Figure 17. TL = 15 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



DS100BR111 Settings: EQA = 0x03, DEMA = 000'b, VOD = 000'b

Figure 18. TL = 15 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps

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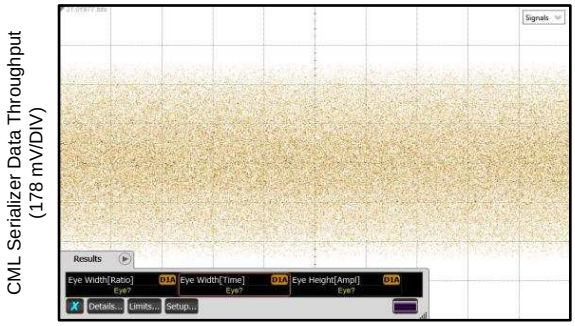
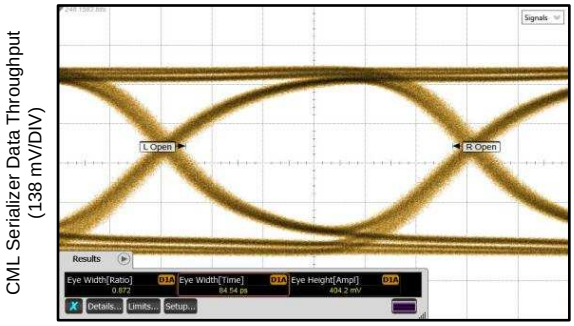


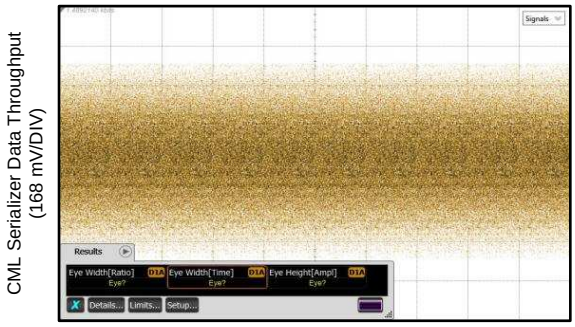
No Repeater Used

Figure 19. TL = 20 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



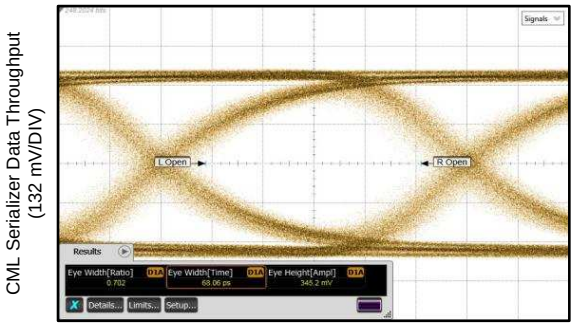
DS100BR111 Settings: EQA = 0x07, DEMA = 000'b, VOD = 000'b

Figure 20. TL = 20 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



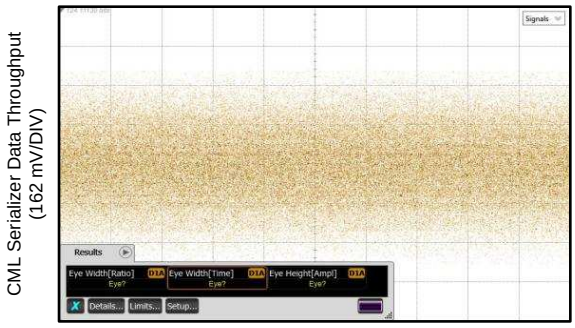
No Repeater Used

Figure 21. TL = 30 Inch 4–Mil FR4 Trace, No Repeater Used, 10.3125 Gbps



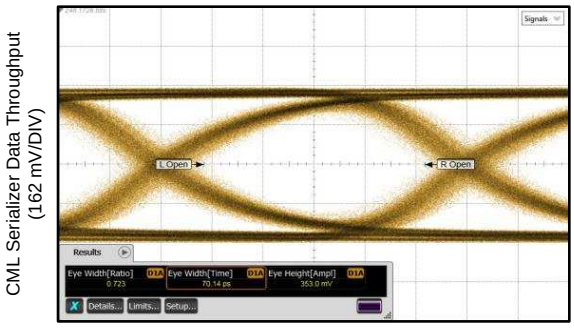
DS100BR111 Settings: EQA = 0x0F, DEMA = 000'b, VOD = 000'b

Figure 22. TL = 30 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



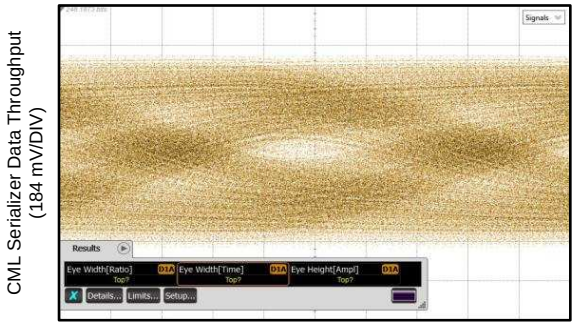
No Repeater Used

Figure 23. TL = 35 Inch 4–Mil FR4 Trace, No Repeater Used, 10.3125 Gbps



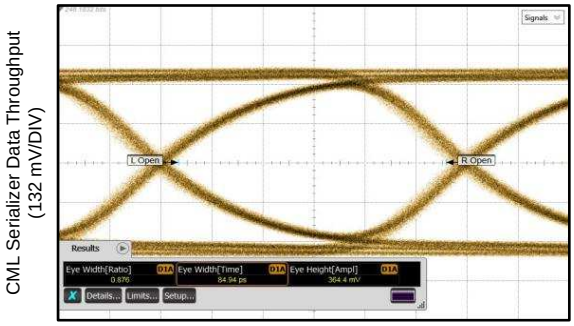
DS100BR111 Settings: EQA = 0x1F, DEMA = 000'b, VOD = 000'b

Figure 24. TL = 35 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



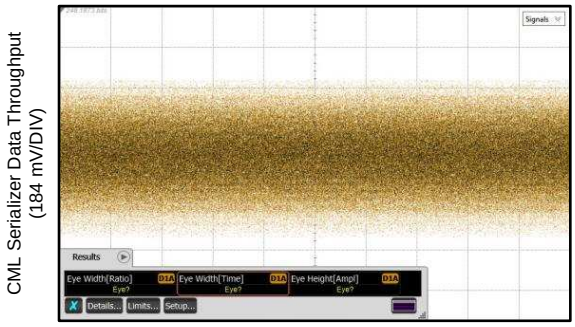
No Repeater Used

Figure 25. TL = 3-Meter 30-AWG 100 Ω Twin-Axial Cable, No Repeater, 10.3125 Gbps



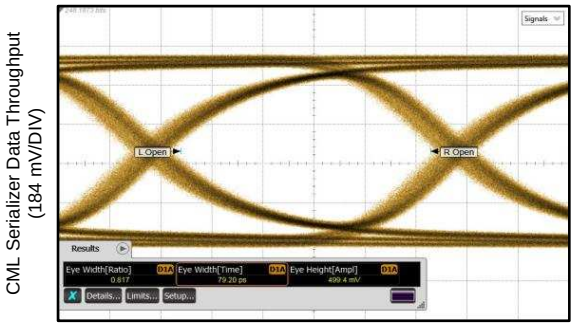
DS100BR111 Settings: EQA = 0x03, DEMA = 000'b, VODA = 000'b

Figure 26. TL = 3-Meter 30-AWG 100 Ω Twin-Axial Cable, DS100BR111 CHA, 10.3125 Gbps



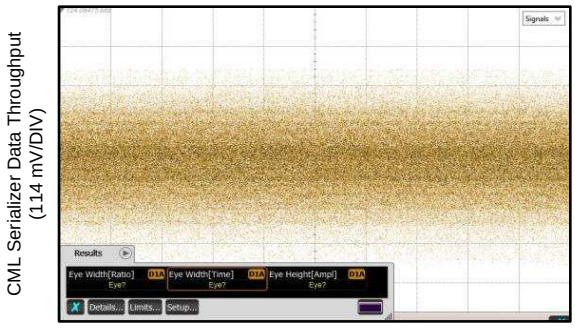
No Repeater Used

Figure 27. TL = 7-Meter 30-AWG 100 Ω Twin-Axial Cable, No Repeater, 10.3125 Gbps



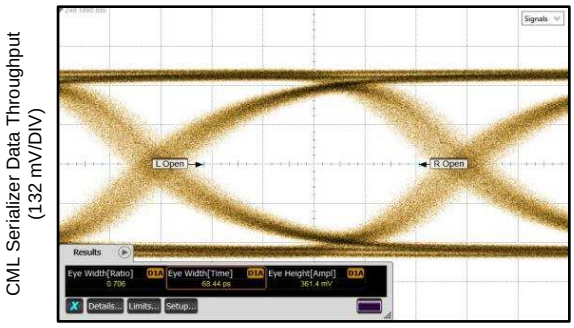
DS100BR111 Settings: EQA = 0x0F, DEMA = 000'b, VODA = 011'b

Figure 28. TL = 7-Meter 30-AWG 100 Ω Twin-Axial Cable, DS100BR111 CHA, 10.3125 Gbps



No Repeater Used

Figure 29. TL = 10-Meter 30-AWG 100 Ω Twin-Axial Cable, No Repeater, 10.3125 Gbps



DS100BR111 Settings: EQA = 0x2F, DEMA = 000'b, VODA = 000'b

Figure 30. TL = 10-Meter 30-AWG 100 Ω Twin-Axial Cable, DS100BR111 CHA, 10.3125 Gbps

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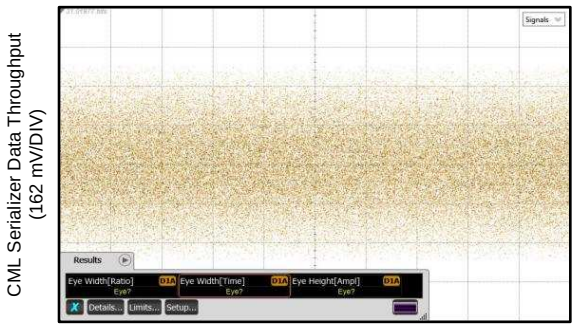
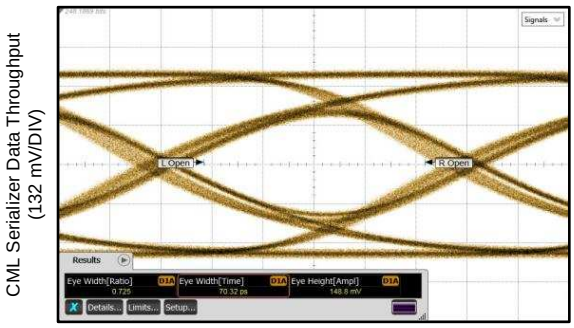
9.2.3.2 Equalization and De-Emphasis Results (Pre-channel and Post-channel, No Tx Source De-emphasis)



No Repeater Used

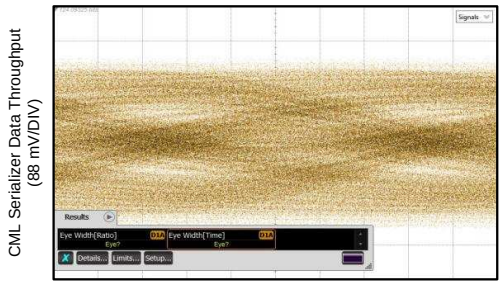
Figure 31. TL1 = 15 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



DS100BR111 Settings: EQA = 0x0B, DEMA = 010'b, VOD = 101'b

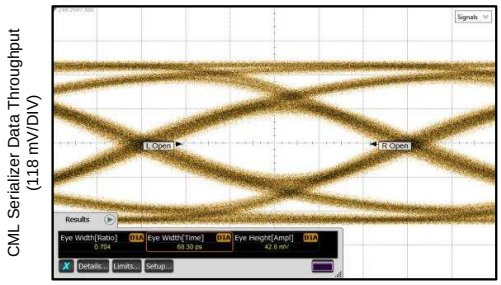
Figure 32. TL1 = 15 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps

9.2.3.3 Equalization and De-Emphasis Results (Pre-channel and Post-channel, -6 dB Tx Source De-emphasis)



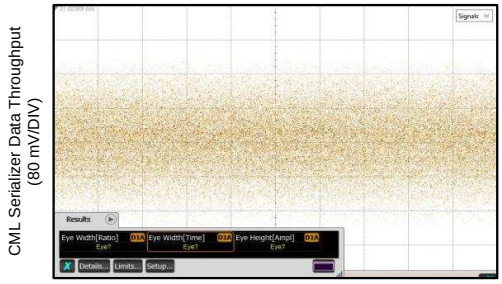
No Repeater Used

Figure 33. TL1 = 15 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



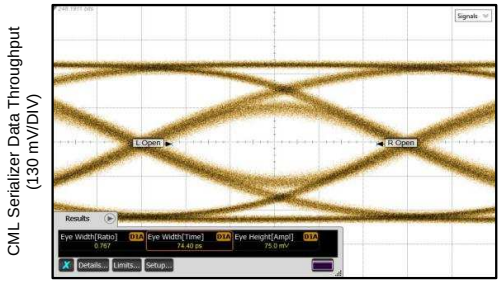
DS100BR111 Settings: EQA = 0x00, DEMA = 000'b, VOD = 011'b

Figure 34. TL1 = 15 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



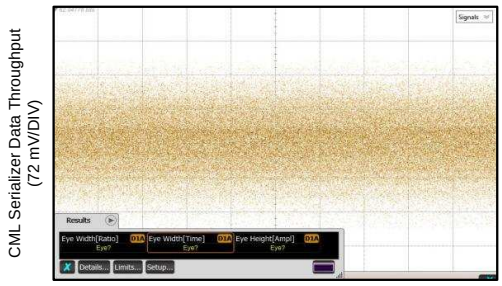
No Repeater Used

Figure 35. TL1 = 30 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



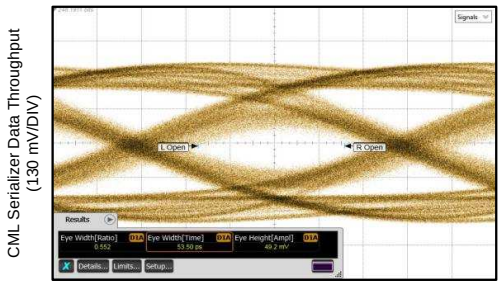
DS100BR111 Settings: EQA = 0x03, DEMA = 010'b, VOD = 101'b

Figure 36. TL1 = 30 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps



No Repeater Used

Figure 37. TL1 = 40 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, No Repeater, 10.3125 Gbps



DS100BR111 Settings: EQA = 0x03, DEMA = 100'b, VOD = 101'b

Figure 38. TL1 = 40 Inch 4–Mil FR4 Trace, TL2 = 10 Inch 4–Mil FR4 Trace, DS100BR111 CHA, 10.3125 Gbps

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10 Power Supply Recommendations

The DS100BR111 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3 V mode, the VIN pin = 3.3 V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1 µF cap is needed at each of the two VDD pins for power supply de-coupling (total capacitance should be ≤ 0.2 µF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5 V mode, the VIN pin should be left open and 2.5 V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

The DS100BR111 can be configured for 2.5 V operation or 3.3 V operation. The lists below outline required connections for each supply selection.

- **3.3 V Mode of Operation**
  - Tie VDD_SEL = GND.
  - Feed 3.3 V supply into VIN pin. Local 10 µF and 1 µF decoupling at VIN is recommended.
  - See information on VDD bypass in *Power Supply Bypass*.
  - SDA and SCL pins should connect pull-up resistor to VIN.
  - Any 4-Level input which requires a connection to "Logic 1" should use a 1 kΩ resistor to VIN.
- **2.5 V Mode of Operation**
  - VDD_SEL = Float
  - VIN = Float
  - Feed 2.5 V supply into VDD pins. Local 10 µF and 1 µF decoupling at VIN is recommended.
  - See information on VDD bypass in *Power Supply Bypass*.
  - SDA and SCL pins connect pull-up resistor to VDD for 2.5 V or 3.3 V microcontroller SMBus IO.
  - Any 4-Level input which requires a connection to "Logic 1" should use a 1 kΩ resistor to VDD.

NOTE

The DAP (bottom solder pad) is the GND connection.

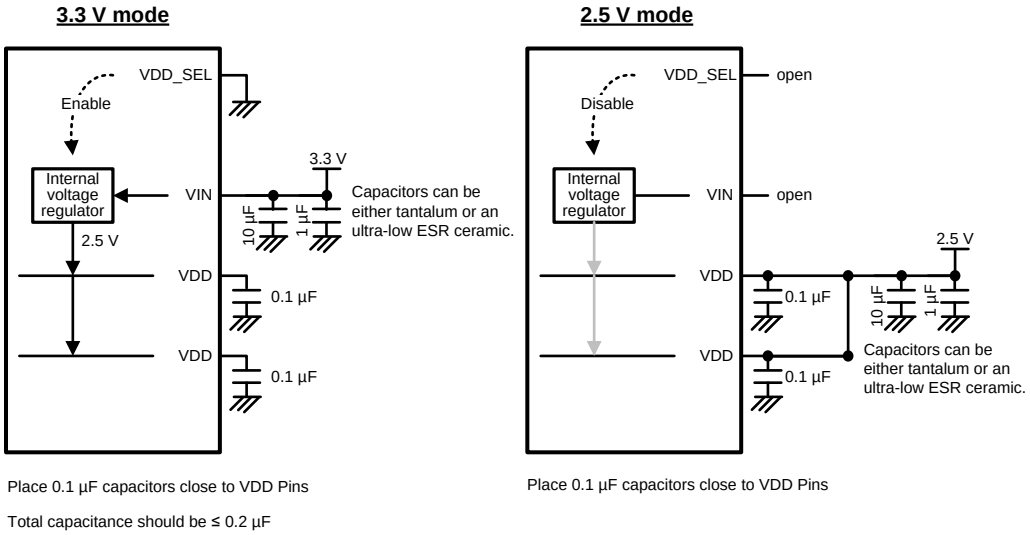

Figure 39. 3.3 V or 2.5 V Supply Connection Diagram

10.1 Power Supply Bypass

Two approaches are recommended to ensure that the DS100BR111 is provided with an adequate power supply bypass. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the device. Small body size capacitors (such as 0402) reduce the capacitors' parasitic inductance and also help in placement close to the VDD pin. If possible, the layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.

11 Layout

11.1 Layout Guidelines

The differential inputs and outputs are designed with 100 Ω differential terminations. Therefore, they should be connected to interconnects with controlled differential impedance of approximately 85-110 Ω. It is preferable to route differential lines primarily on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used, the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair spacing and trace width. See AN-1187 *"Leadless Leadframe Package (LLP) Application Report*" (literature number SNOA401) for additional information on QFN (WQFN) packages.

The DS100BR111 pinout promotes easy high speed routing and layout. To optimize DS100BR111 performance, refer to the following guidelines:

1. Place local VIN and VDD capacitors as close as possible to the device supply pins. Often the best location is directly under the DS100BR111 pins to reduce the inductance path to the capacitor. In addition, bypass capacitors may share a via with the DAP GND to minimize ground loop inductance.
2. Differential pairs going into or out of the DS100BR111 should have adequate pair-to-pair spacing to minimize crosstalk.
3. Use return current via connections to link reference planes locally. This ensures a low inductance return current path when the differential signal changes layers.
4. Optimize the via structure to minimize trace impedance mismatch.
5. Place GND vias around the DAP perimeter to ensure optimal electrical and thermal performance. A 2x2 or 3x3 array of GND vias for the DAP is recommended.
6. Use small body size AC coupling capacitors when possible — 0402 or smaller size is preferred. The AC coupling capacitors should be placed closer to the Rx on the channel.

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11.2 Layout Example

In most cases, DS100BR111 layouts will fit neatly into a 1-lane application. The example layout in Figure 40 shows the DS100BR111 channels in a typical 1-lane bidirectional layout.

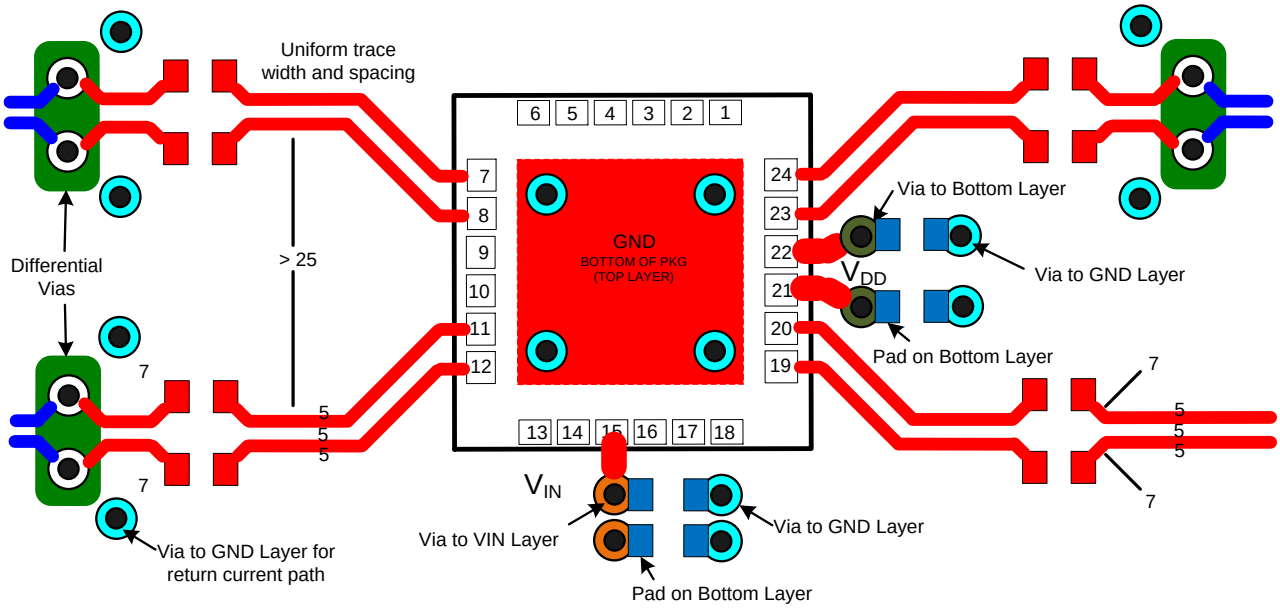

Figure 40. DS100BR111 Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549).
- *Leadless Leadframe Package (LLP) Application Report*, AN-1187 (SNOA401)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS100BR111SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	BR111	Samples
DS100BR111SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	BR111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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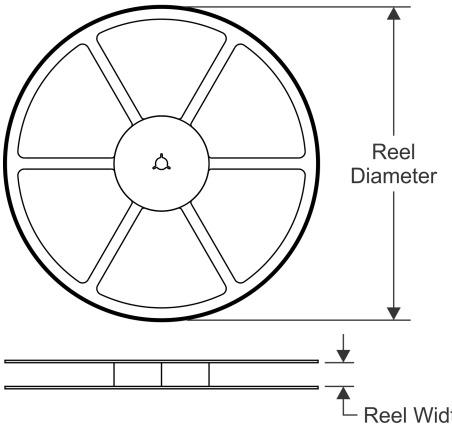
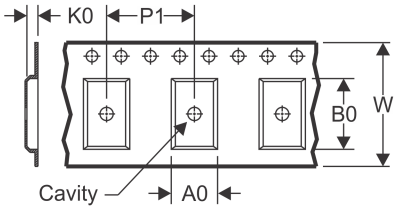
TAPE AND REEL INFORMATION

REEL DIMENSIONS

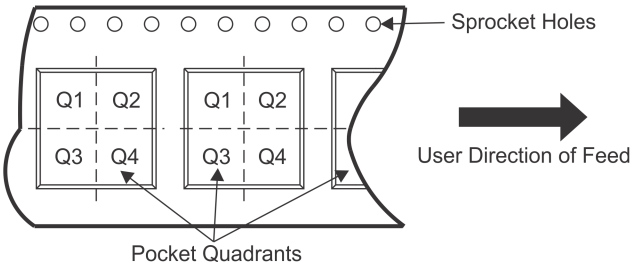


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

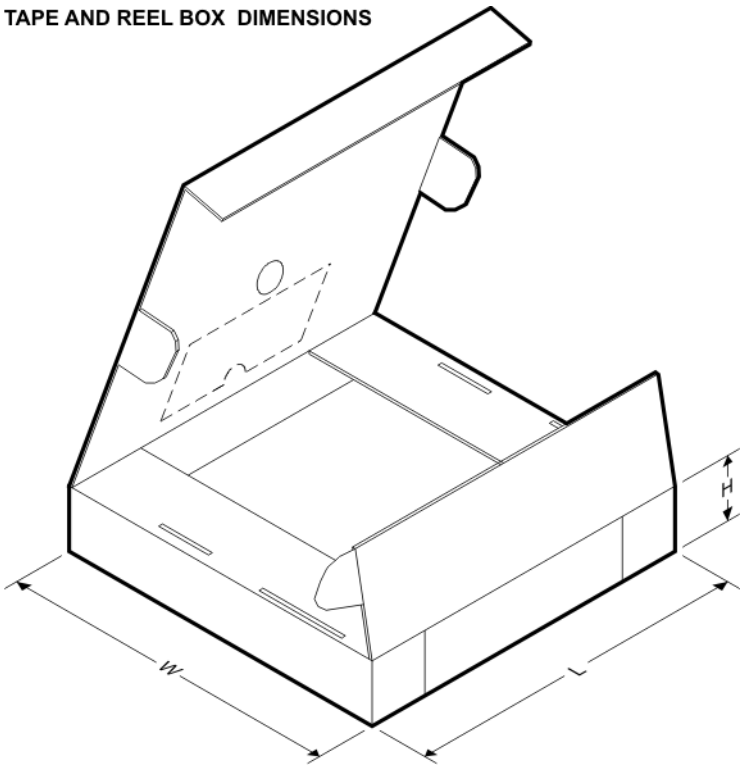
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

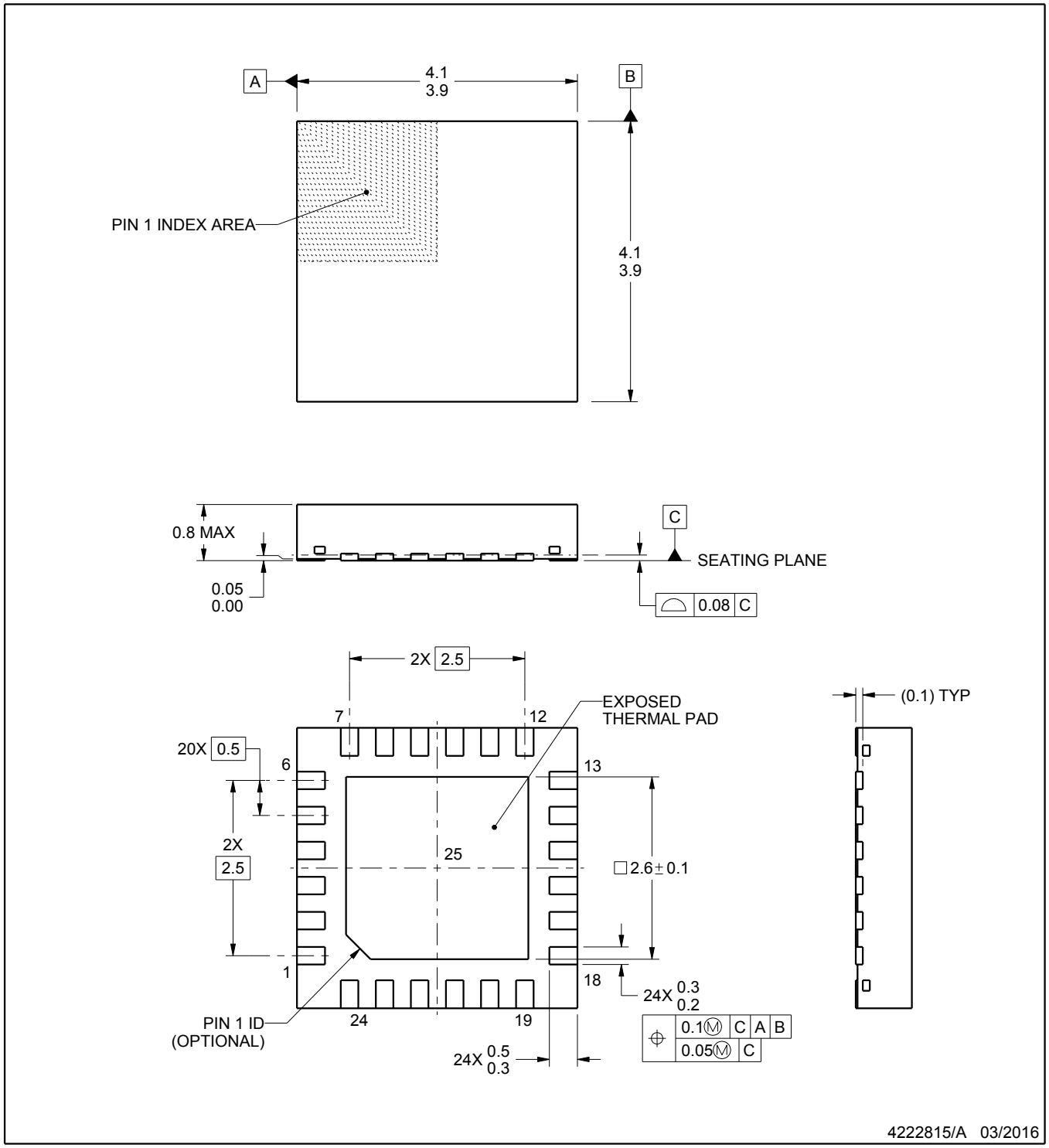
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100BR111SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS100BR111SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



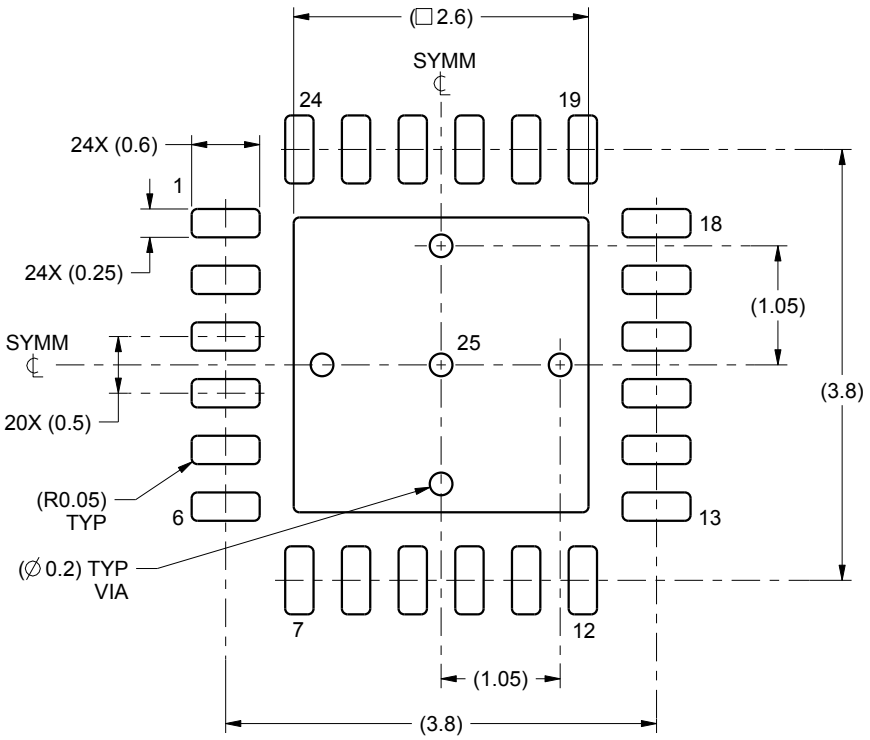
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100BR111SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
DS100BR111SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0

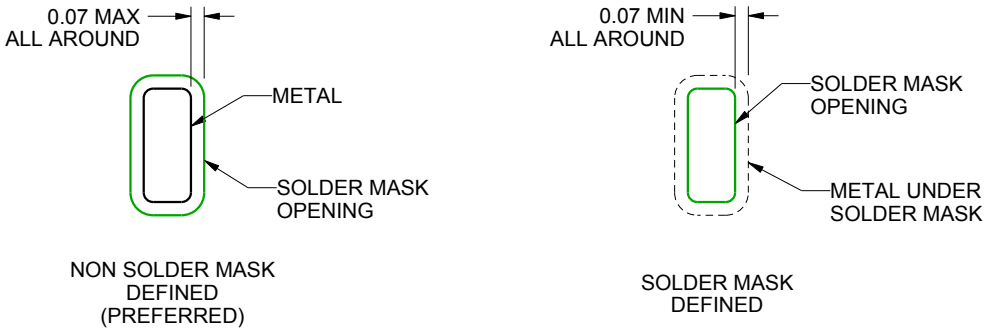


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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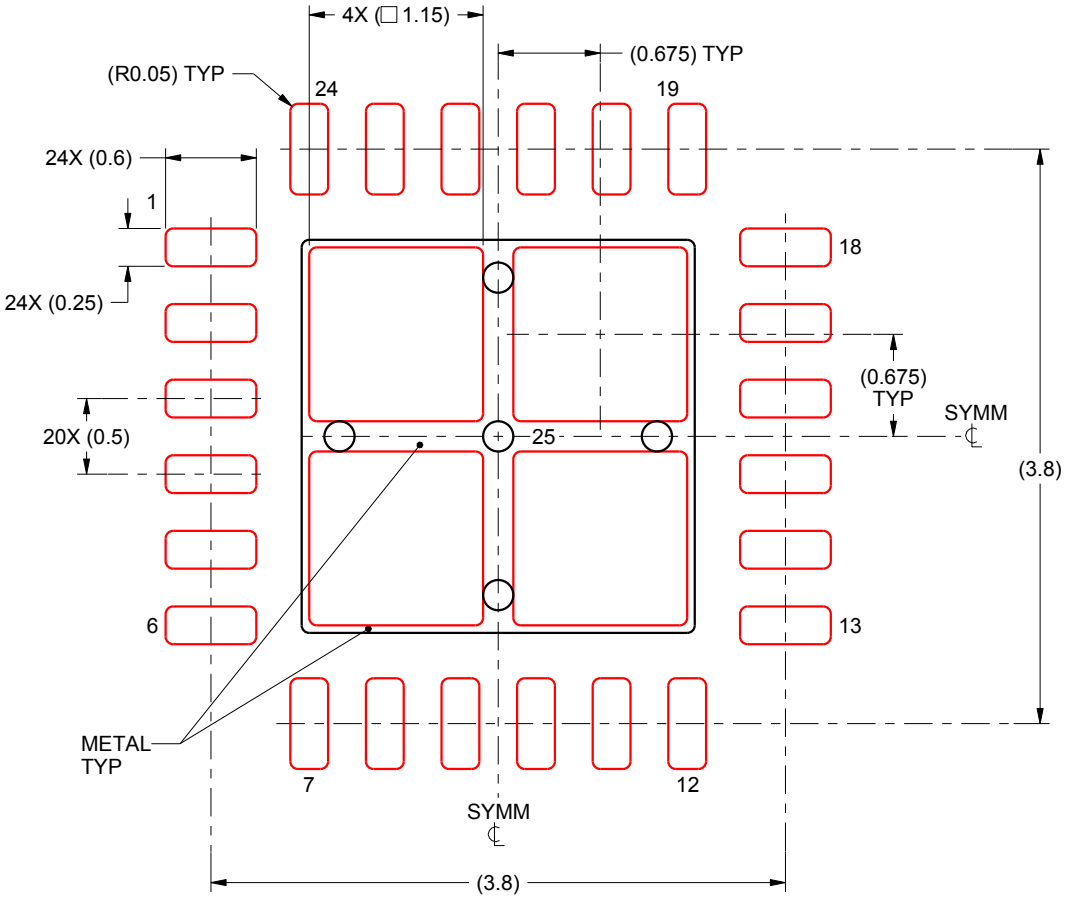
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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