

## SN74LVC4245A Octal Bus Transceiver and 3.3-V to 5-V Shifter With 3-State Outputs

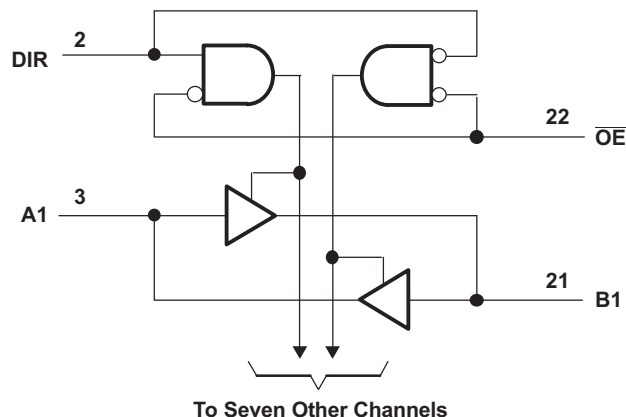
### 1 Features

- Bidirectional Voltage Translator
- 5.5 V on A Port and 2.7 V to 3.6 V on B Port
- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

### 2 Applications

- ATCA Solutions
- CPAP Machines
- Cameras: Surveillance Analog
- Chemical or Gas Sensors
- CT Scanners
- DLP 3D Machine Vision and Optical Networking
- Digital Signage
- ECGs: Electrocardiograms
- Field Transmitters: Pressure Sensors and Temperature Sensors
- High-Speed Data Acquisition and Generation
- HMI (Human Machine Interface)
- RF4CE Remote Controls
- Server Motherboards
- Software Defined Radios (SDR)
- Wireless LAN Cards and Data Access Cards
- X-ray: Medical, Dental, and Baggage Scanners

### 4 Simplified Schematic



### 3 Description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has  $V_{CCB}$ , which is set at 3.3 V, and A port has  $V_{CCA}$ , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

The SN74LVC4245A device terminal out allows the designer to switch to a normal all-3.3-V or all-5-V 20-terminal SN74LVC4245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A device to align with the conventional '245 terminal out.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC4245A	SSOP (24)	8.20 mm × 5.30 mm
	SOIC (24)	15.40 mm × 7.50 mm
	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 B Port .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>10</b>
<b>3 Description</b> .....	<b>1</b>	9.1 Overview .....	<b>10</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	<b>10</b>
<b>5 Revision History</b> .....	<b>2</b>	9.3 Feature Description .....	<b>10</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	9.4 Device Functional Modes .....	<b>10</b>
<b>7 Specifications</b> .....	<b>4</b>	<b>10 Application and Implementation</b> .....	<b>11</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	10.1 Application Information .....	<b>11</b>
7.2 Absolute Maximum Ratings .....	<b>4</b>	10.2 Typical Application .....	<b>11</b>
7.3 ESD Ratings .....	<b>4</b>	<b>11 Power Supply Recommendations</b> .....	<b>13</b>
7.4 Recommended Operating Conditions .....	<b>5</b>	11.1 Power-Up Consideration .....	<b>13</b>
7.5 Recommended Operating Conditions .....	<b>5</b>	<b>12 Layout</b> .....	<b>13</b>
7.6 Thermal Information .....	<b>5</b>	12.1 Layout Guidelines .....	<b>13</b>
7.7 Electrical Characteristics .....	<b>6</b>	12.2 Layout Example .....	<b>13</b>
7.8 Electrical Characteristics .....	<b>6</b>	<b>13 Device and Documentation Support</b> .....	<b>14</b>
7.9 Switching Characteristics .....	<b>7</b>	13.1 Trademarks .....	<b>14</b>
7.10 Operating Characteristics .....	<b>7</b>	13.2 Electrostatic Discharge Caution .....	<b>14</b>
7.11 Typical Characteristics .....	<b>7</b>	13.3 Glossary .....	<b>14</b>
<b>8 Parameter Measurement Information</b> .....	<b>8</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>14</b>
8.1 A Port .....	<b>8</b>		

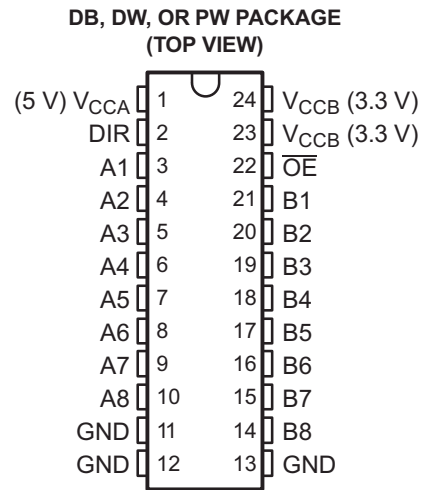
## 5 Revision History

### Changes from Revision H (March 2005) to Revision I

**Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**
- Deleted *Ordering Information* table. .... **1**

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$V_{CCA}$	—	Power supply for side A
2	DIR	I	Direction control
3	A1	I/O	Transceiver I/O pin
4	A2	I/O	Transceiver I/O pin
5	A3	I/O	Transceiver I/O pin
6	A4	I/O	Transceiver I/O pin
7	A5	I/O	Transceiver I/O pin
8	A6	I/O	Transceiver I/O pin
9	A7	I/O	Transceiver I/O pin
10	A8	I/O	Transceiver I/O pin
11	GND	—	Ground
12	GND	—	Ground
13	GND	—	Ground
14	B8	I/O	Transceiver I/O pin
15	B7	I/O	Transceiver I/O pin
16	B6	I/O	Transceiver I/O pin
17	B5	I/O	Transceiver I/O pin
18	B4	I/O	Transceiver I/O pin
19	B3	I/O	Transceiver I/O pin
20	B2	I/O	Transceiver I/O pin
21	B1	I/O	Transceiver I/O pin
22	$\overline{OE}$	I	Output Enable
23	$V_{CCB}$	—	Power supply for side B
24	$V_{CCB}$	—	Power supply for side B

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range for  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCA}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range	A port <sup>(2)</sup>	$V_{CCA} + 0.5$	V
		Control inputs	6	
$V_O$	Output voltage range	-0.5	$V_{CCA} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through each $V_{CCA}$ or GND		$\pm 100$	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 6 V maximum.

### 7.2 Absolute Maximum Ratings

over operating free-air temperature range for  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$  (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCB}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range	B port <sup>(2)</sup>	$V_{CCB} + 0.5$	V
		B port <sup>(2)</sup>	$V_{CCB} + 0.5$	
$V_O$	Output voltage range	-0.5	$V_{CCB} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CCB}$ or GND		$\pm 100$	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.

### 7.3 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.4 Recommended Operating Conditions

 for  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}^{(1)}$ 

		MIN	MAX	UNIT
$V_{CCA}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_{IA}$	Input voltage	0	$V_{CCA}$	V
$V_{OA}$	Output voltage	0	$V_{CCA}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 7.5 Recommended Operating Conditions

 for  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}^{(1)}$ 

			MIN	MAX	UNIT
$V_{CCB}$	Supply voltage		2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
$V_{IB}$	Input voltage		0	$V_{CCB}$	V
$V_{OB}$	Output voltage		0	$V_{CCB}$	V
$I_{OH}$	High-level output current	$V_{CCB} = 2.7\text{ V}$		-12	mA
		$V_{CCB} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CCB} = 2.7\text{ V}$		12	mA
		$V_{CCB} = 3\text{ V}$		24	
$T_A$	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 7.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC4245A			UNIT	
	DB	DW	PW		
	24 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	46	88	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.7 Electrical Characteristics

 over recommended operating free-air temperature range for  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	$V_{CCA}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$	4.5 V	4.3		V	
			5.5 V	5.3			
		$I_{OH} = -24\ \text{mA}$	4.5 V	3.7			
			5.5 V	4.7			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$	4.5 V	0.2		V	
			5.5 V	0.2			
		$I_{OL} = 24\ \text{mA}$	4.5 V	0.55			
			5.5 V	0.55			
$I_i$	Control inputs	$V_i = V_{CCA}$ or GND	5.5 V	$\pm 1$		$\mu\text{A}$	
$I_{OZ}$ <sup>(3)</sup>	A port	$V_O = V_{CCA}$ or GND	5.5 V	$\pm 5$		$\mu\text{A}$	
$I_{CCA}$		$V_i = V_{CCA}$ or GND, $I_O = 0$	5.5 V	80		$\mu\text{A}$	
$\Delta I_{CCA}$ <sup>(4)</sup>		One input at 3.4 V, Other inputs at $V_{CCA}$ or GND	5.5 V	1.5		mA	
$C_i$	Control inputs	$V_i = V_{CCA}$ or GND	Open	5		pF	
$C_{io}$	A port	$V_O = V_{CCA}$ or GND	5 V	11		pF	

 (1)  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$ .

 (2) All typical values are measured at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

 (3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

 (4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated  $V_{CC}$ .

## 7.8 Electrical Characteristics

 over recommended operating free-air temperature range for  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	$V_{CCB}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$	2.7 V to 3.6 V	$V_{CC} - 0.2$		V	
			2.7 V	2.2			
		$I_{OH} = -24\ \text{mA}$	3 V	2.4			
			3 V	2			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$	2.7 V to 3.6 V	0.2		V	
			2.7 V	0.4			
			3 V	0.55			
$I_{OZ}$ <sup>(3)</sup>	B port	$V_O = V_{CCB}$ or GND	3.6 V	$\pm 5$		$\mu\text{A}$	
$I_{CCB}$		$V_i = V_{CCB}$ or GND, $I_O = 0$	3.6 V	50		$\mu\text{A}$	
$\Delta I_{CCB}$ <sup>(4)</sup>		One input at $V_{CCB} - 0.6\text{ V}$ , Other inputs at $V_{CCB}$ or GND	2.7 V to 3.6 V	0.5		mA	
$C_{io}$	B port	$V_O = V_{CCB}$ or GND	3.3 V	11		pF	

 (1)  $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ .

 (2) All typical values are measured at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

 (3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

 (4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated  $V_{CC}$ .

### 7.9 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 3 and Figure 4)

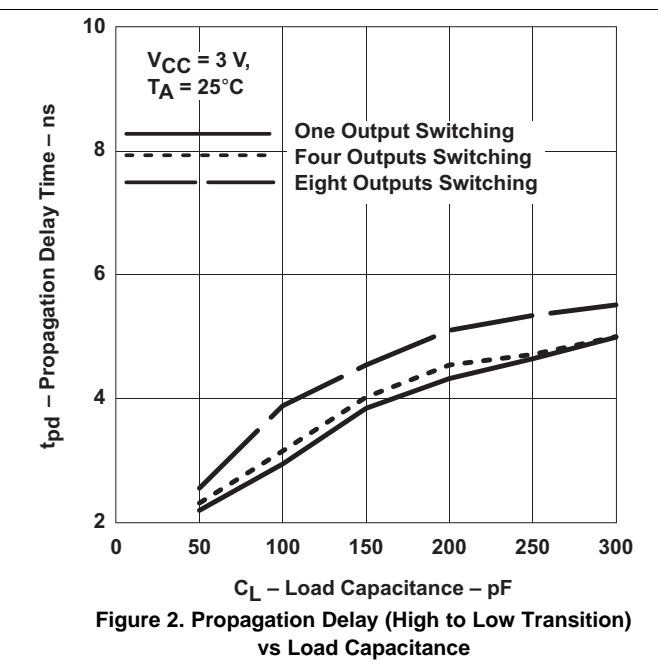
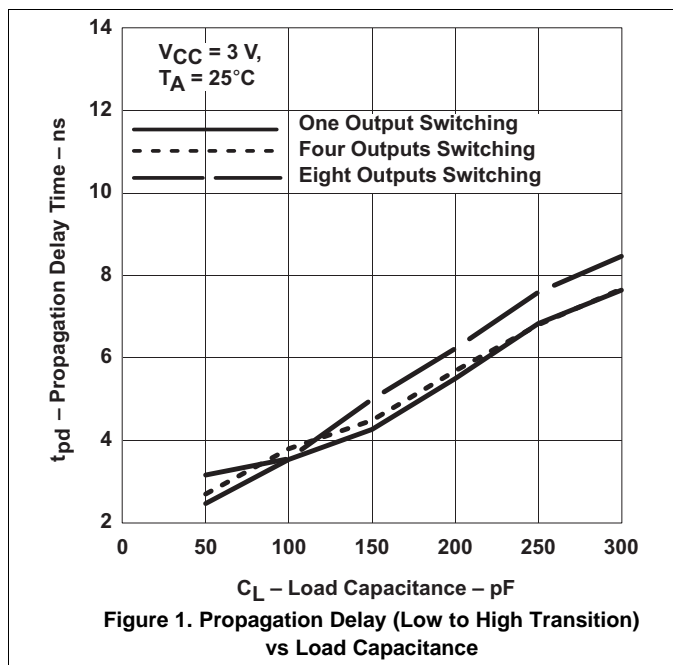
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5 V \pm 0.5 V$ , $V_{CCB} = 2.7 V$ to $3.6 V$		UNIT
			MIN	MAX	
$t_{PHL}$	A	B	1	6.3	ns
$t_{PLH}$			1	6.7	
$t_{PHL}$	B	A	1	6.1	ns
$t_{PLH}$			1	5	
$t_{PZL}$	$\overline{OE}$	A	1	9	ns
$t_{PZH}$			1	8.1	
$t_{PZL}$	$\overline{OE}$	B	1	8.8	ns
$t_{PZH}$			1	9.8	
$t_{PLZ}$	$\overline{OE}$	A	1	7	ns
$t_{PHZ}$			1	5.8	
$t_{PLZ}$	$\overline{OE}$	B	1	7.7	ns
$t_{PHZ}$			1	7.8	

### 7.10 Operating Characteristics

$V_{CCA} = 4.5 V$  to  $5.5 V$ ,  $V_{CCB} = 2.7 V$  to  $3.6 V$ ,  $T_A = 25^\circ C$

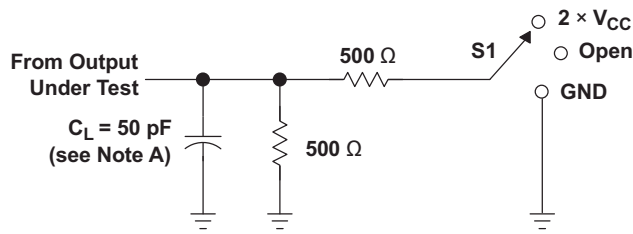
PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 0$ , $f = 10$ MHz	39.5	pF
		Outputs disabled		5	

### 7.11 Typical Characteristics



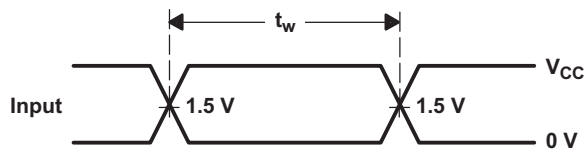
## 8 Parameter Measurement Information

### 8.1 A Port

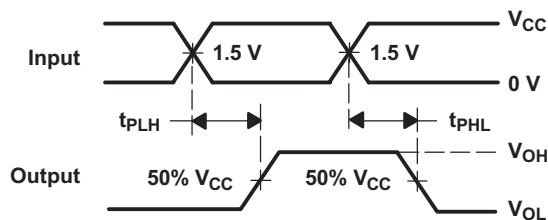


LOAD CIRCUIT

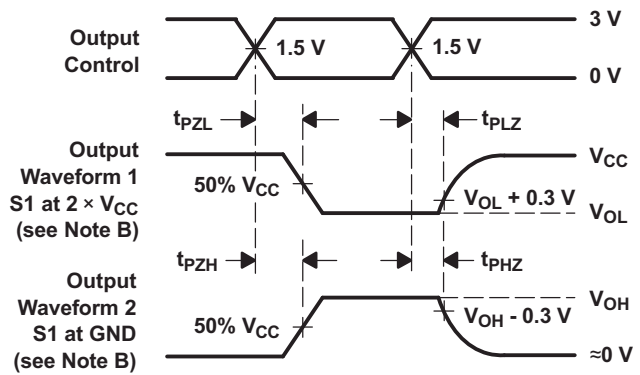
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS



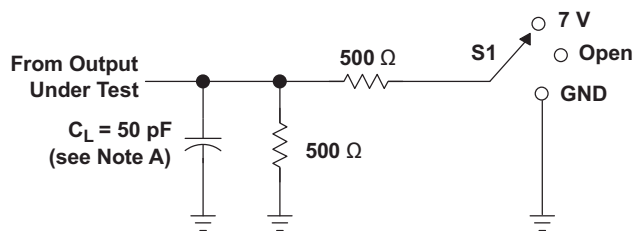
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

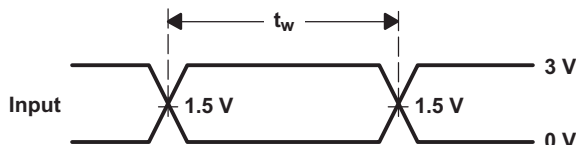


8.2 B Port

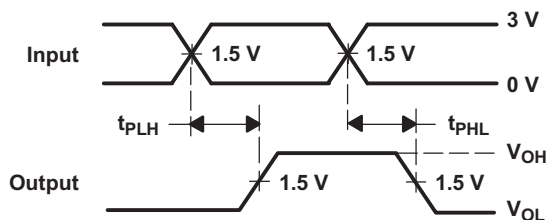


LOAD CIRCUIT

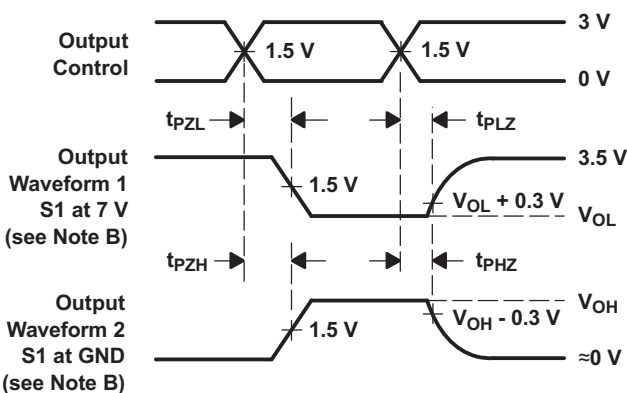
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

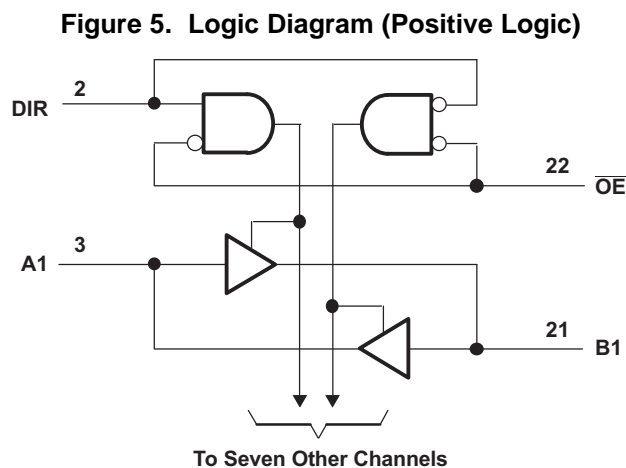
Figure 4. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

SN74LVC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has  $V_{CCB}$ , which is set at 3.3 V, and A port has  $V_{CCA}$ , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- 24 mA drive at 3-V supply
  - Good for heavier loads and longer traces
- Low  $V_{IH}$ 
  - Allows 3.3-V to 5-V translation

### 9.4 Device Functional Modes

**Function Table**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 10 Application and Implementation

### 10.1 Application Information

The SN74LVC4245A device pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional SN74LVC4245 device's pinout. SN74LVC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 10.2 Typical Application

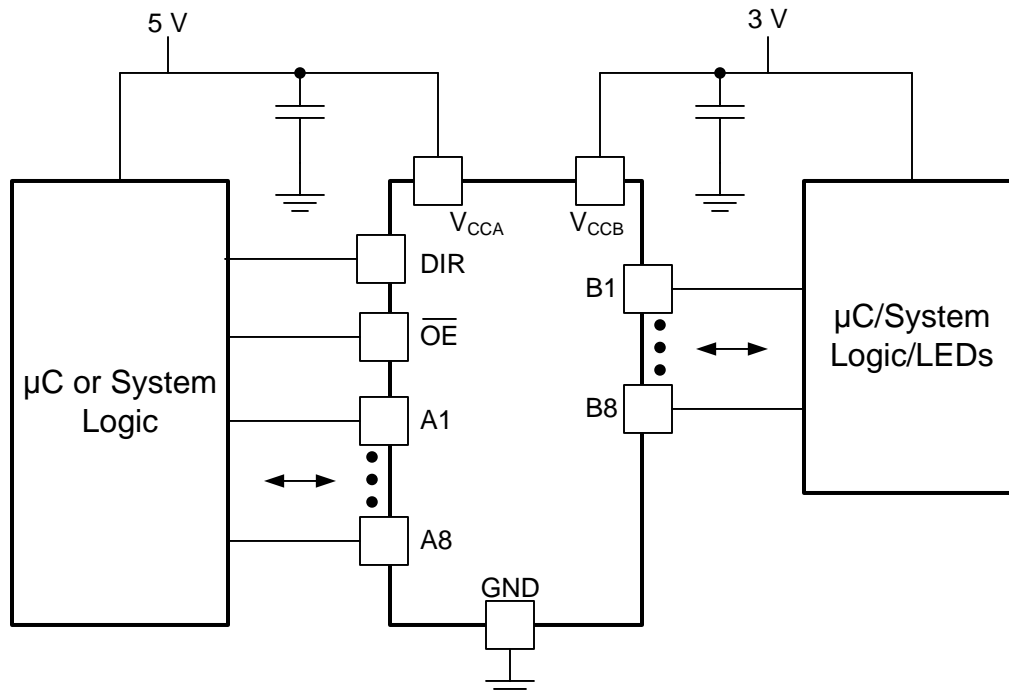


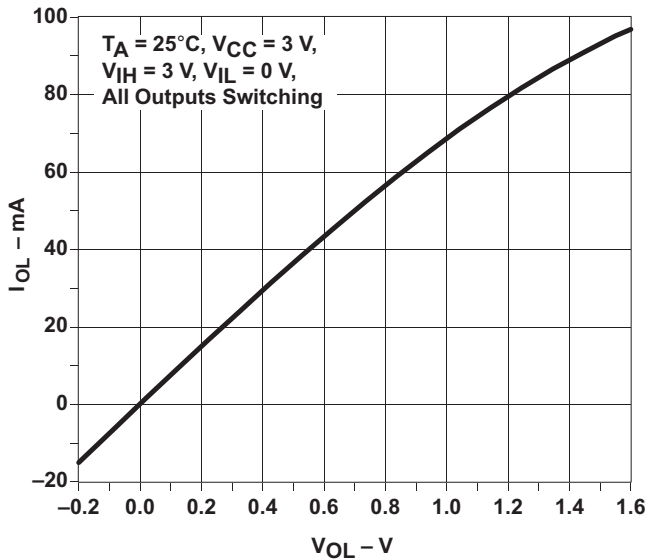
Figure 6. Typical Application Schematic

#### 10.2.1 Design Requirements

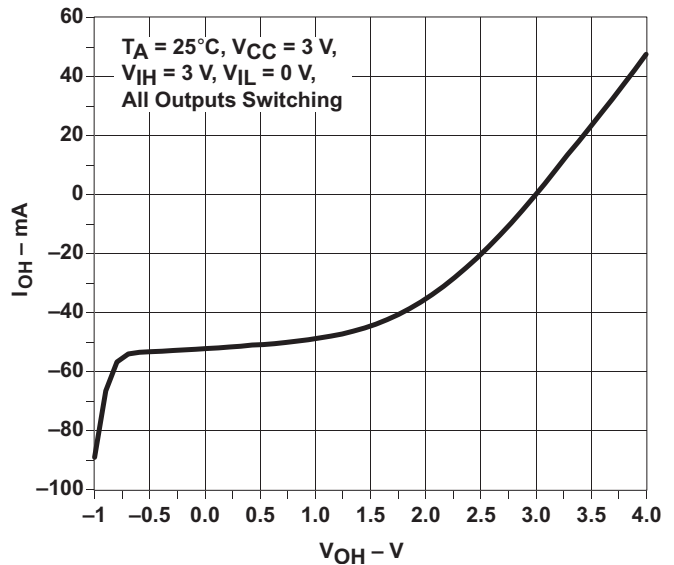
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
2. Recommend Output Conditions:
  - Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .
  - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

**Typical Application (continued)**
**10.2.3 Application Curves**


**Figure 7. Output Drive Current ( $I_{OL}$ ) vs LOW-level Output Voltage ( $V_{OL}$ )**



**Figure 8. Output Drive Current ( $I_{OH}$ ) vs HIGH-level Output Voltage ( $V_{OH}$ )**

## 11 Power Supply Recommendations

### 11.1 Power-Up Consideration

<sup>(1)</sup>TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number [SCEA021](#).

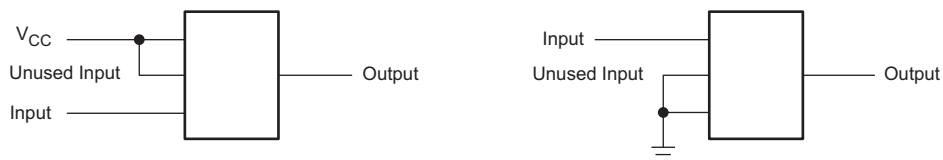
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 9](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 12.2 Layout Example



**Figure 9. Layout Diagram**

## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC4245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	<a href="#">Samples</a>
SN74LVC4245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>
SN74LVC4245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC4245A :**

- Enhanced Product: [SN74LVC4245A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVC4245ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVC4245ADWR	SOIC	DW	24	2000	364.0	361.0	36.0
SN74LVC4245ADWRG4	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVC4245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVC4245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R-PDSO-G24)

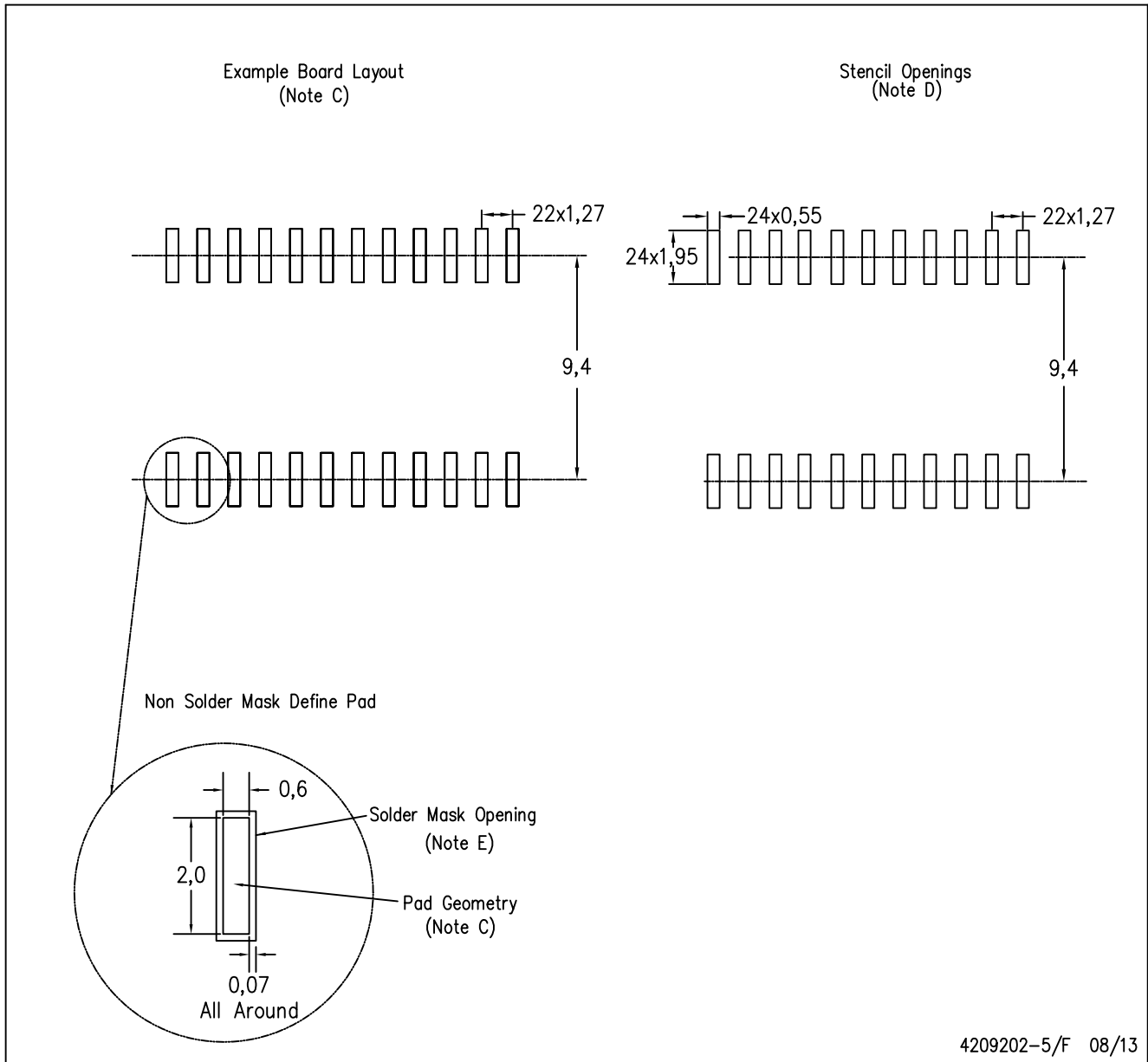
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

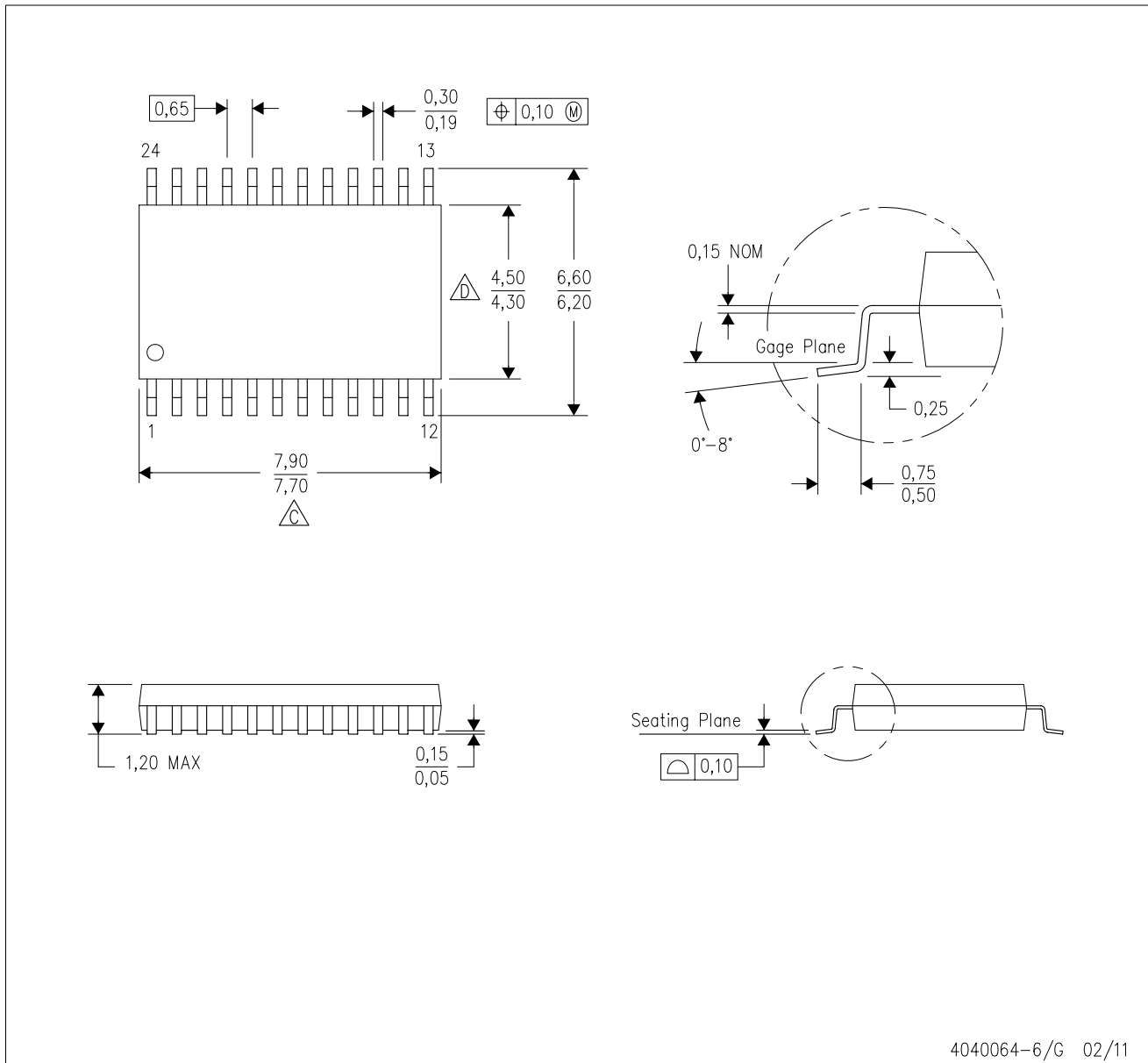


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\triangle$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - $\triangle$  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate design.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.