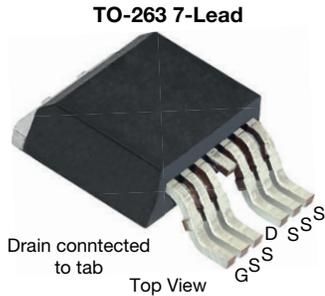


N-Channel 40 V (D-S) MOSFET



FEATURES

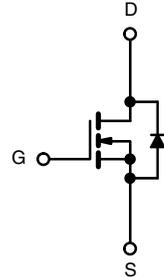
- TrenchFET® Gen IV power MOSFET
- Maximum 175 °C junction temperature
- 100 % R_G and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power supply
- Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing



N-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	40
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.00099
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.00136
Q _g typ. (nC)	182
I _D (A) ^d	200
Configuration	Single

ORDERING INFORMATION

Package	D ² PAK (TO-263-7L)
Lead (Pb)-free and halogen-free	SUM40014M-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	40	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	200 ^d
		T _C = 70 °C	200 ^d
Pulsed drain current (t = 100 μs)	I _{DM}	400	A
Avalanche current	I _{AS}	70	
Single avalanche energy ^a	E _{AS}	245	mJ
Maximum power dissipation ^a	P _D	T _C = 25 °C	375 ^b
		T _C = 125 °C	125 ^b
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) ^c	R _{thJA}	40	°C/W
Junction-to-case (drain)	R _{thJC}	0.4	

Notes

- Duty cycle ≤ 1 %
- See SOA curve for voltage derating
- When mounted on 1" square PCB (FR4 material)
- Package limited



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 10 mA	40	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.4	
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 250	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C	-	-	150	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 175 °C	-	-	5	mA
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	100	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00082	0.00099	Ω
		V _{GS} = 4.5 V, I _D = 15 A	-	0.00113	0.00136	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	-	140	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	-	15 780	-	pF
Output capacitance	C _{oss}		-	2280	-	
Reverse transfer capacitance	C _{rss}		-	90	-	
Total gate charge ^c	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A	-	182	275	nC
Gate-source charge ^c	Q _{gs}		-	41	-	
Gate-drain charge ^c	Q _{gd}		-	9	-	
Gate resistance	R _g	f = 1 MHz	0.5	2.4	4.8	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	20	40	ns
Rise time ^c	t _r		-	10	20	
Turn-off delay time ^c	t _{d(off)}		-	100	200	
Fall time ^c	t _f		-	35	70	
Drain-Source Body Diode Ratings and Characteristics ^b (T_C = 25 °C)						
Pulsed current (t = 100 μs)	I _{SM}		-	-	600	A
Forward voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V	-	0.72	1.5	V
Reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs	-	55	80	ns
Peak reverse recovery charge	I _{RM(REC)}		-	2.2	5	A
Reverse recovery charge	Q _{rr}		-	0.065	0.13	μC

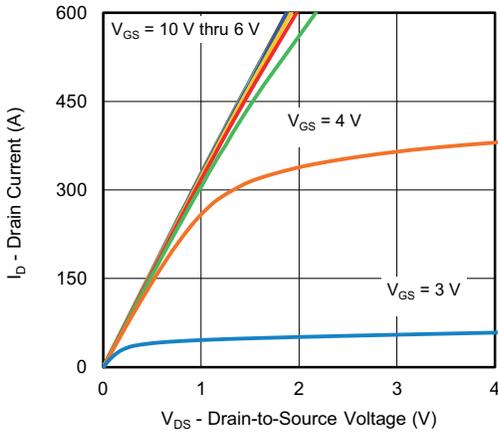
Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

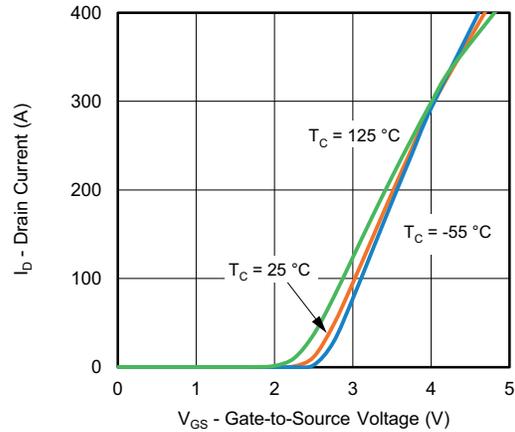
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



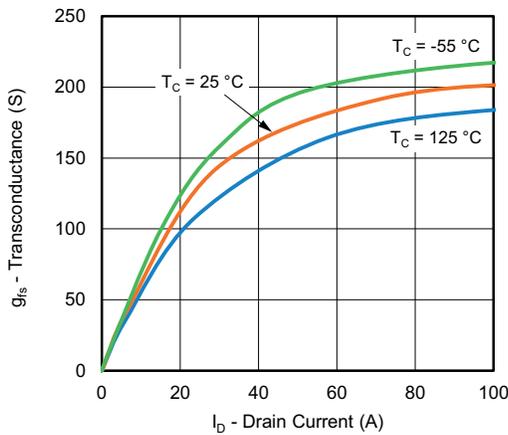
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



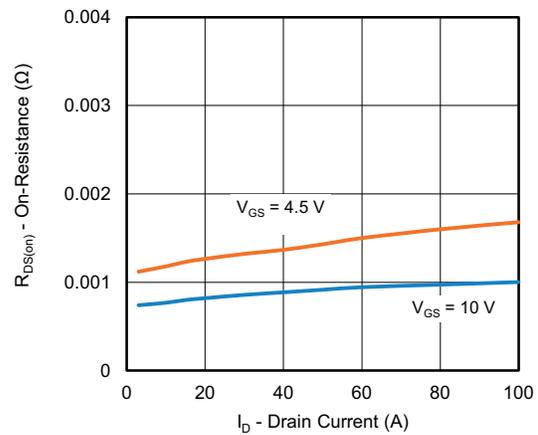
Output Characteristics



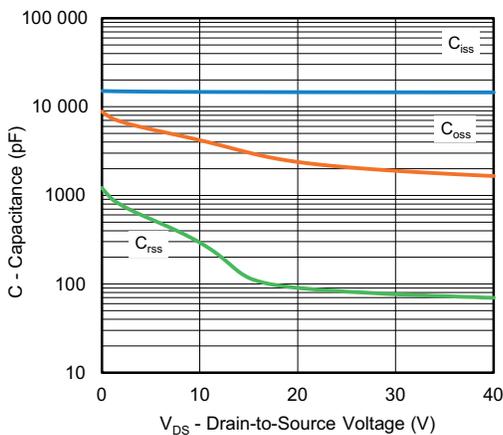
Transfer Characteristics



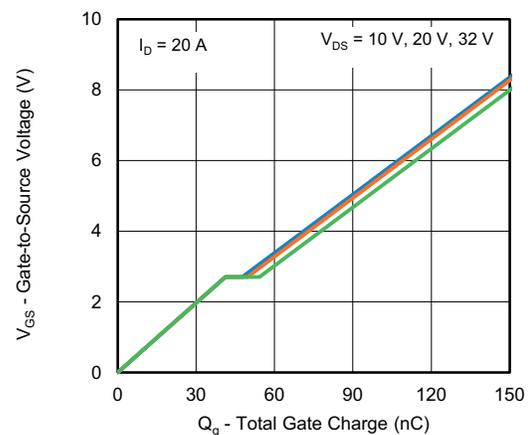
Transconductance



On-Resistance vs. Drain Current



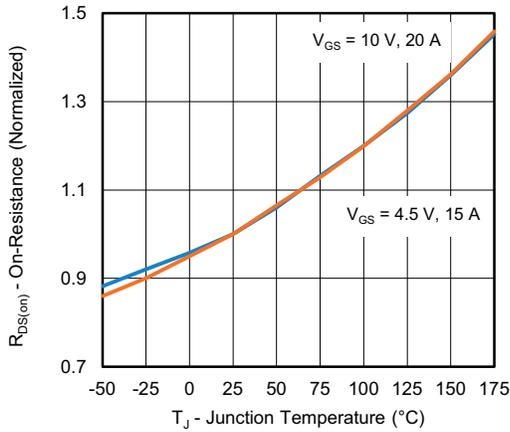
Capacitance



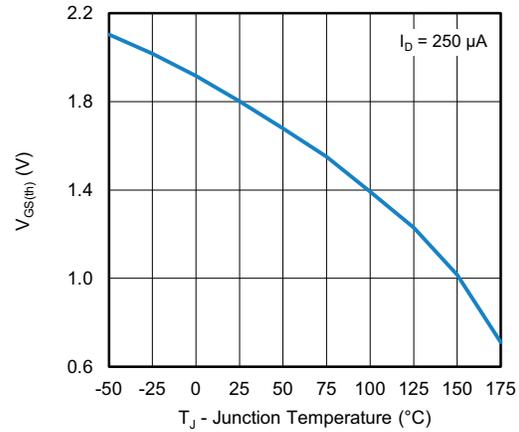
Gate Charge



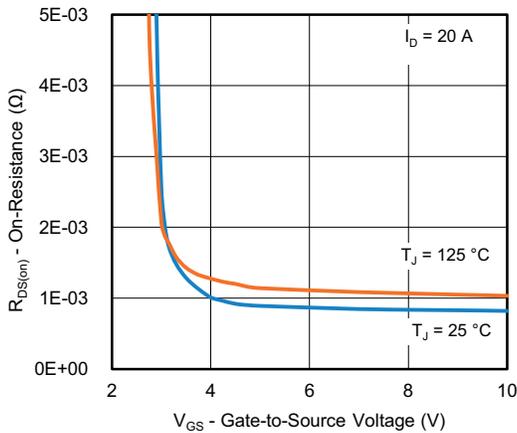
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



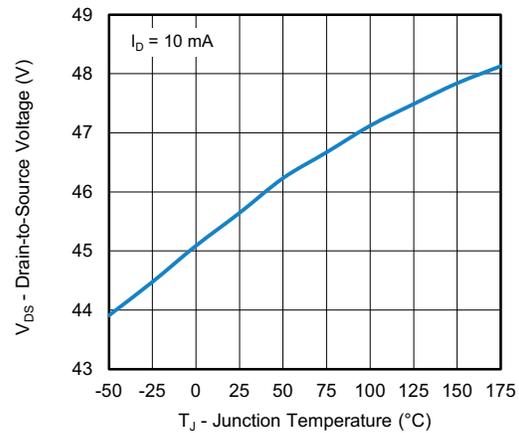
On-Resistance vs. Junction Temperature



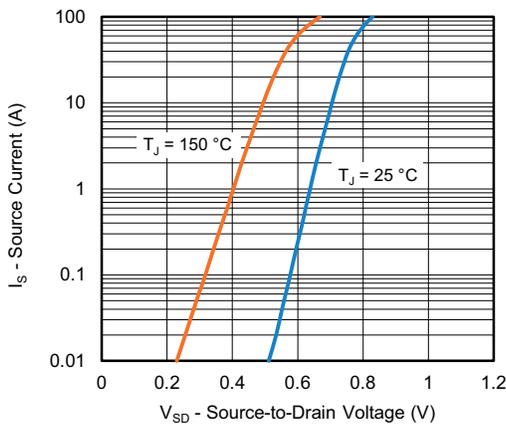
Threshold Voltage



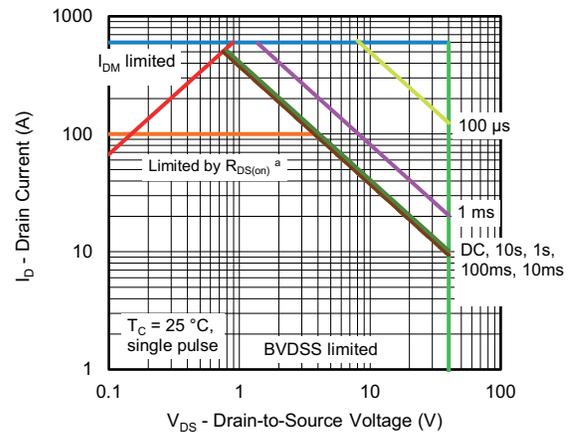
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



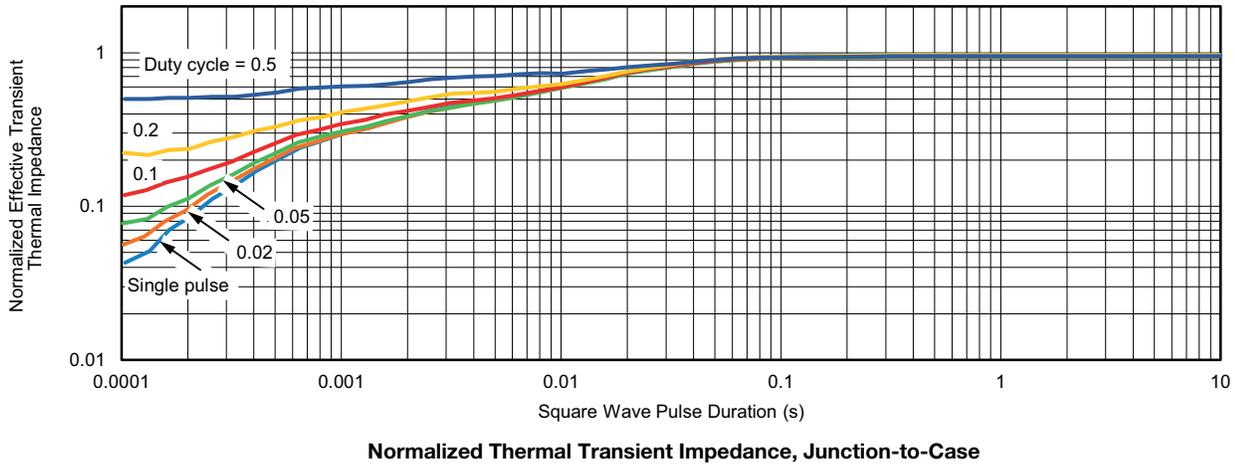
Safe Operating Area

Note

- a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

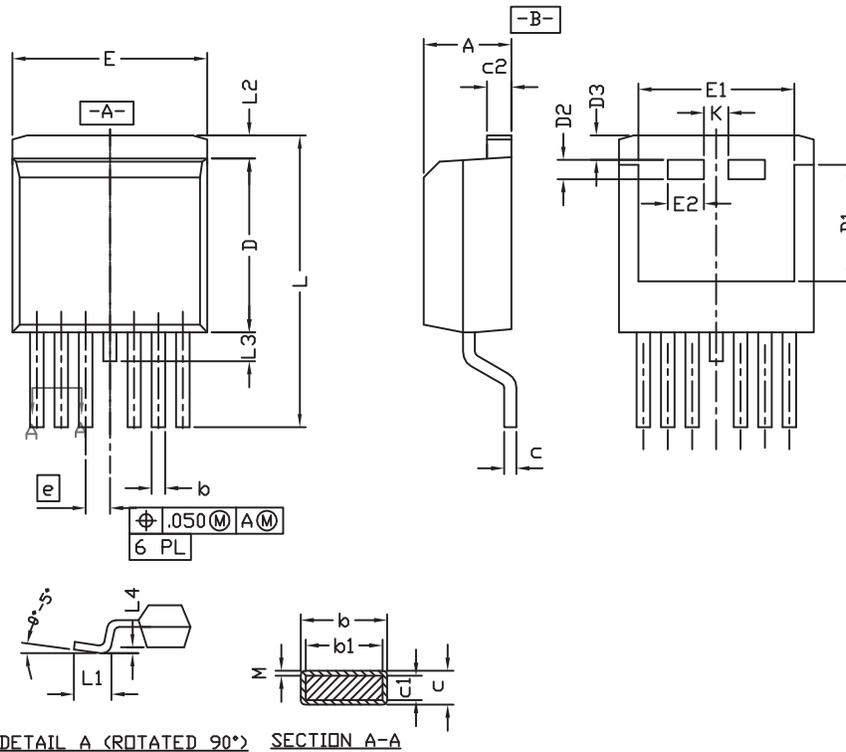


Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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D²PAK (TO-263-7L) Case Outline



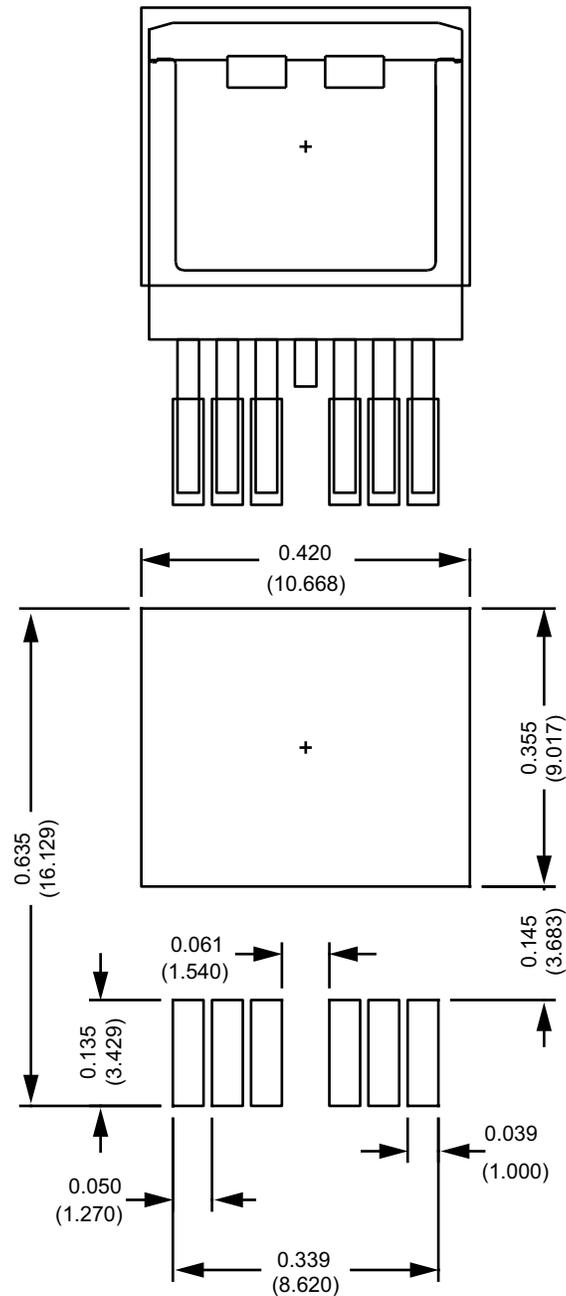
DETAIL A (ROTATED 90°) SECTION A-A

Notes

1. Plane B includes maximum features of heat sink tab and plastic
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
3. Pin to pin coplanarity max. 4 mils
4. Lead thickness 25 mils
5. For SUM part numbers lead thickness is 24 mils to 29 mils
6. For reference only
7. Use inches as the primary measurement
8. This feature is only for SUM

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.260	0.280	6.604	7.112
D2	0.046	0.050	1.168	1.270
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
e	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T22-0410-Rev. D, 19-Sep-2022				
DWG: 6006				

Recommended Land Pattern D²PAK (TO-263-7L)





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