4-Channel I²C Switch with Interrupt and Reset

Features

- Bidirectional Translator of 1:4 I²C Switch
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output and Active-Low Reset Input
- Two Address Terminals, Allowing Up to Four Devices on the I²C Bus
- Operating Power-Supply Voltage Range from 2.3 V to 5.5 V
- Allow Voltage-Level Translation among 2.5-V, 3.3-V, and 5-V Buses
- Support Standard Mode and Fast Mode I²C Devices, 0 to 400-kHz Clock Frequency
- Low R_{ON} Switches
- Latch-up Performance Exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - ±4,000-V Human Body Model
  - ±1,500-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

Description

The TPT29545 is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register. Four interrupt inputs ($\overline{INT0}$ to $\overline{INT3}$) are designed as one for each of the downstream pairs. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{RESET}$) input helps the TPT29545 recover. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed so that the V_{CC} terminal can be used to limit the maximum high voltage which is passed by the TPT29545. This allows the use of different bus voltages on each pair, so that 2.5-V or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

The TPT29545 is available in the TSSOP20 package and is characterized from –40°C to +85°C.

Typical Application Circuit

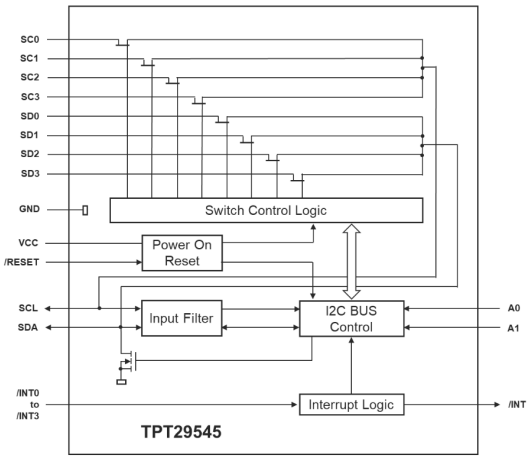


Table of Contents

Revision History

Date	Revision	Notes
2020-03-04	Rev.Pre.0	Initial version.
2021-06-29	Rev.Pre.1	Preliminary version. Added the typical electrical data.
2021-06-30	Rev Pre.2	Updated the Tape and Reel Information.
2021-07-16	Rev.Pre.3	Updated the electrical data.
2021-08-27	Rev.Pre.4	Updated the Order Information.
2022-08-05	Rev.A.0	Released version.
2024-12-24	Rev.A.1	Updated to a new datasheet format. Updated the POD.

Pin Configuration and Functions

TPT29545
TSSOP20
Top View

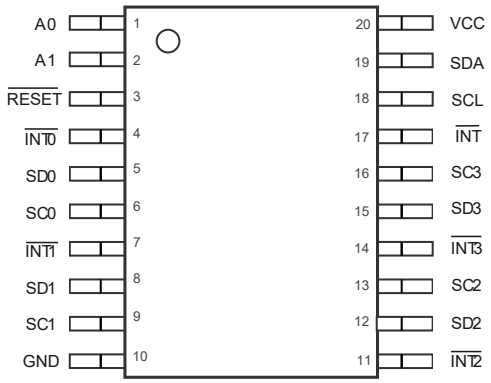


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	A0	I	Address input 0. Connect directly to V_{CC} or ground.
2	A1	I	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{RESET}$	I	Active-low reset input. Connect to V_{CC} or V_{DPUM} (1) through a pull-up resistor if not used.
4	$\overline{INT0}$	I	Active-low interrupt input 0. Connect to V_{DPU0} (1) through a pull-up resistor.
5	SD0	I/O	Serial data 0. Connect to the power of slave channel 0 through a pull-up resistor.
6	SC0	I/O	Serial clock 0. Connect to the power of slave channel 0 through a pull-up resistor.
7	$\overline{INT1}$	I	Active-low interrupt input 1. Connect to V_{DPU1} (1) through a pull-up resistor.
8	SD1	I/O	Serial data 1. Connect to the power of slave channel 1 through a pull-up resistor.
9	SC1	I/O	Serial clock 1. Connect to the power of slave channel 1 through a pull-up resistor.
10	GND	GND	Ground.
11	$\overline{INT2}$	I	Active-low interrupt input 2. Connect to V_{DPU2} (1) through a pull-up resistor.
12	SD2	I/O	Serial data 2. Connect to the power of slave channel 0 through a pull-up resistor.
13	SC2	I/O	Serial clock 2. Connect to the power of slave channel 0 through a pull-up resistor.
14	$\overline{INT3}$	I	Active-low interrupt input 3. Connect to V_{DPU3} (1) through a pull-up resistor.
15	SD3	I/O	Serial data 3. Connect to the power of slave channel 0 through a pull-up resistor.
16	SC3	I/O	Serial clock 3. Connect to the power of slave channel 0 through a pull-up resistor.
17	$\overline{INT}$	O	Active-low interrupt output. Connect to V_{DPUM} (1) through a pull-up resistor.
18	SCL	I/O	Clock bus. Connect to V_{CC} through a pull-up resistor.
19	SDA	I/O	Data bus. Connect to V_{CC} through a pull-up resistor.
20	V_{CC}	Supply	Supply power.

Specifications

Absolute Maximum Ratings (1)

Parameter		Condition	Min	Max	Unit
V_{CC}	Supply Voltage		–0.5	7	V
V_I	Input Voltage		–0.5	7	V
I_{IK}	Input Clamp Current	$V_I < 0$	–20	20	mA
I_{OK}	Output Clamp Current	$V_O < 0$	–25	25	mA
I_{CC}	Continuous Current through GND		–100	100	mA
T_J	Maximum Junction Temperature			125	°C
T_A	Operating Temperature Range		–45	85	°C
T_{STG}	Storage Temperature		–60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Condition	Min	Max	Unit
V_{CC}	Supply Voltage		2.3	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A1, A0, $\overline{RESET}$, $\overline{INTx}$	0.7 × V_{CC}	5.5	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	–0.5	0.3 × V_{CC}	mA
		A1, A0, $\overline{RESET}$, $\overline{INTx}$	–0.5	0.3 × V_{CC}	mA
T_A	Operating Temperature Range		−40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP20	120	50	°C/W

Electrical Characteristics-DC Parameters

All test conditions: V_{CC} = 2.3 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 3.6 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz	−	2.4	20	μA
		V_{CC} = 3.6 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz	−	6.5	30	μA
I_{STB}	Standby Current	V_{CC} = 3.6 V; no load; V_I = V_{CC} or GND	−	0.9	3	μA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND	−	1.2	1.45	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.2		V
Input SCLx; Input/Output SDAx						
V_{IL}	Low-Level Input Voltage	V_{CC} = 2.3 V			0.3 V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 2.3 V	0.7 V_{CC}			V
I_{OL}	Low-Level Output Current	V_{CC} = 2.3 V, V_{OL} = 0.4 V	3	10		mA
	Low-Level Output Current, INT	V_{CC} = 2.3 V, V_{OL} = 0.6 V	6	13		mA
I_L	Leakage Current	V_{CC} = 2.3 V, V_I = V_{CC} or GND	−1	0.1	1	μA
C_I	Input Capacitance (1)	V_I = GND		15		pF
Select Inputs A0, A1, $\overline{\text{RESET}}$						
V_{IL}	Low-Level Input Voltage	V_{CC} = 2.3 V			0.3 V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 2.3 V	0.7 V_{CC}			V
I_{LI}	Input Leakage Current	V_{CC} = 2.3 V, pin at V_{CC} or GND	−1	0.1	1	μA
C_I	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{ON}	On-State Resistance	V_{CC} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	2	4.8	25	Ω
		V_{CC} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	4	6.5	30	Ω
$V_{O(SW)}$	Switch Output Voltage (1)	$V_{I(SW)}$ = V_{CC} = 3.3 V; $I_{O(SW)}$ = −100 μA	−	2.1	−	V
		$V_{I(SW)}$ = V_{CC} = 3.0 V to 3.6 V; $I_{O(SW)}$ = −100 μA	1.6		2.8	V
		$V_{I(SW)}$ = V_{CC} = 2.5 V; $I_{O(SW)}$ = −100 μA	−	1.5	−	V
		$V_{I(SW)}$ = V_{CC} = 2.3 V to 2.7 V; $I_{O(SW)}$ = −100 μA	1		2	V
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IO}	Input/Output Capacitance (1)	V_I = GND		3		pF
Output, $\overline{INT}$						
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V	3			mA
I_{OH}	High-Level Output Current				10	μA

(1) Parameters are provided by lab bench tests and design simulation.

Electrical Characteristics-DC Parameters (Continued)

All test conditions: V_{CC} = 4.5 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz	−	5	20	μA
		V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		14	30	μA
I_{STB}	Standby Current	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND	−	1.8	3	μA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND	−	1.25	1.45	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage (1)	V_{CC} = 5.5 V			0.3 V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 5.5 V	0.7 V_{CC}			V
I_{OL}	Low-Level Output Current	V_{CC} = 5.5 V, V_{OL} = 0.4 V	3	22		mA
	Low-Level Output Current, INT	V_{CC} = 5.5 V, V_{OL} = 0.6 V	6	32		mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA
C_I	Input Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$, $\overline{\text{INTx}}$						
V_{IL}	Low-Level Input Voltage	V_{CC} = 5.5 V			0.3 V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 5.5 V	0.7 V_{CC}			V
I_{LI}	Input Leakage Current	Pin at V_{CC} or GND	−1	0.1	1	μA
C_I	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{ON}	On-State Resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	1	3.3	20	Ω
$V_{O(SW)}$	Switch Output Voltage (1)	$V_{I(SW)}$ = V_{CC} = 5.0 V; $I_{O(SW)}$ = −100 μA	−	3.55	−	V
		$V_{I(SW)}$ = V_{CC} = 4.5 V to 5.5 V; $I_{O(SW)}$ = −100 μA	2.6		4.5	V
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA
C_{IO}	Input/Output Capacitance (1)	V_I = GND		3		pF
Output, $\overline{\text{INT}}$						
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V	3			mA
I_{OH}	High-Level Output Current				10	μA

(1) Parameters are provided by lab bench tests and design simulation.

Electrical Characteristics-AC Parameters

I²C Interface Timing Requirements

All test conditions: over recommended operating free-air temperature range, unless otherwise noted.

Parameter		Condition	Min	Max	Unit
I²C BUS—Fast Mode					
f_{SCL}	I²C Clock Frequency		0	400	kHz
t_{SCH}	I²C Clock High Time		0.6		μs
t_{SCL}	I²C Clock Low Time		1.3		μs
t_{SP}	I²C Spike Time			50	ns
t_{SDS}	I²C Serial Data Setup Time		100		ns
t_{SDH}	I²C Serial Data Hold Time		0		ns
t_{ICR}	I²C Input Rise Time		20	300	ns
t_{ICF}	I²C Input Fall Time		20 + 0.1 Cb	300	ns
t_{OCF}	I²C Output Fall Time (1)	10-pF to 400-pF bus	20 + 0.1 Cb	300	ns
t_{BUF}	I²C Bus Free Time between Stop and Start		1.3		μs
t_{STS}	I²C Start or Repeated Start Condition Setup		0.6		μs
t_{STH}	I²C Start or Repeated Start Condition Hold		0.6		μs
t_{SPS}	I²C Stop Condition Setup		0.6		μs
$t_{VD(DATA)}$	Valid Data Time	SCL Low to SDA output valid		0.9	μs
$t_{VD(ACK)}$	Valid Data Time of ACK Condition	ACK signal from SCL Low to SDA (out) Low		0.9	μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter			50	ns
t_{PD}	Propagation Delay (1)	From SDA to SDx, or SCL to SCx		0.3	ns
C_B	I²C Bus Capacitive Load			400	pF

(1) The propagation delay is calculated from the 20 typical R_{ON} and the 15-pF load capacitance.

Switching Characteristics

All test conditions: over recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
$T_{VD;\ DAT}$	Data Valid Time	High to Low		1	μs
		Low to High		0.55	μs

Symbol	Description	Condition	Min	Max	Unit
$T_{VD;\ DAT}$	Data Valid Time Acknowledge Time			1	ns
$\overline{\text{RESET}}$					
$t_{W(RST)L}$	Low-Level Reset Time		4		ns
t_{RST}	Reset Time	SDA clear		500	ns
$t_{REC;STA}$	Recovery Time to START Condition		0		ns

Parameter Measurement Waveforms

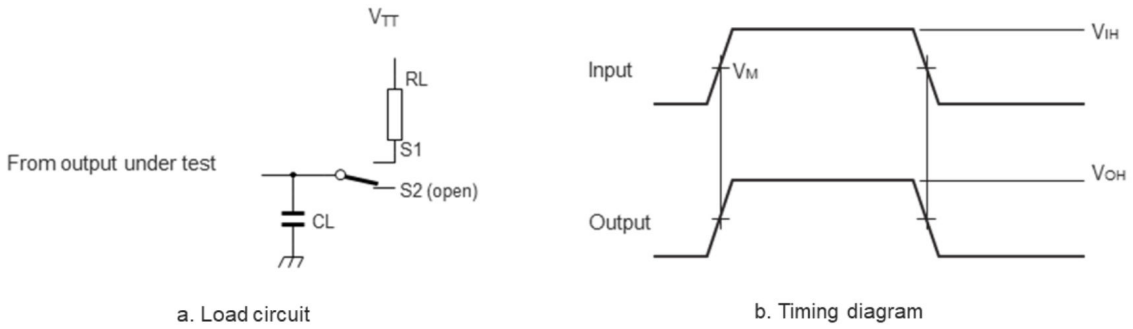


Figure 1. Load Circuit for Outputs

Detailed Description

Overview

The TPT29545 is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register. Four interrupt inputs ($\overline{INT0}$ to $\overline{INT3}$) are designed as one for each of the downstream pairs. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{RESET}$) input helps the TPT29545 recover. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

Functional Block Diagram

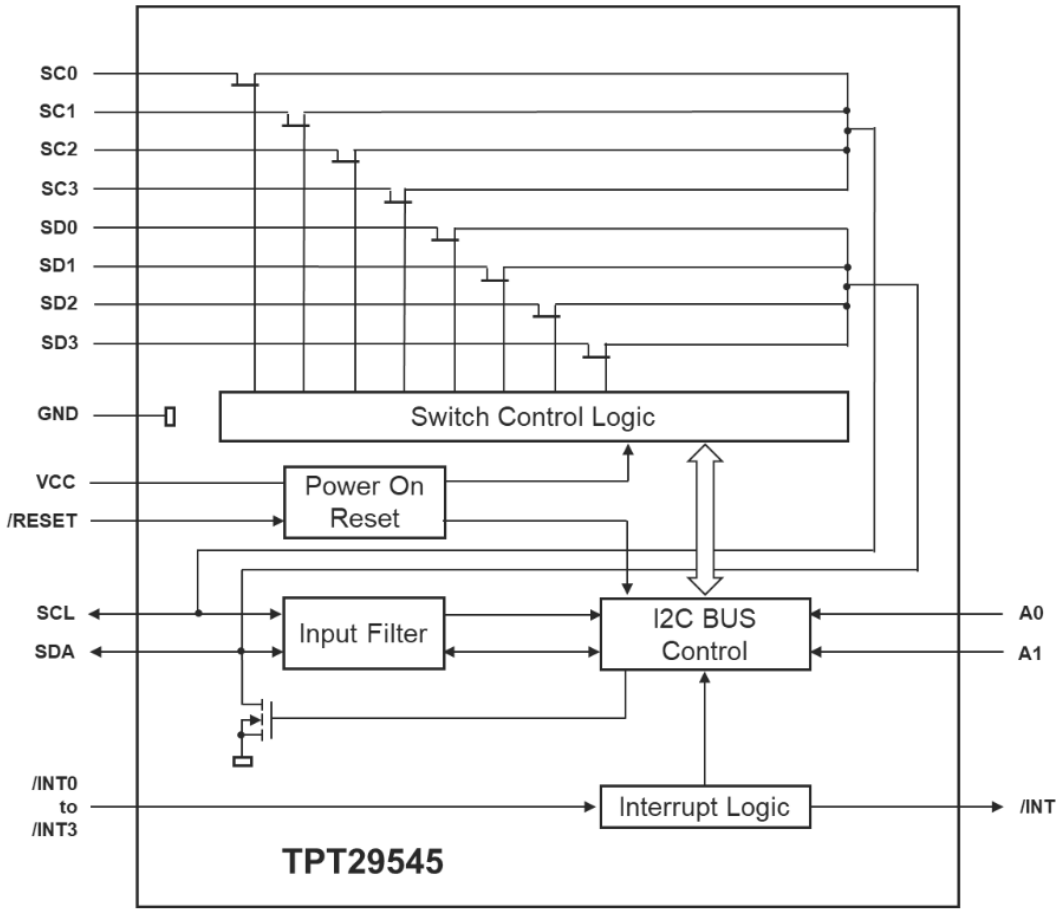


Figure 2. Functional Block Diagram

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

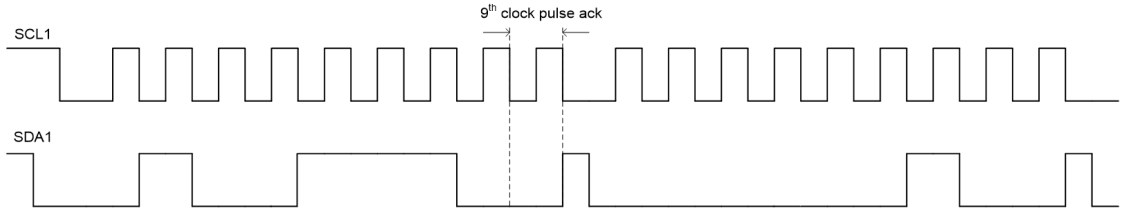


Figure 3. I²C Bus (2.3 V to 5.5 V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave when it is accessing. To conserve power, no internal pull-up resistor is incorporated on the hardware selectable address pins, and they must be pulled high or low. The address of the TPT29545 is shown below.

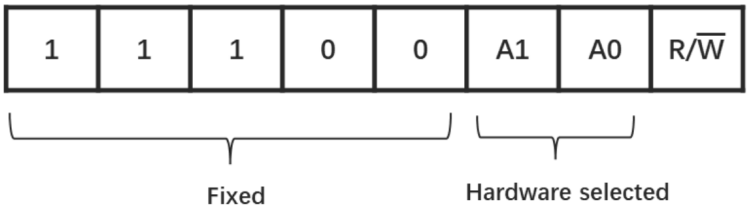


Figure 4. Slave Device Address

Control Register

Following the successful acknowledgement of the slave address, the bus master sends a byte to the TPT29545 which is stored in the control register. If multiple bytes are received by the TPT29545, it saves the last byte received. This register can be written and read via the I²C bus.

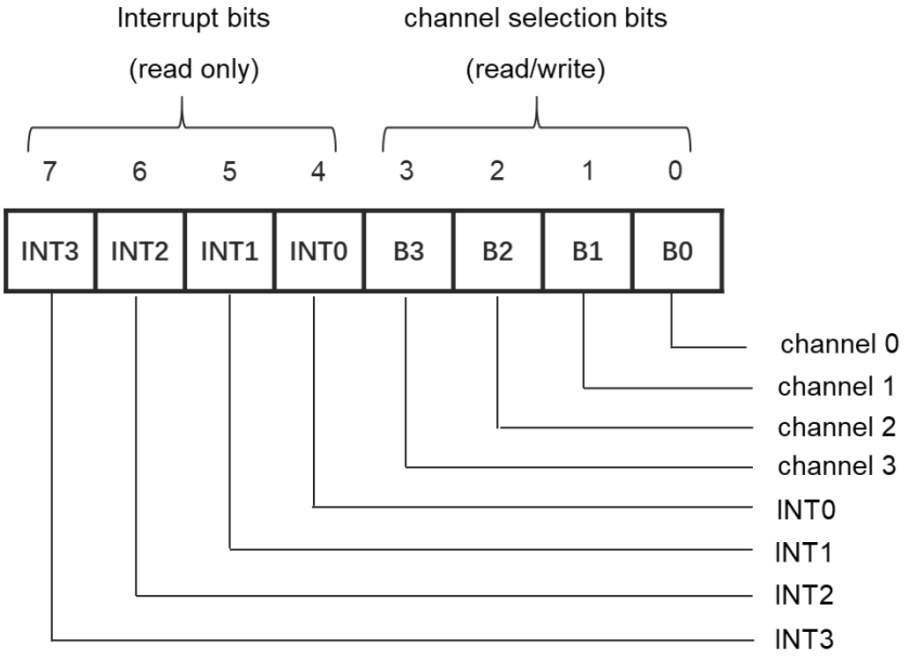


Figure 5. Control Register

Control Register Definition

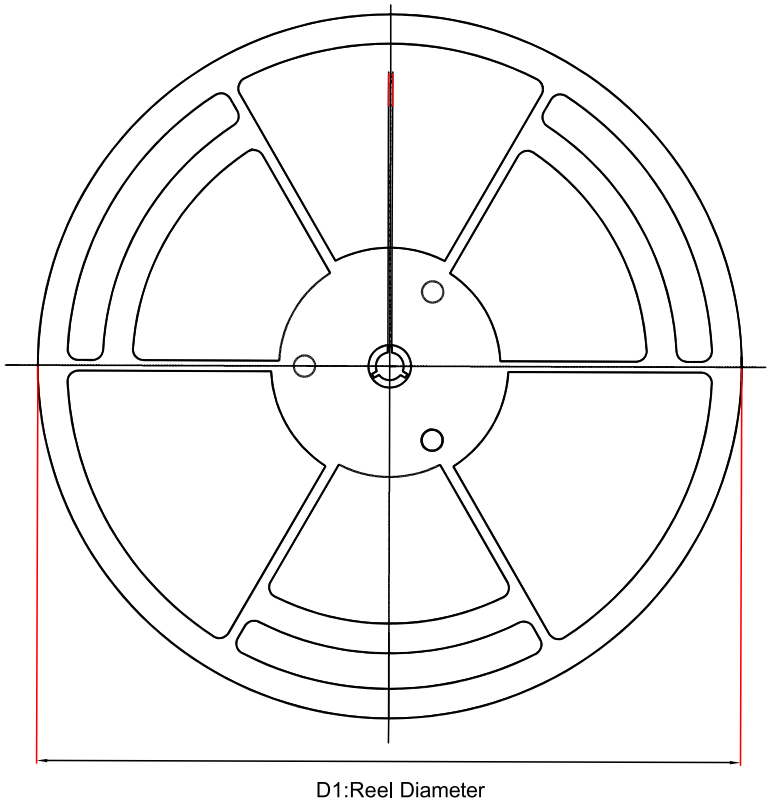
One or several SCx/SDx downstream pair(s), or channel(s), are selected by the contents of the control register. This register is written after the TPT29545. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a STOP condition has been placed on the I²C bus. This ensures that all SCx/SDx lines are in a high state when the channel is made active so that no false conditions are generated during the connection.

Table 2. Control Register: Write—Channel Selection; Read—Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Multiple channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, which means that channel 0 and channel 3 are disabled while channel 1 and channel 2 are enabled. Should not exceed the maximum bus capacitance.

Tape and Reel Information



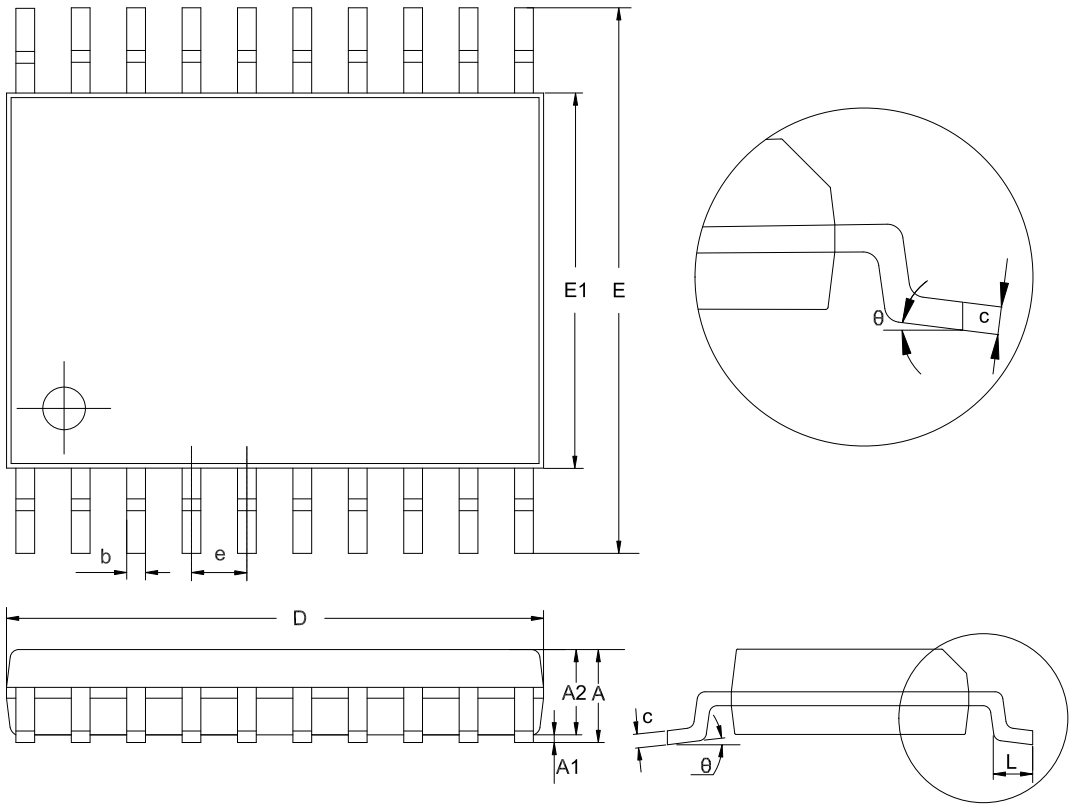
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29545-TS4R	TSSOP20	330	22.4	6.8	6.9	1.5	8.0	16.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

TSSOP20

Package Outline Dimensions TS4(TSSOP-20-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.260
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29545-TS4R	−40 to 85°C	TSSOP20	29545	3	Tape and Reel, 3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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