UMW AOD2610E

60V N-Channel MOSFET

1.Description

- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Eoss
- E_{SD} protected
- RoHS and Halogen-Free Compliant

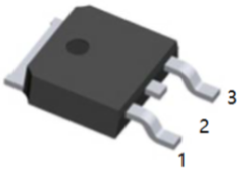
2.Features

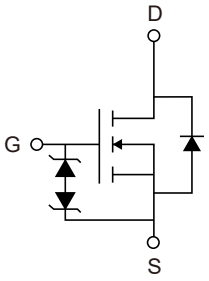
- $V_{DS\ (V)}$=60V
- I_D=46A(V_{GS}=10V)
- $R_{DS(ON)}$<9.5mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<13.3mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [G]	T_C=25°C	I_D	46	A
	T_C=100°C		36.5	
Pulsed Drain Current [C]		I_{DM}	110	
Continuous Drain Current	T_A=25°C	I_{DSM}	19	
	T_A=70°C		15	
Avalanche Current [c]		I_{AS}	17	
Avalanche energy L=0.3mH [c]		E_{AS}	43	mJ
V_{DS} Spike [I]	10μs	V_{SPIKE}	72	V
Power Dissipation [B]	T_C=25°C	P_D	59.5	W
	T_C=100°C		23.5	

Power Dissipation [A]	T_C=25°C	P_{DSM}	6.2	W
	T_C=70°C		4	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient [AD]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.7	2.1	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
		T_J=55°C			5	μA
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.4	1.8	2.4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		7.7	9.5	mΩ
		V_{GS}=4.5V, I_D=20A		10.3	13.3	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A		52		S
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V		0.72	1	V
Maximum Body-Diode Continuous Current [G]	I_S				46	A
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=30V, f=1MHz		1100		pF
Output Capacitance	C_{oss}			300		pF
Reverse Transfer Capacitance	C_{rss}			28		pF
Gate resistance	R_g	f=1MHz	0.6	1.2	2	Ω
Total Gate Charge	Q_g(10V)	V_{GS}=10V, V_{DS}=30V, I_D=20A		14.5	25	nC
Total Gate Charge	Q_g(4.5V)			7	13	nC
Gate Source Charge	Q_{gs}			2.5		nC
Gate Drain Charge	Q_{gd}			3.5		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=10V, V_{DS}=30V, R_L=1.5Ω, R_{GEN}=3Ω		6.5		ns
Turn-On Rise Time	t_r			3.5		ns
Turn-Off DelayTime	$t_{D(off)}$			22		ns
Turn-Off Fall Time	t_f			3		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A, dI/dt=500A/μs		19		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=20A, dI/dt=500A/μs		65		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

I. The spike duty cycle 5% max, limited by junction temperature $T_{J(MAX)}$=125°C.

7.1Typical characteristic

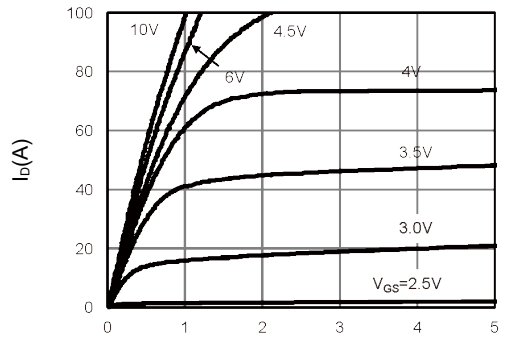


Figure 1: On-Region Characteristics (Note E)

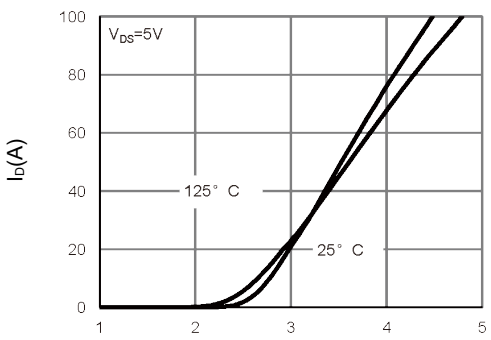


Figure 2: Transfer Characteristics (Note E)

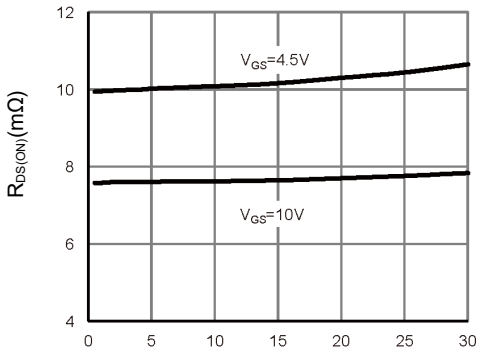


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

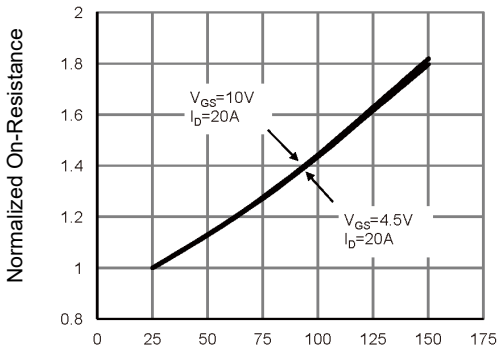


Figure 4: On-Resistance vs. Junction Temperature (Note E)

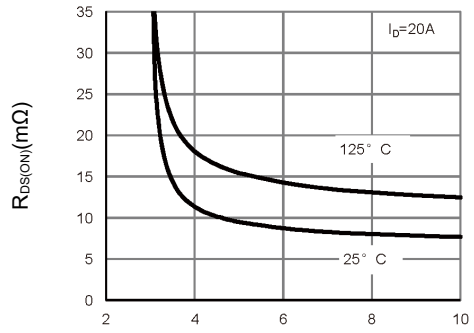


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

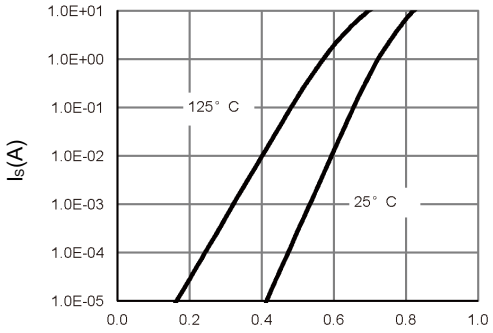


Figure 6: Body-Diode Characteristics(Note E)

7.2Typical characteristic

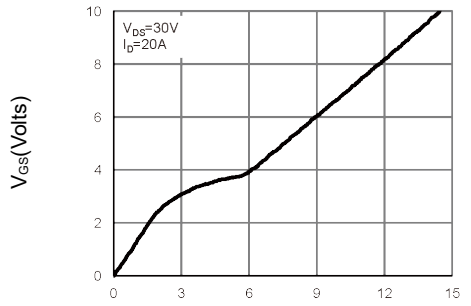


Figure 7: Gate-Charge Characteristics

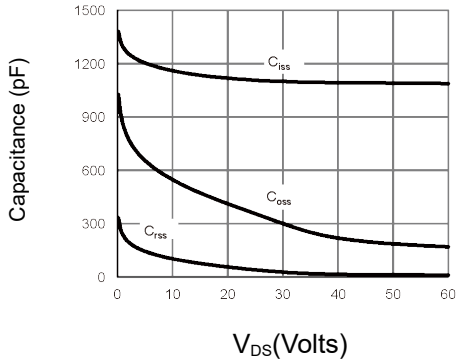


Figure 8: Capacitance Characteristics

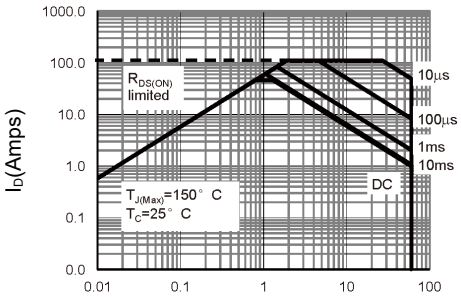


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

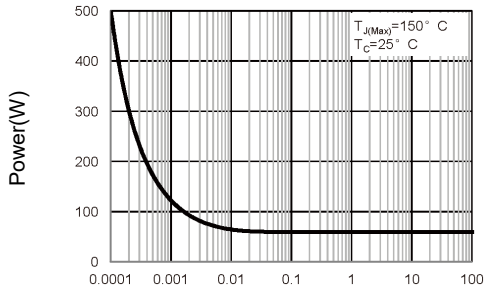


Figure 10: Single Pulse Power Rating Junction-to Case (Note F)

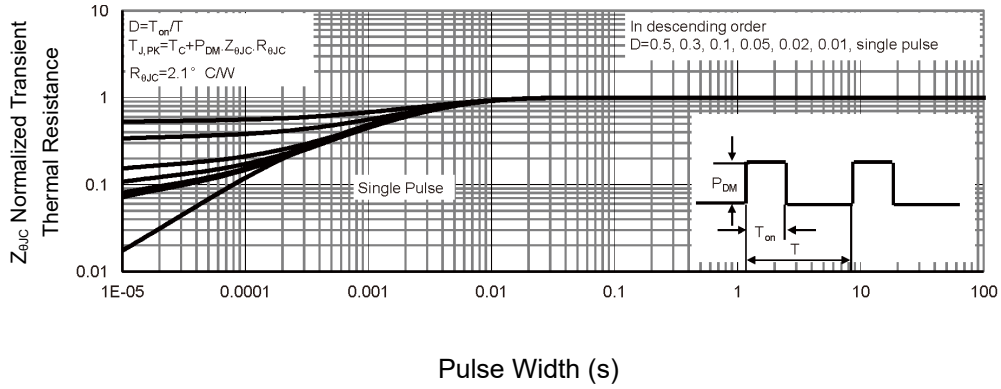


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

7.3Typical characteristic

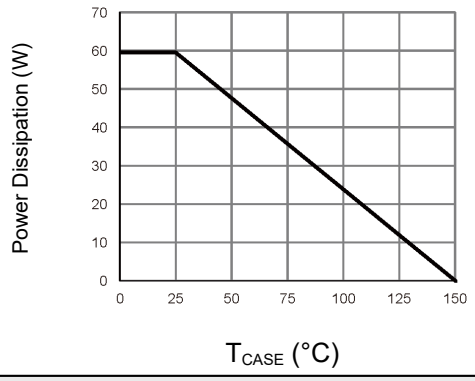


Figure 12: Power De-rating (Note F)

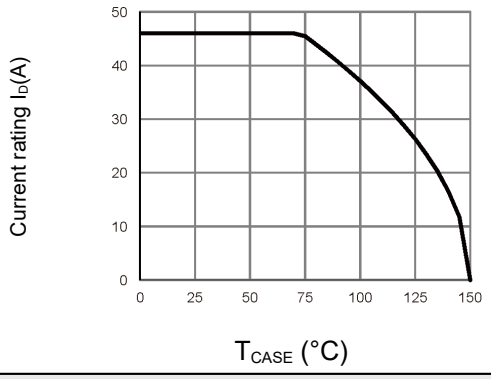


Figure 13: Current De-rating (Note F)

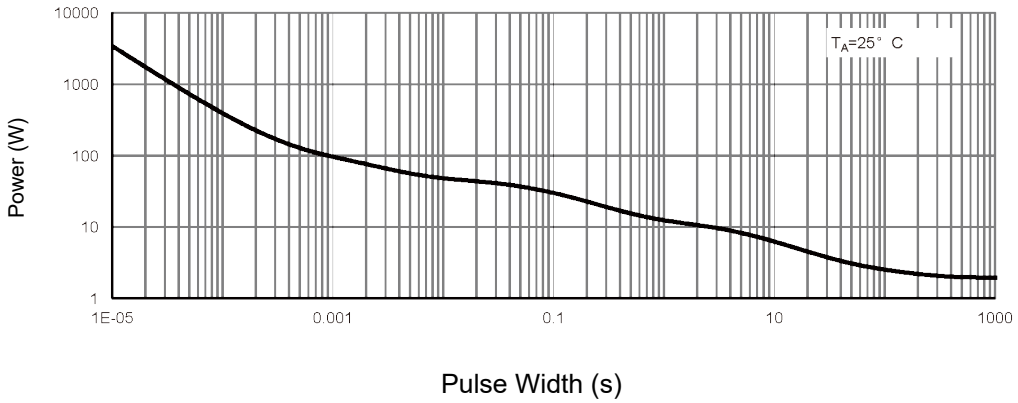


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

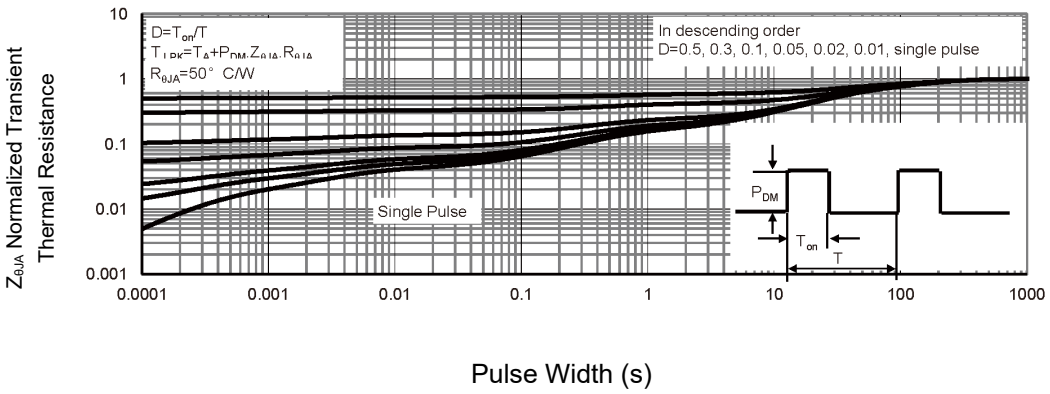


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

7.4Typical characteristic

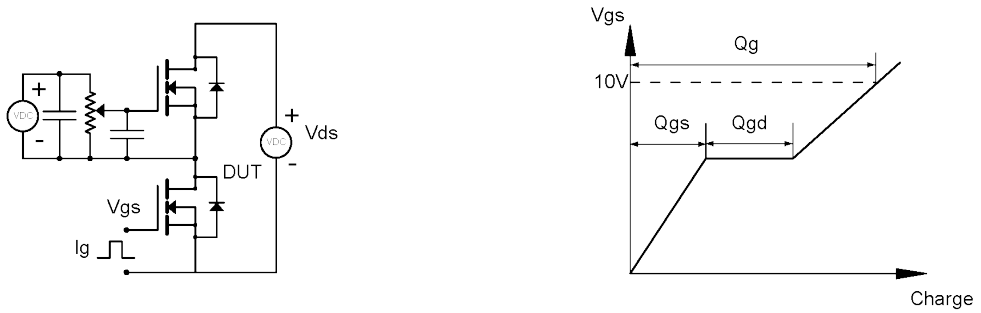


Figure A: Gate Charge Test Circuit & Waveforms

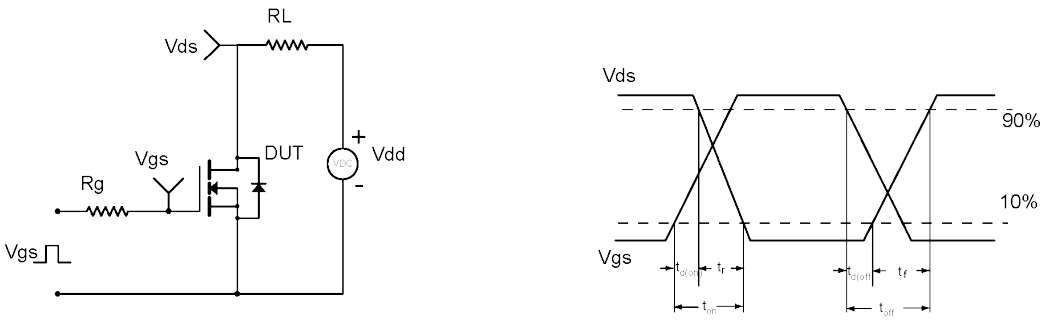


Figure B: Resistive Switching Test Circuit & Waveforms

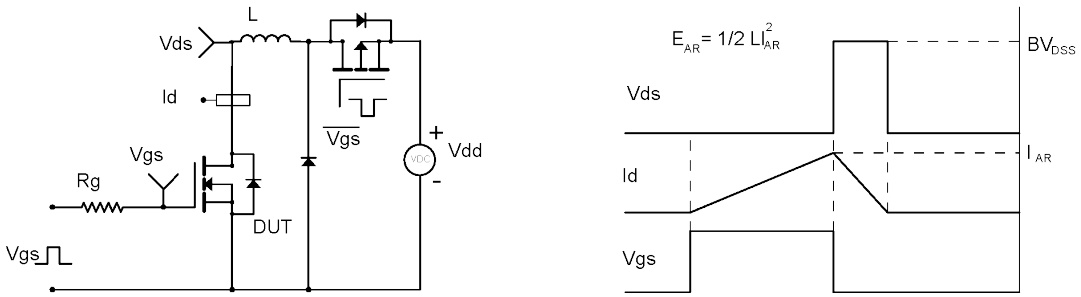


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

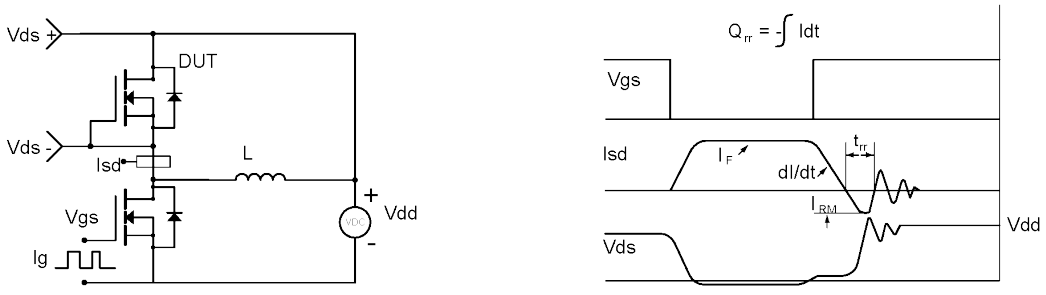
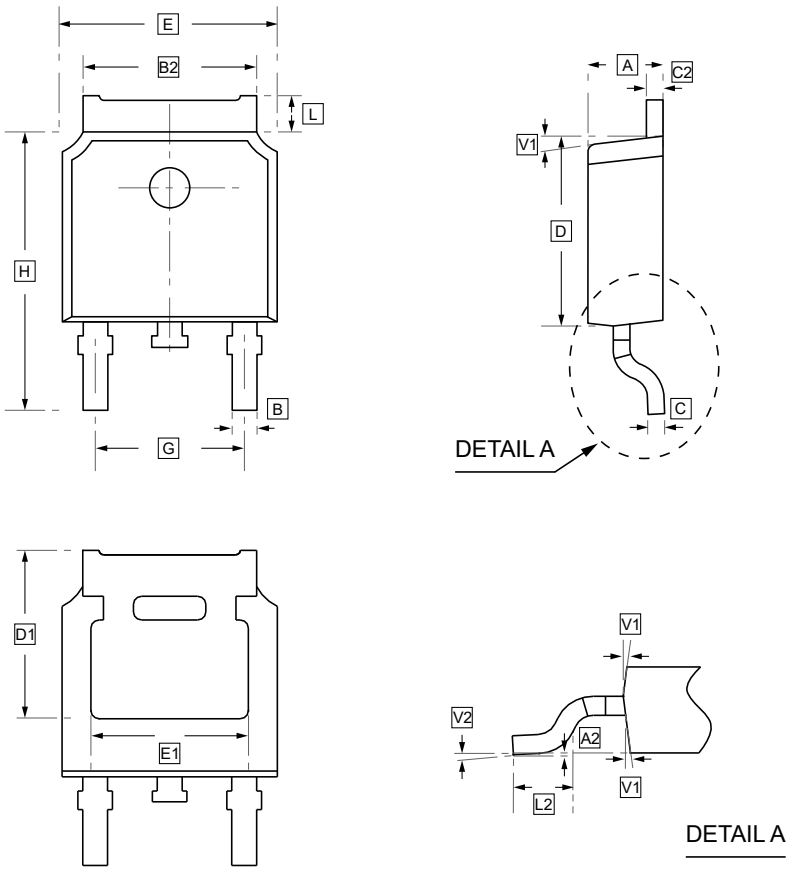


Figure D: Diode Recovery Test Circuit & Waveforms

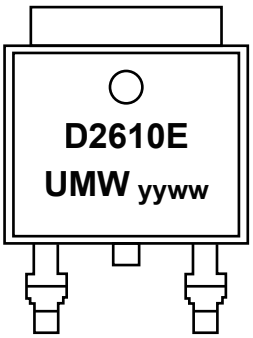
8.TO-252 PACKAGE OUTLINE DIMENSIONS



DIMENSIONS (mm are the original dimensions)

Symbol	A	A2	B	B2	C	C2	D	D1	E	E1	G	H	L	L2	V1	V2
Min	2.10	0	0.66	5.18	0.40	0.44	5.90	5.30	6.40	4.63	4.47	9.50	1.09	1.35		0°
Max	2.50	0.10	0.86	5.48	0.60	0.58	6.30	REF	6.80		4.67	10.70	1.21	1.65		6°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AOD2610E	TO-252	2500	Tape and reel

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