512Mx8, 256Mx16 4Gb DDR3 SDRAM with On-Chip ECC

JANUARY 2024

FEATURES

- Standard Voltage: V_{DD} and V_{DDQ} = 1.5V ± 0.075V
- Low Voltage (L): V_{DD} and V_{DDQ} = 1.35V + 0.1V, -0.067V
  - Backward compatible to 1.5V
- 8 internal banks for concurrent operation
- 8n-Bit pre-fetch architecture
- Programmable CAS Latency
- Programmable Additive Latency: 0, CL-1,CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)
- Refresh Interval:
  - 7.8 µs (8192 cycles/64 ms) Tc= -40°C to 85°C
  - 3.9 µs (8192 cycles/32 ms) Tc= 85°C to 95°C
  - 1.95 µs (8192 cycles/16 ms) Tc= 95°C to 105°C
  - 0.97 µs (8192 cycles/8 ms) Tc= 105°C to 115°C
  - 0.488 µs (8192 cycles/4 ms) Tc= 115°C to 125°C
- Partial Array Self Refresh
- Asynchronous RESET pin
- TDQS (Termination Data Strobe) supported (x8 only)
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Up to 200 MHz in DLL off mode
- Operating temperature:
  - Commercial (T_C = 0°C to +95°C)
  - Industrial (T_C = -40°C to +95°C)
  - Automotive, A1 (T_C = -40°C to +95°C)
  - Automotive, A2 (T_C = -40°C to +105°C)
  - Automotive, A25 (T_C = -40°C to +115°C)
  - Automotive, A3 (T_C = -40°C to +125°C)

ECC FEATURES

- ECC Single bit error protection (per 4-bits)
- 1-bit error correction, 2-bit error detection
- 6 ECC registers to set ECC features, to store ECC event status
- ECC registers can be accessed by Mode Register access or I^{2}C interface by ordering option
- ERR output signal

OPTIONS

- Configuration: 512Mx8, 256Mx16
- Green Package:
  - 96-ball BGA (10mm x 14mm) for x16
  - 78-ball BGA (10mm x 14mm) for x8
- Speed bin up to 1866

ADDRESS TABLE

Parameter	512Mx8	256Mx16
Row Addressing	A0-A15	A0-A14
Column Addressing	A0-A9	A0-A9
Bank Addressing	BA0-2	BA0-2
Page size	1KB	2KB
Auto Precharge Addressing	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#

SPEED BIN

Speed Option	125L	125K	107N	Units
JEDEC Speed Grade	DDR3-1600L	DDR3-1600K	DDR3-1866N	
CL-nRCD-nRP	12-11-11	11-11-11	14-13-13	tCK
tRCD,tRP(min)	13.75	13.75	13.91	ns
tAA(min)	15.00	13.75	14.98	ns

1. DDR3 PACKAGE BALLOUT

1.1 DDR3 SDRAM package ballout 78-ball BGA – x8

	1	2	3	4	5	6	7	8	9
A	VSS	VDD	NC				NU/TDQS#	VSS	VDD
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ
D	VSSQ	DQ6	DQS#				VDD	VSS	VSSQ
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ
F	NC/SCL[2]	VSS	RAS#				CK	VSS	NC/SDA[2]
G	ODT	VDD	CAS#				CK#	VDD	CKE
H	NC/AD0[2]	CS#	WE#				A10/AP	ZQ	NC/ERR[3]
J	VSS	BA0	BA2				A15	VREFCA	VSS
K	VDD	A3	A0				A12/BC#	BA1	VDD
L	VSS	A5	A2				A1	A4	VSS
M	VDD	A7	A9				A11	A6	VDD
N	VSS	RESET#	A13				A14	A8	VSS

Notes:
1. NC balls have no internal connection.
2. SDA, SCL and AD0 balls are for optional I^2C interface, and are available for optional B2, B4 packages.
3. ERR ball is available for optional B2, B3 packages.

1.2 DDR3 SDRAM package ballout 96-ball BGA – x16

	1	2	3	4	5	6	7	8	9
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS
B	VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ
G	VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ
J	NC/SCL[2]	VSS	RAS#				CK	VSS	NC/SDA[2]
K	ODT	VDD	CAS#				CK#	VDD	CKE
L	NC/AD0[2]	CS#	WE#				A10/AP	ZQ	NC/ERR[3]
M	VSS	BA0	BA2				NC(A15)[1]	VREFCA	VSS
N	VDD	A3	A0				A12/BC#	BA1	VDD
P	VSS	A5	A2				A1	A4	VSS
R	VDD	A7	A9				A11	A6	VDD
T	VSS	RESET#	A13				A14	A8	VSS

Notes:

1. NC balls have no internal connection. NC(A15) is an NC pin and reserved for higher densities.
2. SDA, SCL and AD0 balls are for optional I^2C interface, and are available for optional B2, B4 packages.
3. ERR ball is available for optional B2, B3 packages.

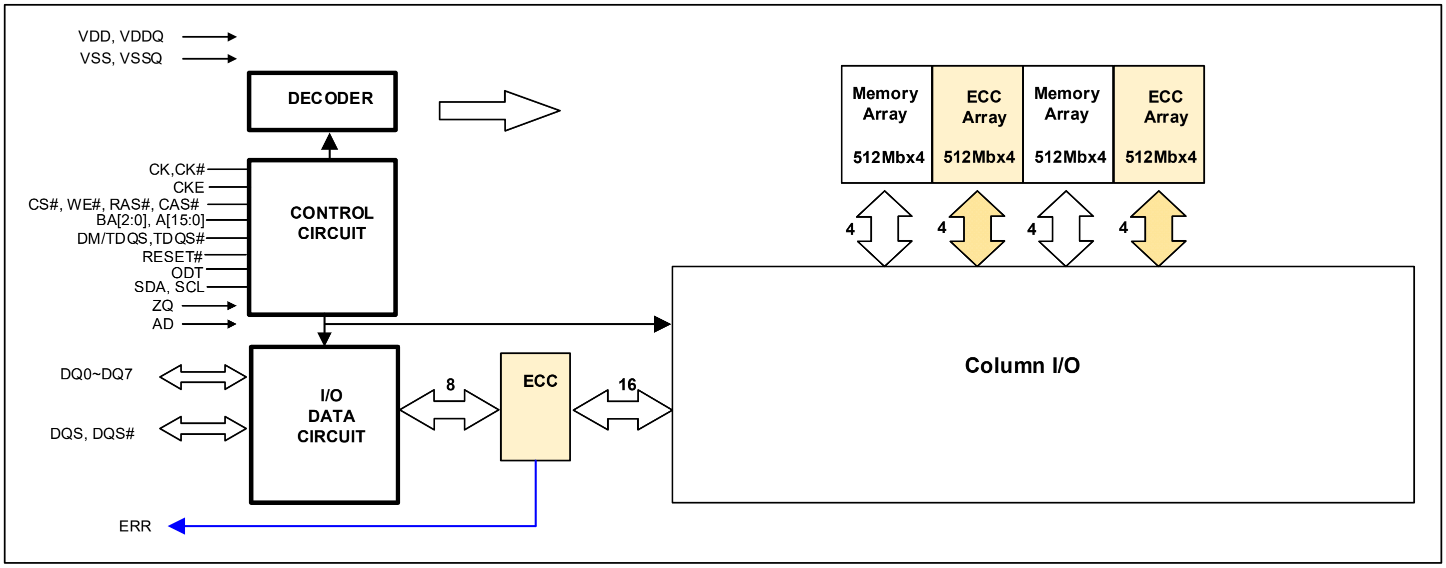
1.3 Pinout Description - JEDEC Standard

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 1.20V for DC high and 0.30V for DC low.
DQ(DQL, DQU)	Input / Output	Data Input/ Output: Bi-directional data bus.
DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.

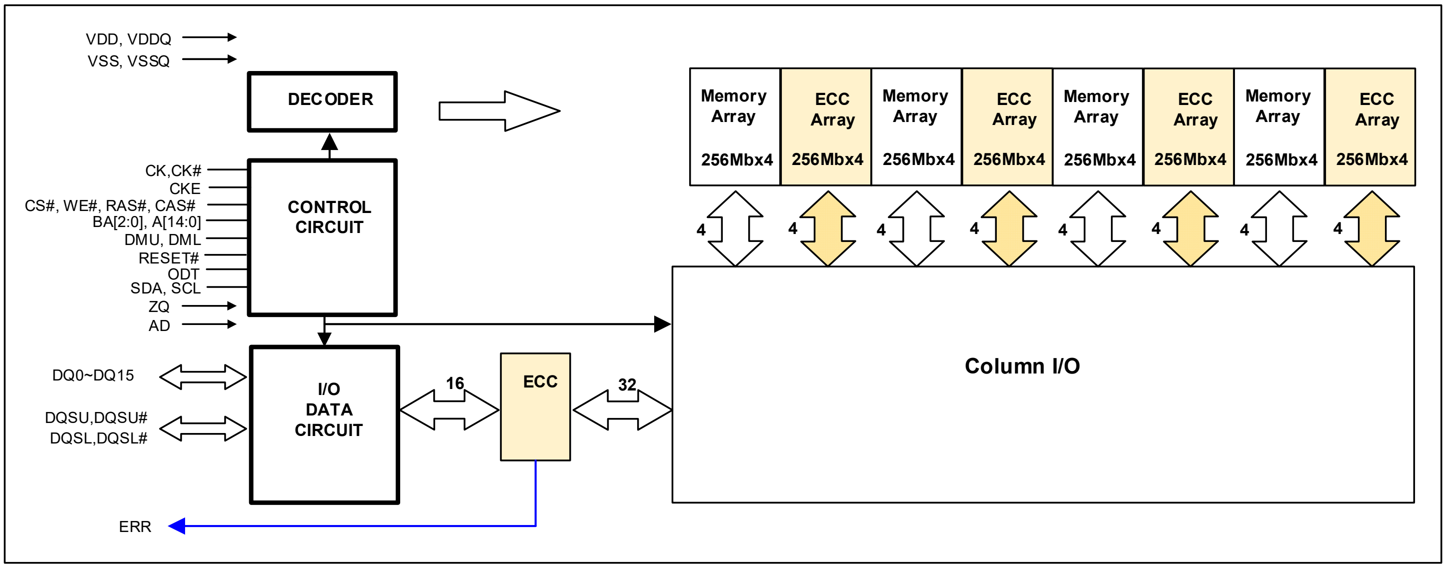
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage
VSS	Supply	Ground
VREFDQ	Supply	Reference voltage for DQ
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ
SDA	Input/Output	Serial Data Address: This is a bidirectional pin for the two-wire interface. It is open-drain and is intended to be wire-AND'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity. An external pull-up resistor (1K ohm) is required, if using I^2C.
SCL	Input	Serial Clock: The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input incorporates a Schmitt trigger input for noise immunity. The pin is pulled up internally. An external pull-up resistor (1K ohm) is required, if using I^2C.
AD0	Input	Device Select Address: The pin is used to select one of two devices of the same type on the same two-wire bus. To select the device, the pin must be pulled-up ("1"), or pulled down ("0") to match the corresponding bits contained in the slave address.
ERR	Output	ERR Signal: Indicates ECC event. Asynchronous output signal. If unused, may be left floating.

Note: Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

1.4 Functional Block Diagram for 4Gb DDR3 x8

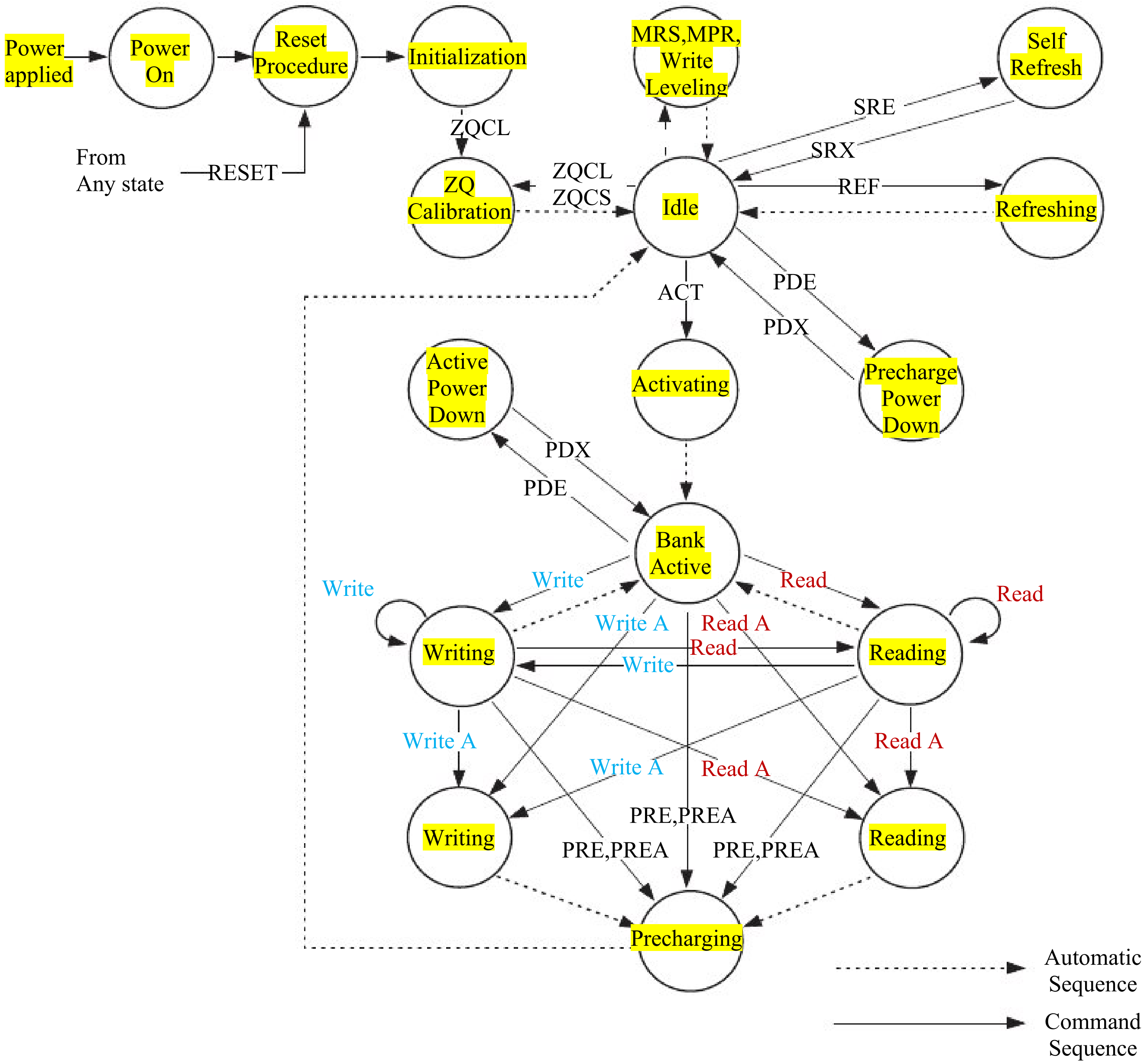


Functional Block Diagram for 4Gb DDR3 x16



2. FUNCTION DESCRIPTION

2.1 Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short		

2.2 RESET and Initialization Procedure

2.2.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300mV to VDD(min) must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.

- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
- Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 x tCK)

6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)

7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)

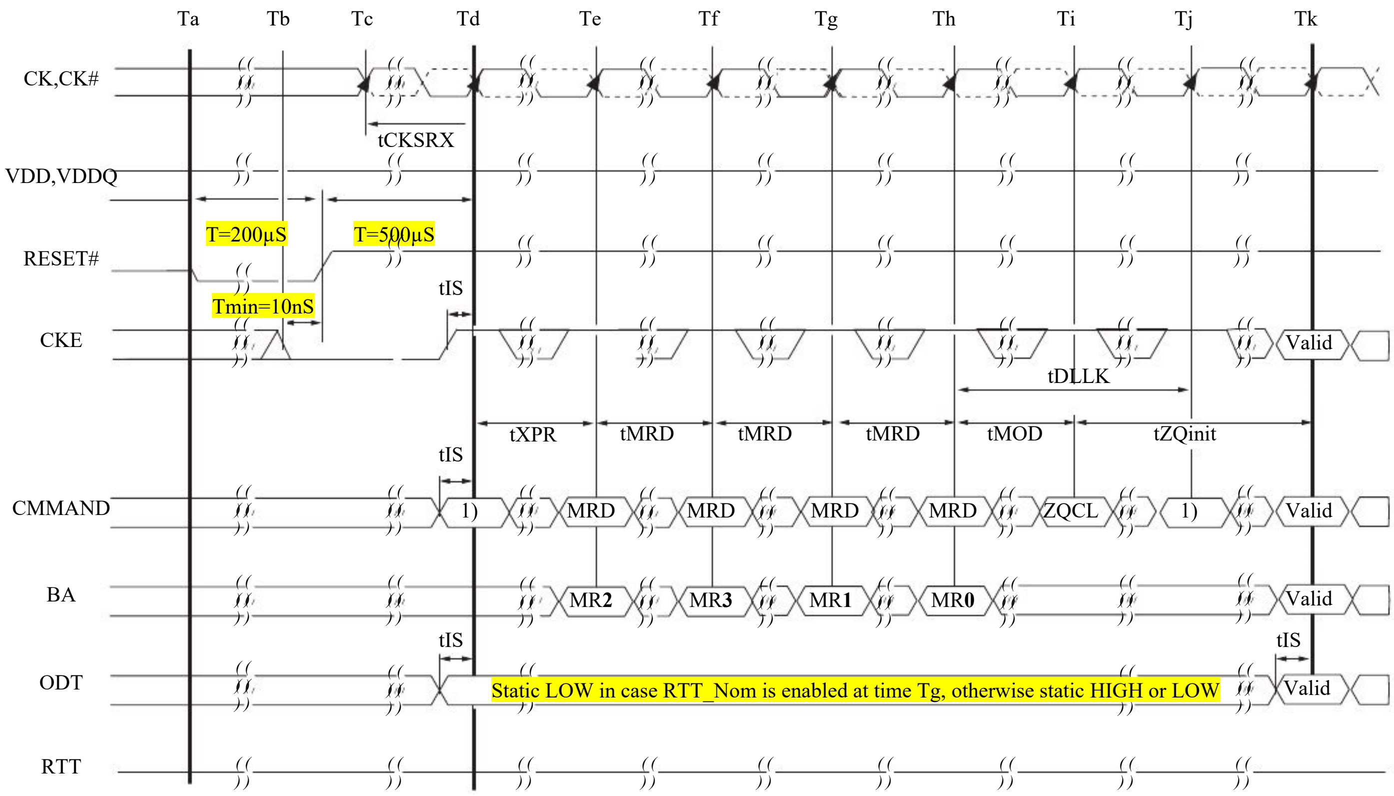
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).

9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.



Note1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Figure2.1.1 Reset and Initialization Sequence at Power-on Ramping

2.2.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled “LOW” before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

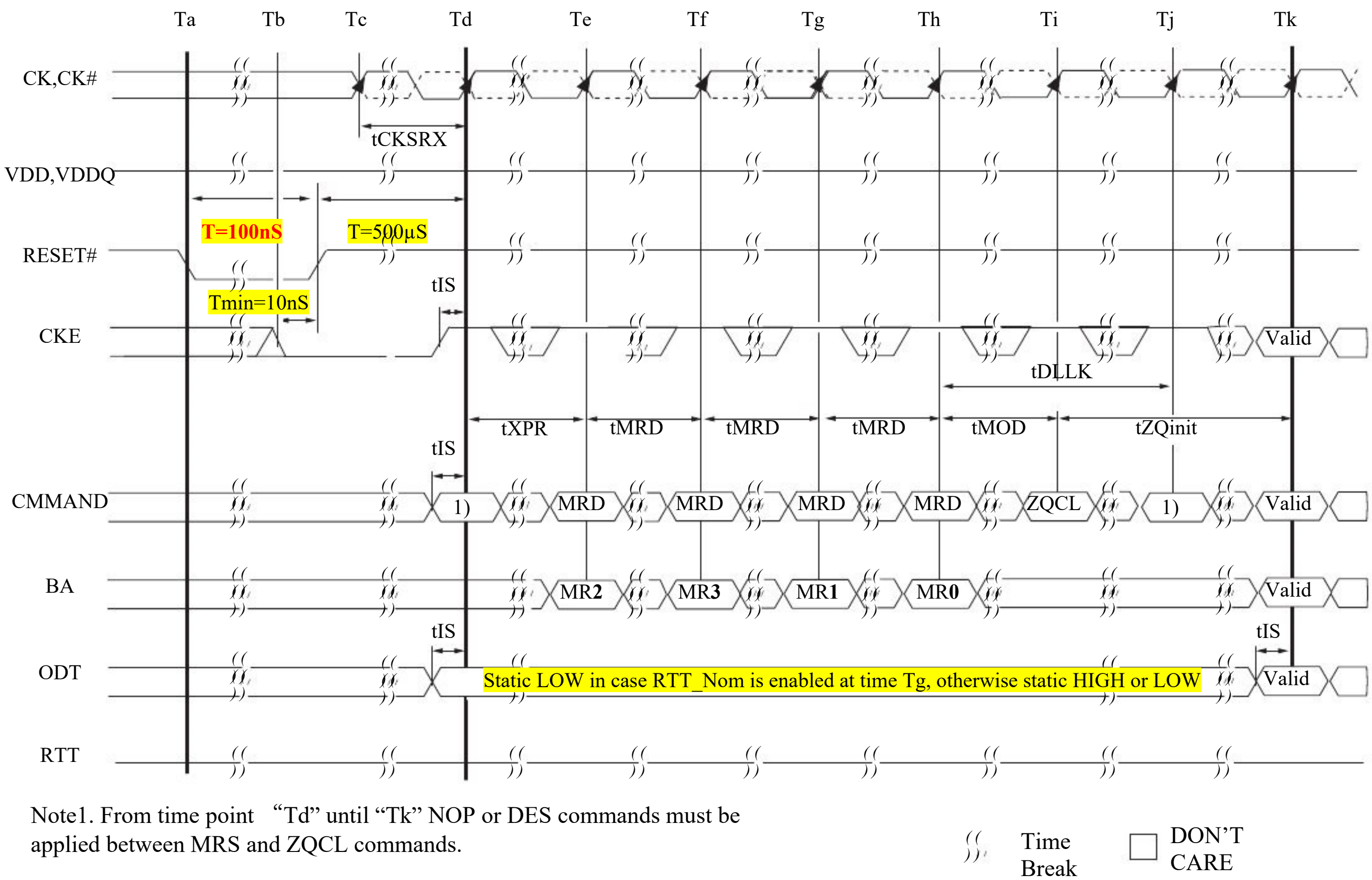


Figure2.1.2 Reset Procedure at Power Stable Condition

2.3 Register Definition

2.3.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.

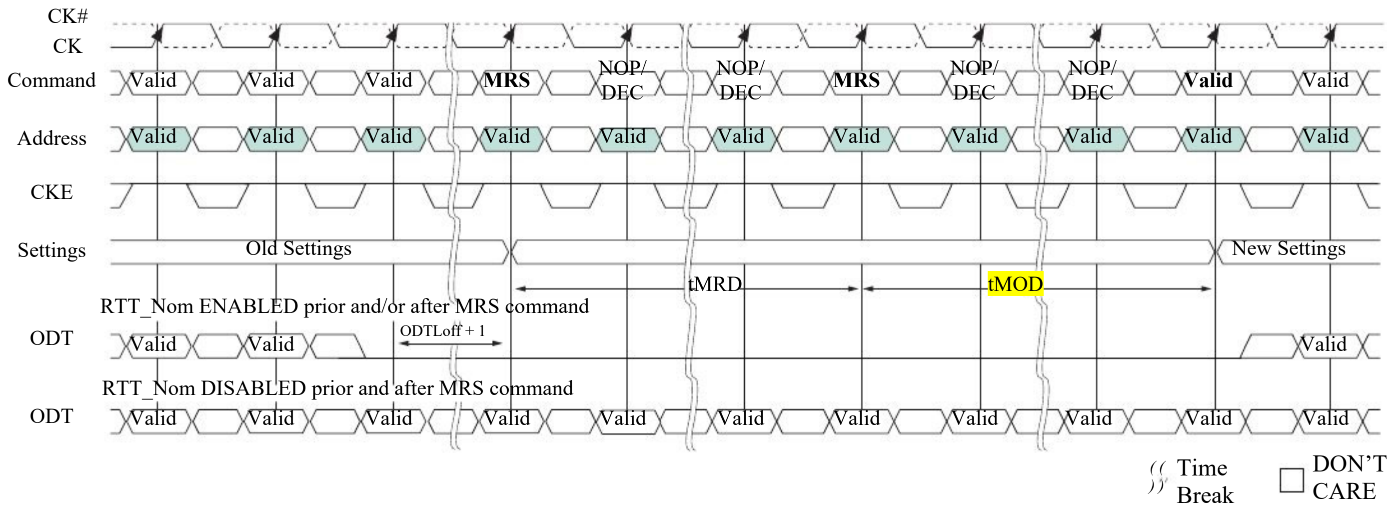


Figure2.3.1a tMRD Timing

The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.

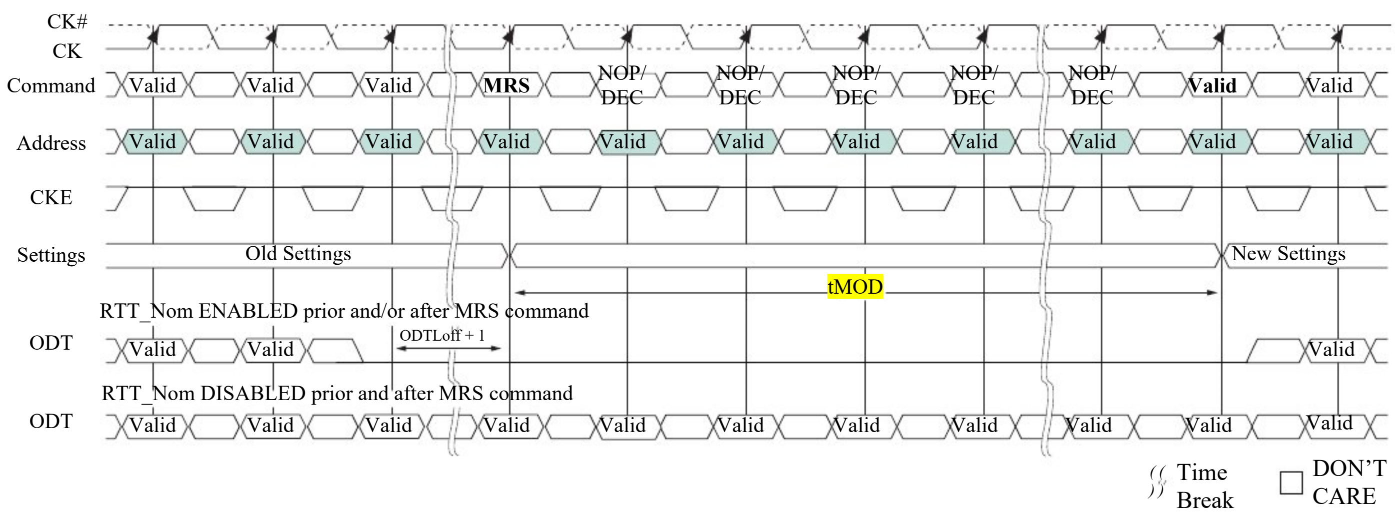


Figure 2.3.1b tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal maybe registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

2.3.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	0	0	**0*1**	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL		Mode Register 0

A8	DLL Reset
0	No
1	Yes

A7	mode
0	Nomal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

BA1	BA0	MR Select
0	**0**	**MR0**
0	1	MR1
1	0	MR2
1	1	MR3

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

1. A15,A14 and A13 must be programmed to 0 during MRS.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency
4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Figure 2.3.2 — MR0 Definition

2.3.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 2.3.2. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table below. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		10	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		11	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		100	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		101	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		110	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		111	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		10	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		11	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		101	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		110	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		111	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

2.3.2.2 CAS Latency
The CAS Latency is defined by MR0 (bits A2 and A4-A6) as shown in Figure 2.3.2. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins".

2.3.2.3 Test Mode
The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 2.3.2. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

2.3.2.4 DLL Reset
The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

2.3.2.5 Write Recovery
The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

2.3.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

2.3.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 2.3.3.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	0	**1**	**0*1**	Qoff	TDQS	**0*1**	Rtt	**0*1**	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL	Mode Register 1

A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom *3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 Ω
*3:In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
*4:If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

A0	DLL Enable
0	Enable
1	Disable

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, DQS#s.

BA1	BA0	MR Select
0	0	MR0
0	**1**	**MR1**
1	0	MR2
1	1	MR3

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

* 1 : A8, A10, A13, A14, and A15 must be programmed to 0 during MRS.
* TDQS must be disabled for x16 option.

Figure 2.3.3 MR1 Definition

2.3.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode”.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

2.3.3.2 Output Driver Impedance Control
The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 2.3.3.

2.3.3.3 ODT Rtt Values
DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

2.3.3.4 Additive Latency (AL)
Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table below.

A4	A3	Additive Latency (AL) Settings
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

NOTE: AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

2.3.3.5 Write leveling
For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew.

2.3.3.6 Output Disable
The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 2.3.3. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to ‘0’.

2.3.3.7 TDQS, TDQS#
TDQS (Termination Data Strobe) is a feature of X8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations. The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X16 configuration.

2.3.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the below.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	1	0	0*1			Rtt_WR		0*1	SRT	ASR	CWL			PASR			Mode Register 2

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended operating temperature range

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A2	A1	A0	Partial Array Self-Refresh
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5 ns)
0	0	1	6 (2.5 ns > tCK(avg) ≥ 1.875 ns)
0	1	0	7 (1.875 ns > tCK(avg) ≥ 1.5 ns)
0	1	1	8 (1.5 ns > tCK(avg) ≥ 1.25 ns)
1	0	0	9 (1.25 ns > tCK(avg) ≥ 1.07ns)
1	0	1	10 (1.07 ns > tCK(avg) ≥ 0.935 ns)
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	**0**	**MR2**
1	1	MR3

* 1 : A5, A8, A11 ~ A15 must be programmed to 0 during MRS.
* 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Figure 2.3.4 MR2 Definition

2.3.4.1 Partial Array Self-Refresh (PASR)

If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 2.3.4 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

2.3.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 2.3.4. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins”.

2.3.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

For more details refer to “Extended Temperature Usage”. DDR3 SDRAMs support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

2.3.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT”.

2.3.5 Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the below.

BA2	BA1	BA0	A15-A10	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	1	1	**0*1**	**ECC Register Select* 1**										MPR			Mode Register 3

MRP Operation

A2	MPR
0	Normal operation *1
1	Dataflow from MPR or ECC Register Access

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	**1**	**MR3**

MPR Access

A4	A3	A2	A1	A0	MPR Acccess
0	0	1	X	X	Select “Predefined Pattern”*2
0	1	1	0	0	Read ECC Register 0
0	1	1	0	1	Read ECC Register 1
0	1	1	1	0	Read ECC Register 2
0	1	1	1	1	Read ECC Register 3
1	0	1	0	0	Read ECC Register 4
1	0	1	0	1	Read ECC Register 5
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Write ECC Register 5

* 1 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored, and A3-A15 must be programmed to 0.
* 2 : The predefined pattern will be used for read synchronization.
* 3 : The ECC Register access is further described in Section 10.2.

Figure 2.3.5 MR3 Definition

2.3.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence, or access the ECC Registers (see Section 10.2). The basic concept of the MPR is shown in Figure 2.3.5.1.

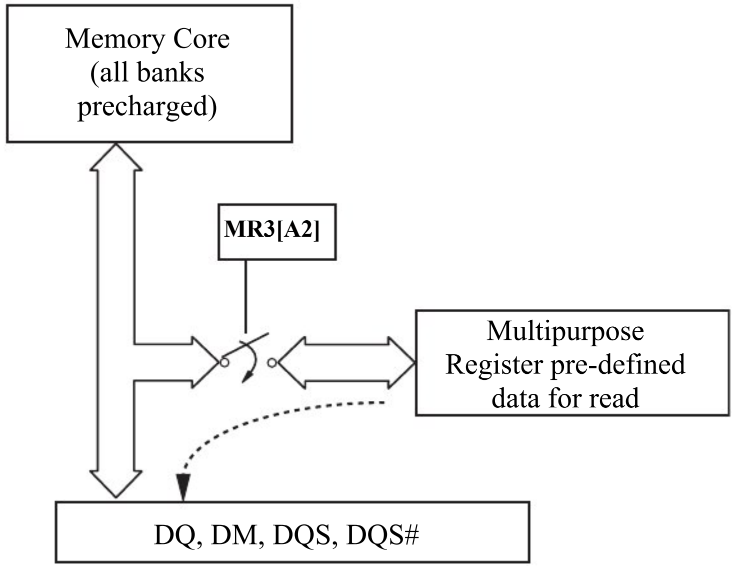


Figure 2.3.5.1 MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register.

The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0).

Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don’t care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See MPR Definition table	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Register Address Definition

The following Table provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read predefined pattern for system Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

NOTE: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent

MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x16:
  - DQL[0] and DQU[0] drive information from MPR.
  - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order: 4,5,6,7 *)
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11, A13, A14, A15: don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

NOTE: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.
NOTE: Good reference for the example of MPR feature is the JEDEC standard No.93-3D, 4.10.4 Protocol example.

Relevant Timing Parameters

AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing

2.4 DDR3 SDRAM Command Description and Operation

2.4.1 Command Truth Table

[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

Function	Abbrev.	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A11, A13 A14 A15	A12/ BC#	A10 /AP	A0 - A9	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address(RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

2.4.1. CKE Truth Table

Current State[2]	CKE		Command (N)[3] RAS#, CAS#, WE#, CS#	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1](N)			
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Bank Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9.13.18

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh cannot be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

2.4.2 No Operation (NOP) Command

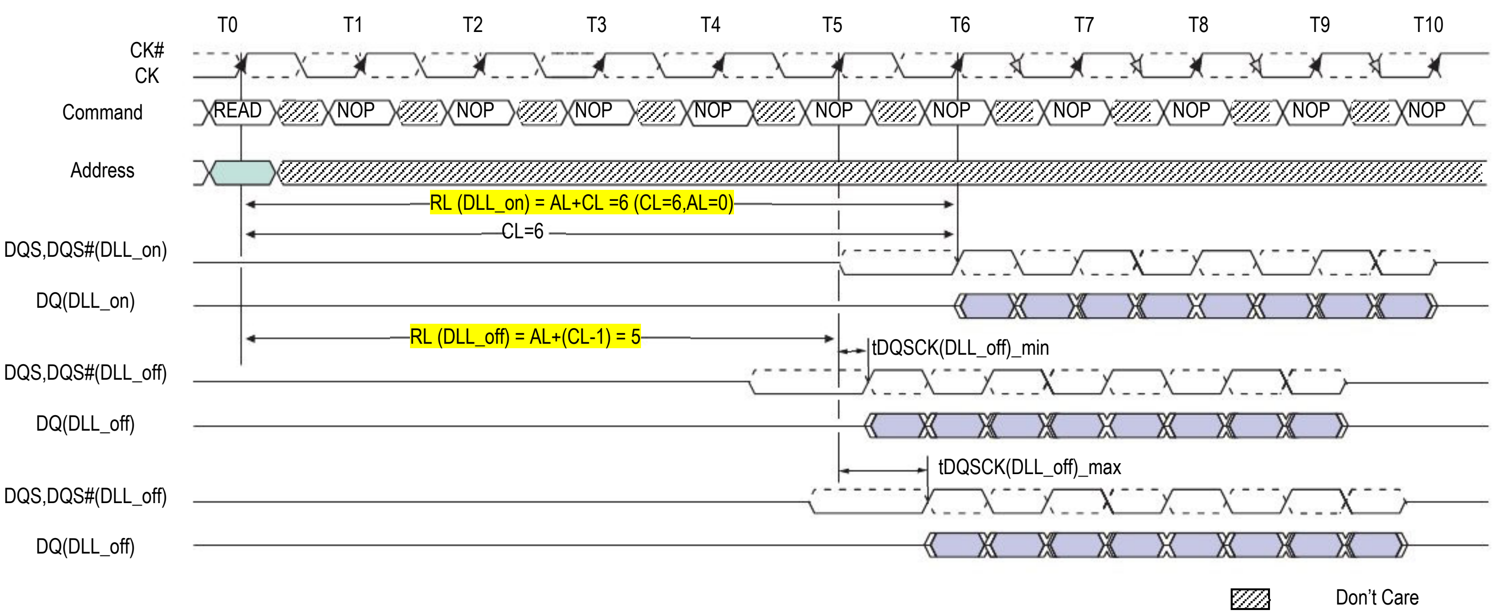
The No operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# low and RAS#,CAS#,WE# high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.4.3 Deselect(DES) Command

The Deselect function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.4.4 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI. Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6. DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.
Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. The timing relations on DLL-off mode READ operation have shown at the following Timing Diagram (CL=6, BL=8)



Note: The tDQSCK is used here for DQS, DQS, and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ, DQS, and DQS# signals will still be tDQSQ.

Figure 2.4.4 DLL-off mode READ Timing Operation

2.4.5 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operation until A0 bit set back to “0”.

2.4.5.1 DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires te frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timing fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).
2. Set MR1 Bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, and then set Mode Registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, and then DRAM is ready for next command.

2.4.5.2 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change".
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to “0” to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

2.4.6. Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.
The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met.

The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to “DLL on/off switching procedure”.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

2.4.7 Write leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew.

The memory controller can use the ‘write leveling’ feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification.

Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 2.4.7.

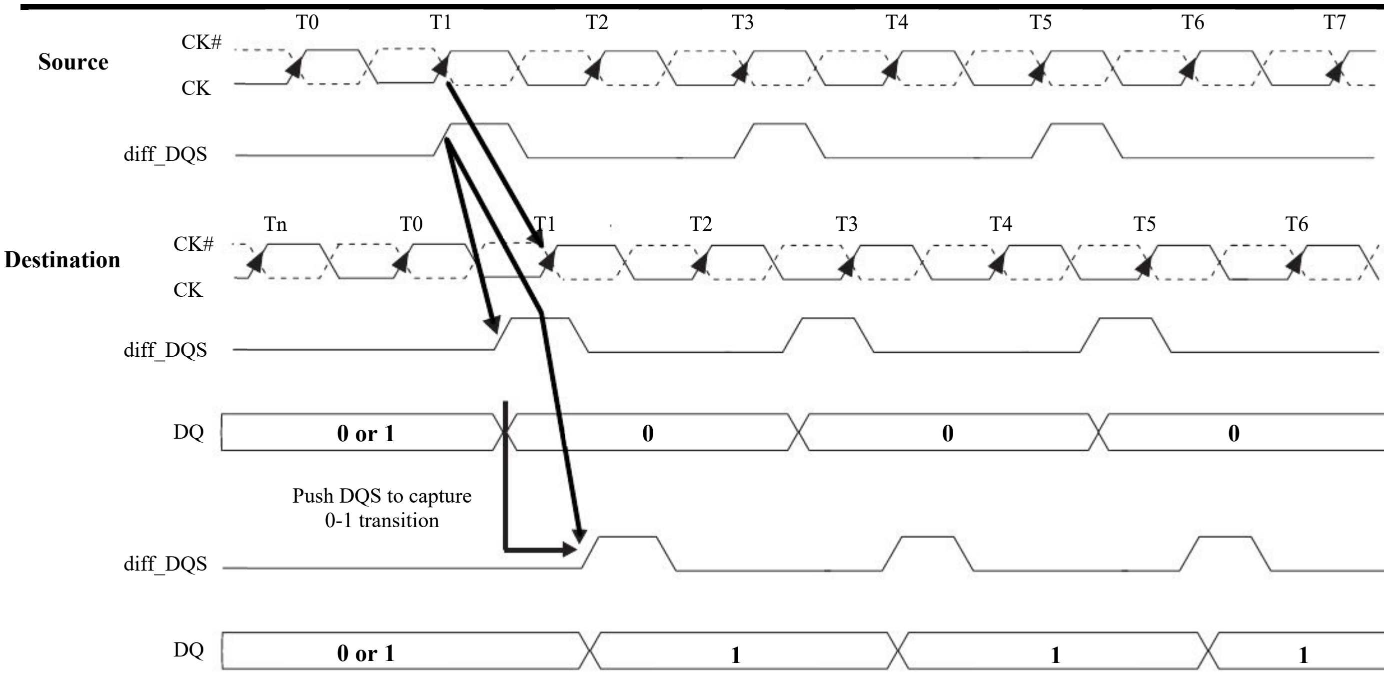


Figure 2.4.7 Write Leveling Concept

DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits carry the leveling feedback to the controller across the DRAM configurations X8 and X16. On a X16 device, both byte lanes should be leveled independently.

Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

2.4.7.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low'. Note that in write leveling mode, only DQS/DQS# terminations are activated and deactivated via ODT pin, unlike normal operation.

MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/DQS# termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

NOTE: In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

2.4.7.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1.
The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on the DQ bus asynchronously after tWLO timing. In this product, all data bits, which are DQ0~DQ7 for x8, or DQ0~DQ15 for x16 provide the leveling feedback. (Note: It is recommended the Controller rely solely on DQ0 for x8, or DQ0 and DQ8 for x16 for the prime DQ bits to maintain the broadest industry compatibility). There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Figure 2.4.7.2 describes the timing diagram and parameters for the overall Write Leveling procedure.

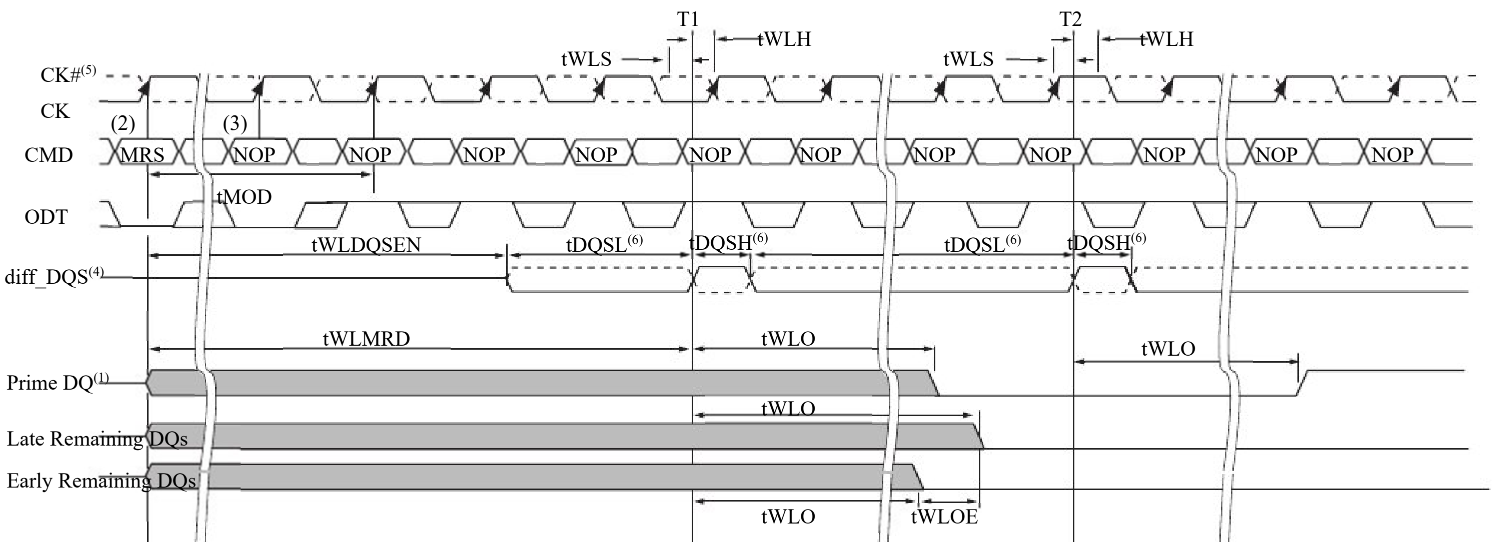


Figure 2.4.7.2 Write leveling sequence [DQS - DQS# is capturing CK-CK# low at T1 and CK-CK# high at T2]

Notes:
1. The JEDEC specification for DDR3 DRAM has the option to drive leveling feedback on a single prime DQ or all DQs. For best compatibility with future DDR3 products, applications should use the lowest order DQ for each byte lane (DQ0 for x8, or DQ0 and DQ8 for x16).
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

2.4.7.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge, stop driving the strobe signals. Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command.
2. Drive ODT pin low (tIS must be satisfied) and continue registering low.
3. After the RTT is switched off, disable Write Level Mode via MRS command.
4. After tMOD is satisfied, any valid command may be registered. (MR commands may be issued after tMRD).

2.4.8 Extended Temperature Usage

a. Auto Self-refresh supported
b. Extended Temperature Range supported
c. Double refresh required for operation in the Extended Temperature Range (applies only for devices supporting the Extended Temperature Range)

Mode Register Description

Field	Bits	Description
ASR	MR2 (A6)	**Auto Self-Refresh (ASR)** when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation 0 = Manual SR Reference (SRT) 1 = ASR enable
SRT	MR2 (A7)	**Self-Refresh Temperature (SRT) Range** If ASR = 0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended operating temperature range

2.4.8.1 Auto Self-Refresh mode - ASR Mode

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1b and MR2 bit A7 = 0b. The DRAM will manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0b.

If the ASR mode is not enabled (MR2 bit.A6 = 0b), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range. Refer to operating temperature range for restrictions on operating conditions.

2.4.8.2 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = 0b, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = 0b, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = 1b then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.
For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0b and the DRAM should not be operated outside the Normal Temperature Range.

Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 to 85 °C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal (0 to 85 °C) and Extended (85 to 105°C)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 to 85 °C)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 to 85 °C) and Extended (85 to 105°C)
1	1	Illegal	

Note: Self-Refresh Mode operation above 95° C permitted only for Automotive grade (A2); refer to 3.2 Component Operating Temperature Range.

2.5 ECC Function

The DRAM has an error correcting feature which reduces the likelihood of occurrences of bit errors. When carrying out a Write command for an address location, the ECC module uses the data in the burst to calculate an additional set of ECC bits that are stored in the DRAM memory in a location adjacent to the data. When later carrying out a Read command for that same location, the ECC module analyzes and compares the data from memory and the ECC bits. If a bit had changed its value within 4-bits of the stored data, that bit will have a corrected value during the Read burst. If more than one bit had changed value with 4-bits of the stored data, the ECC feature cannot correct all the bits during the Read burst. The ECC function is further described in Section 10.

3. Absolute Maximum Ratings and AC & DC Operating Conditions

3.1 Absolute Maximum DC Ratings.

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VIN, VOUT	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
TSTG	Storage Temperature	-55 to +150	°C	1,2

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

3.2 Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Commercial	Tc = 0 to 85	°C	1,2
		Tc = 85 to 95	°C	1,3
	Industrial	Tc = -40 to 85	°C	1,2
		Tc = 85 to 95	°C	1,3
	Automotive (A1)	Tc = -40 to 85	°C	1,2
		Tc = 85 to 95	°C	1,3
	Automotive (A2)	Tc = -40 to 85	°C	1,2
		Tc = 85 to 105	°C	1,3
	Automotive (A25)	Tc = -40 to 85	°C	1,2
		Tc = 85 to 105	°C	1,3
		Tc = 105 to 115	°C	1,4
	Automotive (A3)	Tc = -40 to 85	°C	1,2
		Tc = 85 to 105	°C	1,3
		Tc = 105 to 125	°C	1,4

Notes:
1. Operating Temperature TOPER is the case surface temperature (Tc) on the center / top side of the DRAM.
2. This temperature range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained in this range under all operating conditions.
3. Some applications require operation of the DRAM in an elevated temperature range. For each permitted temperature range, full specifications are supported, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval (tREFI) to the value specified in Table 8.2.
   b) If Self-Refresh operation is used in this range, it is mandatory to use either the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).
4. Same as note 3, except part (b). *No type of Self-Refresh is supported for this range*.

3.3 Recommended DC Operating Conditions

Symbol	Parameter		Rating Min	Rating Typ	Rating Max	Unit	Notes
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6,7
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6,7

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDD (t) over a long period of time.
4. If the maximum limit is exceeded, the input levels are covered by the DDR3 specification.
5. With these supply voltages, the device operates with DDR3L specifications.
6. After initialized for DDR3 operation, the DDR3L may be used only upon reset.
7. The DDR3L product supports 1.5V operation, and if initialized as such, retains the original speed timing defined for DDR3L speed.

3.4. Thermal Resistance

Package	Substrate	Theta-ja (Airflow = 0m/s)	Theta-ja (Airflow = 1m/s)	Theta-ja (Airflow = 2m/s)	Theta-jc	Units
78-ball	4-layer	31.5	27.1	24.5	2.6	C/W
96-ball	4-layer	29.4	25.2	22.8	2.6	C/W

4. AC & DC INPUT MEASUREMENT LEVELS

4.1. AC and DC Logic Input Levels for Single-Ended Signals

4.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units	Note
		Min.	Max.	Min.	Max.	V	1
VIH.CA(DC100)	DC input logic high	Vref + 0.100	V_{DD}	Vref + 0.100	V_{DD}	V	1
VIL.CA(DC100)	DC input logic low	V_{SS}	Vref - 0.100	V_{SS}	Vref - 0.100	V	1, 2, 5
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2	--	--	V	1, 2, 5
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175	--	--	V	1, 2, 5
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note2	--	--	V	1, 2, 5
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150	--	--	V	1, 2, 5
VIH.CA(AC135)	AC input logic high	--	--	Vref + 0.135	Note2	V	1, 2, 5
VIL.CA(AC135)	AC input logic low	--	--	Note2	Vref - 0.135	V	1, 2, 5
VIH.CA(AC125)	AC input logic high	--	--	Vref + 0.125	Note2	V	1, 2, 5
VIL.CA(AC125)	AC input logic low	--	--	Note2	Vref - 0.125	V	1, 2, 5
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	V	3, 4

Symbol	Parameter	DDR3L-800/1066/1333/1600		DDR3L-1866		Units	Note
		Min.	Max.	Min.	Max.	V	1
VIH.CA(DC90)	DC input logic high	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	V	1
VIL.CA(DC90)	DC input logic low	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V	1, 2, 5
VIH.CA(AC160)	AC input logic high	Vref + 0.16	Note2	--	--	V	1, 2, 5
VIL.CA(AC160)	AC input logic low	Note2	Vref - 0.160	--	--	V	1, 2, 5
VIH.CA(AC135)	AC input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1, 2, 5
VIL.CA(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1, 2, 5
VIH.CA(AC125)	AC input logic high	--	--	Vref + 0.125	Note2	V	1, 2, 5
VIL.CA(AC125)	AC input logic low	--	--	Note2	Vref - 0.125	V	1, 2, 5
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	V	3, 4

Notes:
1. For input only pins except RESET.Vref=VrefCA(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 1.0% VDD.
4. For reference: DDR3 has approx. V_{DD}/2 +/- 15mV, DDR3L has approx V_{DD}/2 +/- 13.5mV.
5. To allow VREFCA margining, all DRAM Command and Address Input Buffers MUST use external VREF (provided by system) as the input for their VREFCA pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Command and Address input buffer

4.1.2 AC and DC Logic Input Levels for Single-Ended Signals & DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	V	1
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	V_{DD}	Vref + 0.100	V_{DD}	Vref + 0.100	V_{DD}	V	1
VIL.DQ(DC100)	DC input logic low	V_{SS}	Vref - 0.100	V_{SS}	Vref - 0.100	V_{SS}	Vref - 0.100	V	1, 2, 5
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	Note2	--	--	--	--	V	1, 2, 5
VIL.DQ(AC175)	AC input logic low	Note2	Vref - 0.175	--	--	--	--	V	1, 2, 5
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note2	Vref + 0.150	Note2	--	--	V	1, 2, 5
VIL.DQ(AC150)	AC input logic low	Note2	Vref - 0.150	Note2	Vref - 0.150	--	--	V	1, 2, 5
VIH.DQ(AC135)	AC input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1, 2, 5
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	V	3, 4

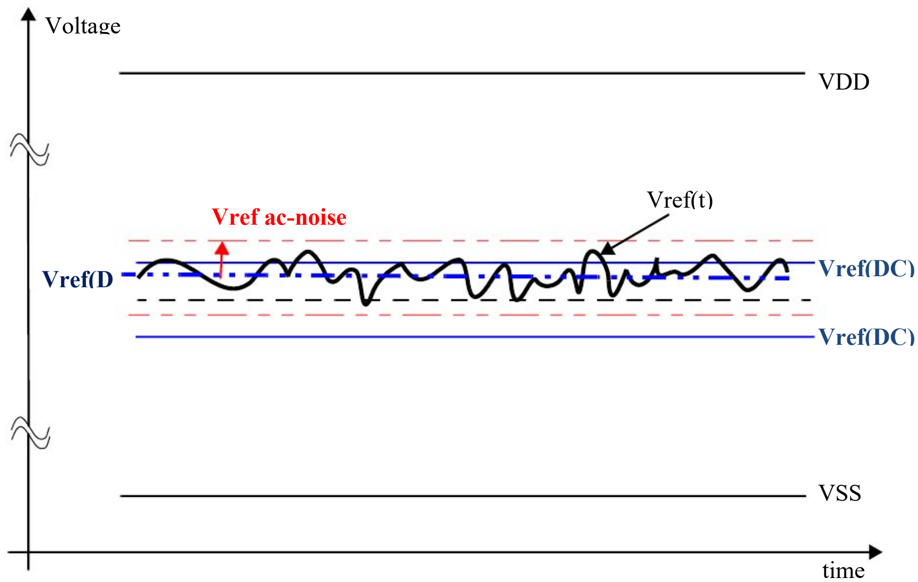
Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	V	1
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	V	1
VIL.DQ(DC90)	DC input logic low	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V	1, 2, 5
VIH.DQ(AC160)	AC input logic high	Vref + 0.16	Note2	Vref + 0.16	Note2	--	--	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note2	Vref - 0.16	Note2	Vref - 0.16	--	--	V	1, 2, 5
VIH.DQ(AC135)	AC input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1, 2, 5
VIH.DQ(AC130)	AC input logic high	--	--	--	--	Vref + 0.13	Note2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	--	--	--	--	Note2	Vref - 0.13	V	1, 2, 5
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	0.49 * V_{DD}	0.51* V_{DD}	V	3, 4

Notes:
1. For input only pins except RESET#. Vref = VrefDQ(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than ± 1.0% VDD.
4. For reference: DDR3 has approx. VDD/2 ±15mV, and DDR3L has approx. V_{DD}/2 ± 13.5mV.
5. Single-ended swing requirement for DQS-DQS#, is 350mV (peak to peak). Differential swing requirement for DQS-DQS#, is 700mV (peak to peak)

4.2 Vref Tolerances

The dc-tolerance limits and ac-moist limits for the reference voltages VrefCA and VrefDQ are illustrated in the following figure. It shows a valid reference voltage Vref(t) as a function of time. (Vref stands for VrefCA and VrefDQ likewise).
Vref(DC) is the linear average of Vref(t) over a very long period of time (e.g.,1 sec). This average has to meet the min/max requirement in previous page. Furthermore Vref(t) may temporarily deviate from Vref(DC) by no more than ±1% VDD.
The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on Vref. "Vref" shall be understood as Vref(DC). The clarifies that dc-variations of Vref affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for Vref(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and de-rating values need to include time and voltage associated with Vref ac-noise. Timing and voltage effects due to ac-noise on Vref up to the specified limit (±1% of VDD) are included in DRAM timing and their associated de-ratings.

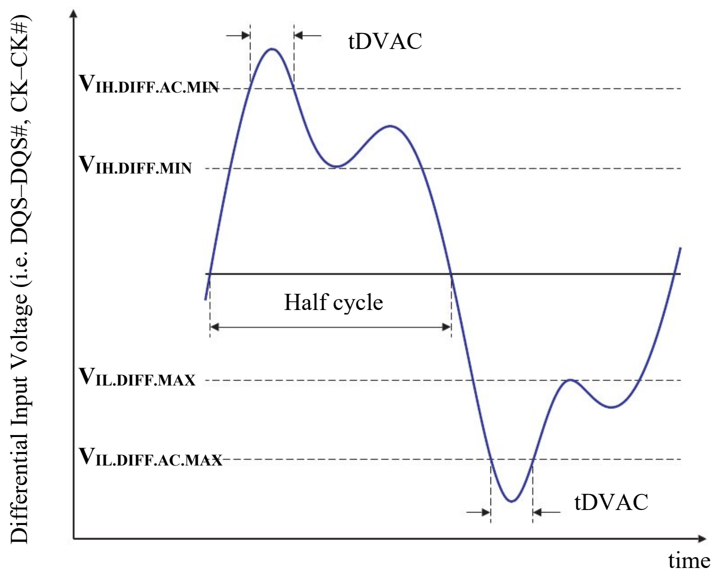
Figure 4.2 Illustration of Vref(DC) tolerance and Vrefac-noise limits



4.3. AC and DC Logic Input Levels for Differential Signals

4.3.1 Differential signal definition

Figure 4.3.1 Definition of differential ac-swing and "time above ac-level"



4.3.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

4.3.2.1 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800, 1066, 1333, 1600, 1866, 2133		unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+0.200	Note3	V	1
VILdiff	Differential input logic low	Note3	-0.200	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
VILdiff(ac)	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+0.180	Note3	V	1
VILdiff	Differential input logic low	Note3	-0.180	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
VILdiff(ac)	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2

Notes:
1. Used to define a differential signal slew-rate.
2. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.3.2.2 Minimum required time before ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/ns]	DDR3-800/1066/1333/1600			DDR3-1866/2133	
	tDVAC [ps] @ |VIH/Ldiff(AC)| = 350mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 300mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = (DQS - DQS#) only	tDVAC [ps] @ |VIH/Ldiff(AC)| = 300mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = (CK - CK#) only
> 4.0	75	175	214	134	139
4	57	170	214	134	139
3	50	167	191	112	118
2	38	119	146	67	77
1.8	34	102	131	52	63
1.6	29	81	113	33	45
1.4	22	54	88	9	23
1.2	Note	19	56	Note	Note
1	Note	Note	11	Note	Note
< 1	Note	Note	Note	Note	Note

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600		DDR3L-1866		
	tDVAC [ps] @ |VIH/Ldiff(AC)| = 320mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 270mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 270mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 250mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 260mV
> 4.0	189	201	163	168	176
4	189	201	163	168	176
3	162	179	140	147	154
2	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	56
1.2	Note	44	5	22	24
1	Note	Note	Note	Note	Note
< 1	Note	Note	Note	Note	Note

Note: The rising input differential signal shall become equal to or greater than VIHdiff(ac) level; and the falling input differential signal shall become equal to or less than VILdiff(ac) level.

4.3.3. Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.
CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

4.3.3.1. Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3/DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
VSEH	Single-ended high-level for strobes	(VDDQ/2) + 0.175	note3	V	1, 2
	Single-ended high-level for CK, CK	(VDD/2) + 0.175	note3	V	1, 2
VSEL	Single-ended low-level for strobes	note3	(VDDQ/2) - 0.175	V	1, 2
	Single-ended Low-level for CK, CK	note3	(VDD/2) - 0.175	V	1, 2

Notes:
1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

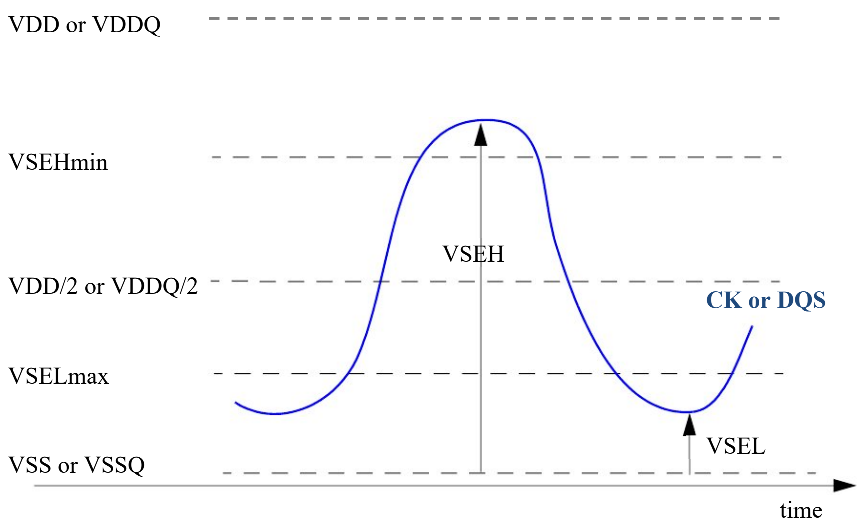


Figure 4.3.3 Single-ended requirement for differential signals.

4.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK and DQS, DQS) must meet the requirements in the following table. The differential input cross point voltage Vix is measured from the actual cross point of true and completement signal to the midlevel between of VDD and VSS.

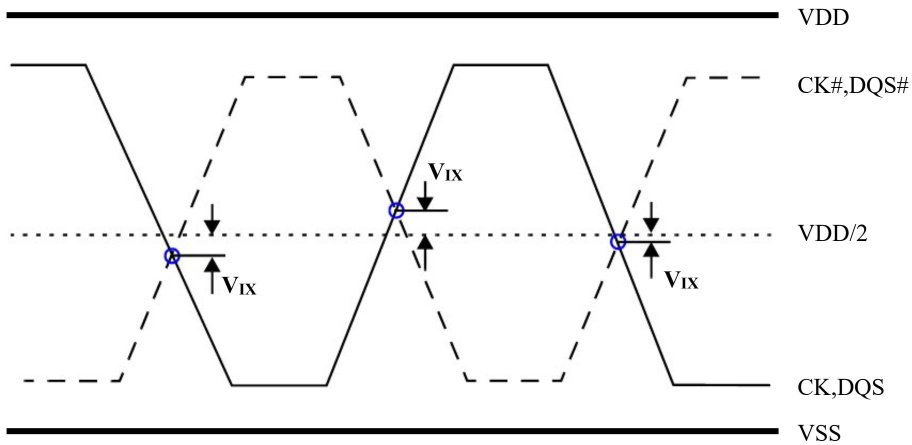


Figure 4.4. Vix Definition

4.4.1 Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter		DDR3/DDR3L-800, 1066, 1333, 1600, 1866, 2133		Unit	Note
			Min.	Max.		
Vix	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK	DDR3	-150	150	mV	2
			-175	175	mV	1
		DDR3L	-150	150	mV	2
	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS	DDR3	-150	150	mV	2
		DDR3L	-150	150	mV	2

Notes:

1. Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/ns.
2. The following must be true: $(V_{DD}/2) + Vix(min) – V_{SEL} \geq 25$ mV and $V_{SEH} – ((V_{DD}/2) + Vix\ (max.)) \geq 25$mV.

4.5 Slew Rate Definitions for Single-Ended Input Signals

See “Address / Command Setup, Hold and Derating” for single-ended slew rate definitions for address and command signals.
See “Data Setup, Hold and Slew Rate Derating” for single-ended slew rate definitions for data signals.

4.6. Slew Rate Definition for Differential Input Signals

4.6.1 Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-CK# & DQS-DQS#)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-CK# & DQS-DQS#)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff

Note : The differential signal (i.e., CK-CK# & DQS-DQS#) must be linear between these thresholds.

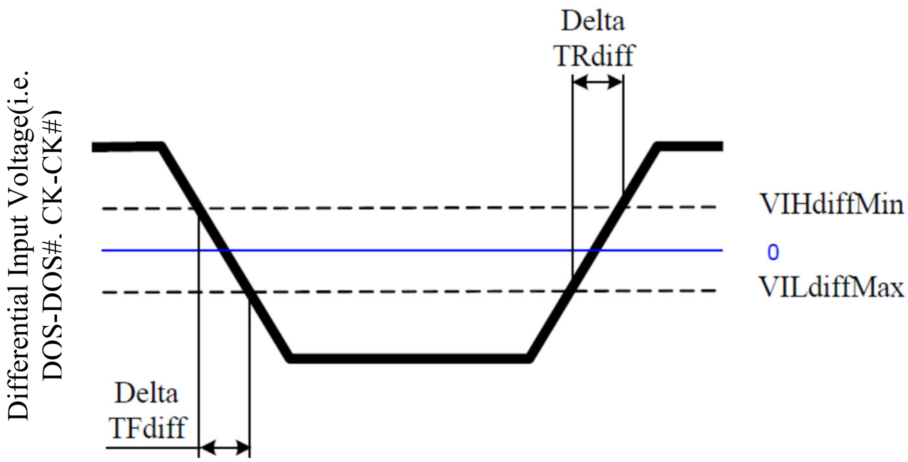


Figure 4.6.1 Input Nominal Slew Rate Definition for DQS, DQS# and CK, CK#

5. AC AND DC OUTPUT MEASUREMENT LEVELS

5.1 Single Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8xVDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5xVDDQ	V	
VOL(DC)	DC output low measurement level (fro IV curve linearity)	0.2xVDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT+0.1xVDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT-0.1xVDDQ	V	1

NOTE 1. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2.

5.2 Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

NOTE 1. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

5.3 Single Ended Output Slew Rate

5.3.1 Single Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / DeltaTRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / DeltaTFse

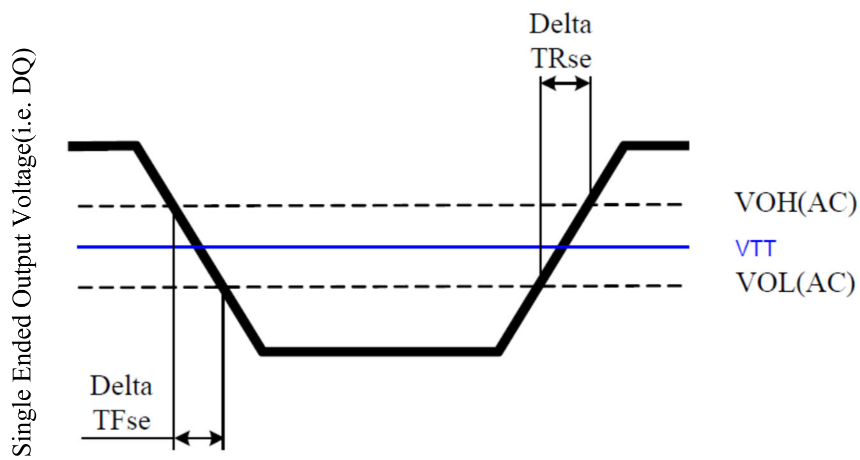


Figure 5.3.1 Single Ended Output Slew Rate Definition

5.3.2 Output Slew Rate (single-ended)

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Unit
			Min.	Max.	Min.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	
Single-ended Output Slew Rate	DDR3	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5	V/ns
	DDR3L		1.75	5	1.75	5	1.75	5	1.75	5	1.75	5	1.75	5	

Note: SR: Slew Rate. Q: Query Output (like in DQ, which stands for Data-in, Query -Output). se: Single-ended signals. For Ron = RZQ/7 setting.

5.4 Differential Output Slew Rate

5.4.1 Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)]/DeltaTRdiff
Differential output slew rate for falling	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)]/DeltaTFdiff

Note: Output slew rate is verified by design and characterization, and not 100% tested in production.

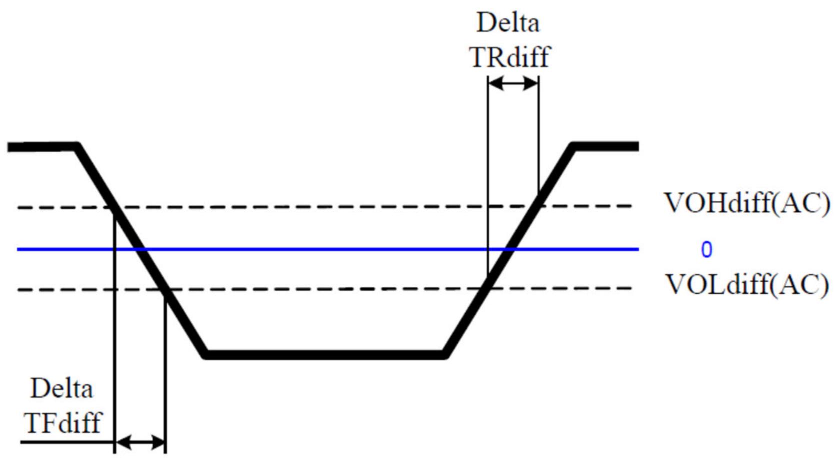


Figure 5.4.1 Differential Output Slew Rate Definition

5.4.2 Differential Output Slew Rate

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Unit
			Min.	Max.	Min.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	
Differential Output Slew Rate	DDR3	SRQdiff	5	10	5	10	5	10	5	10	5	10	5	10	V/ns
	DDR3L		3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	

Description: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals, For Ron = RZQ/7 setting

5.5 Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements. It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

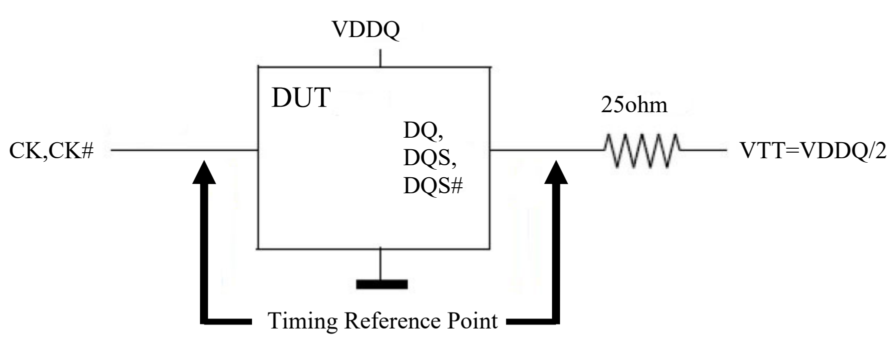


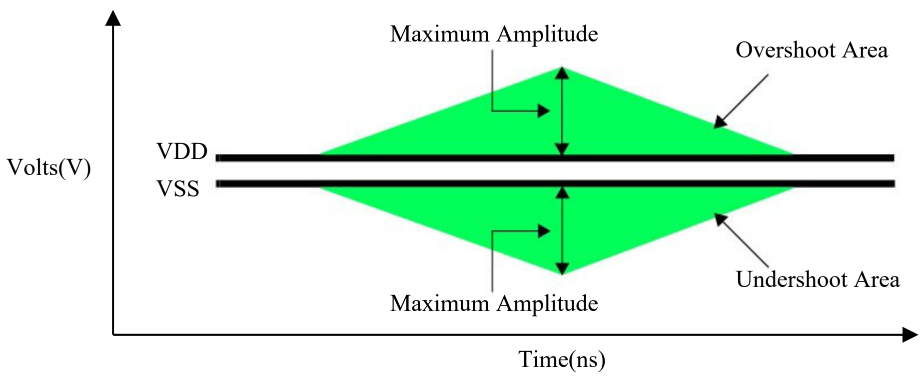
Figure 5.5 Reference Load for AC Timing and Output Slew Rate

5.6 Overshoot and Undershoot Specifications

5.6.1 AC Overshoot/Undershoot Specification for Address and Control Pins

Item	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
undershoot area below VSS	0.67	0.5	0.4	0.33	0.28	0.25	V-ns

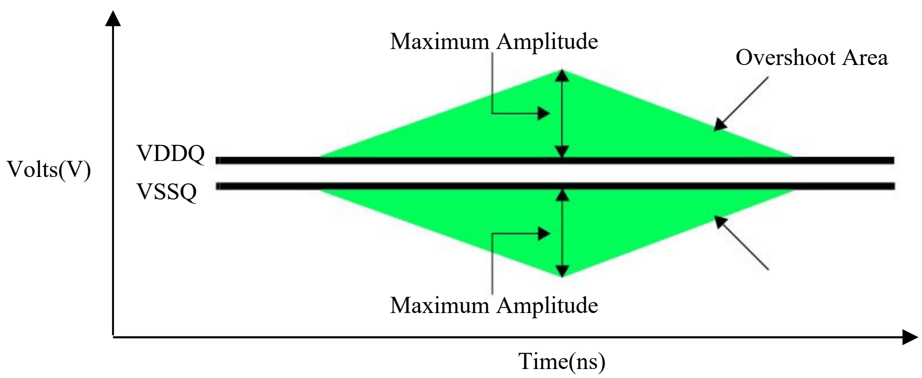
Note : A0-A13, BA0-BA2, CS#, RAS#, CAS#, WE#, CKE, ODT



5.6.2 AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask

Item	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
undershoot area below VSS	0.25	0.19	0.15	0.13	0.11	0.10	V-ns

Note : CK, CK#, DQ, DQS, DQS#, DM



5.7 34Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value ofthe external reference resistor RZQ as follows:

RON34 = RZQ / 7 (nominal 34.4ohms +/-10% with nominal RZQ=240ohms)

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

RONPu = [VDDQ-Vout] / | Iout | ------------------- under the condition that RONPd is turned off (1)

RONPd = Vout / | Iout | -------------------------------under the condition that RONPu is turned off (2)

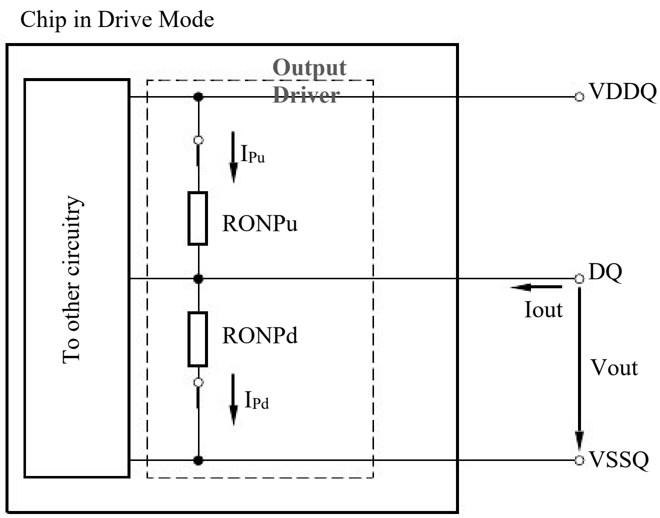


Figure 5.7 Output Driver : Definition of Voltages and Currents

5.7.1 Output Driver DC Electrical Characteristics

DDR3 (assuming 1.5V, RZQ = 240ohms; entire operating temperature range; after proper ZQ calibration)

RONNom	Resistor	Vout	Min	Nom	Max	Unit	Notes
34 ohms	RON34Pd	VOLdc=0.2xVDDQ	0.6	1	1.1	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/7	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.4	RZQ/7	1,2,3
	RON34Pu	VOLdc=0.2xVDDQ	0.9	1	1.4	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/7	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.1	RZQ/7	1,2,3
40 ohms	RON40Pd	VOLdc=0.2xVDDQ	0.6	1	1.1	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/6	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.4	RZQ/6	1,2,3
	RON40Pu	VOLdc=0.2xVDDQ	0.9	1	1.4	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/6	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.1	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.5xVDDQ	-10		+10	%	1,2,4

DDR3L (assuming 1.35V, RZQ = 240ohms; entire operating temperature range; after proper ZQ calibration)

RONNom	Resistor	Vout	Min	Nom	Max	Unit	Notes
34 ohms	RON34Pd	VOLdc=0.2xVDDQ	0.6	1	1.15	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/7	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.45	RZQ/7	1,2,3
	RON34Pu	VOLdc=0.2xVDDQ	0.9	1	1.45	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/7	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.15	RZQ/7	1,2,3
40 ohms	RON40Pd	VOLdc=0.2xVDDQ	0.6	1	1.15	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/6	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.45	RZQ/6	1,2,3
	RON40Pu	VOLdc=0.2xVDDQ	0.9	1	1.45	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/6	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.15	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.5xVDDQ	-10		+10	%	1,2,4

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ=VDD and that VSSQ=VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5xVDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 * VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
   Measure RONPu and RONPd, both at 0.5 x VDDQ:
   MMPuPd = [RONPu - RONPd] / RONNom x 100

5.7.2 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table below.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

5.7.2.1 Output Driver Sensitivity Definition

Items	Min.	Max.	Unit
RONPU@VOHdc	0.6 - dRONdTH*lDelta Tl - dRONdVH*lDelta Vl	1.1 + dRONdTH*lDelta Tl - dRONdVH*lDelta Vl	RZQ/7
RON@VOMdc	0.9 - dRONdTM*lDelta Tl - dRONdVM*lDelta Vl	1.1 + dRONdTM*lDelta Tl - dRONdVM*lDelta Vl	RZQ/7
RONPD@VOLdc	0.6 - dRONdTL*lDelta Tl - dRONdVL*lDelta Vl	1.1 + dRONdTL*lDelta Tl - dRONdVL*lDelta Vl	RZQ/7

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

5.7.2.2 Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-800/1066/1333		DDR3-1600/1866/2133		Unit
Items	Min.	Max	Min.	Max	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.15	0	0.13	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.15	0	0.13	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.15	0	0.13	%/mV

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

5.8 On-Die Termination (ODT) Levels and I-V Characteristics

5.8.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6, and A2 of the MR1 Register.
ODT is applied to the DQ, DM, DQS/DQS, and TDQS/TDQS (x8 devices only) pins.
A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:
RTTPu = [VDDQ - Vout] / | Iout | ------------------ under the condition that RTTPd is turned off (3)
RTTPd = Vout / | Iout | ------------------------------ under the condition that RTTPu is turned off (4)

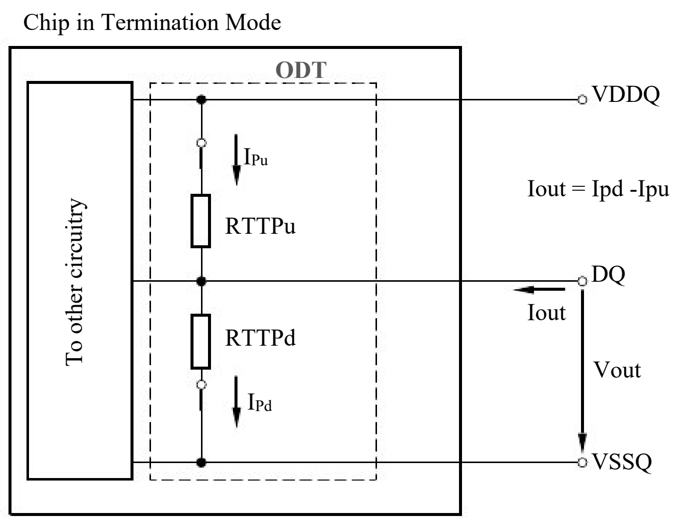


Figure 5.8.1 On-Die Termination : Definition of Voltages and Currents

5.8.2 ODT DC Electrical Characteristics

The following table provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics

(assuming RZQ = 240ohms +/- 1% entire operating temperature range; after proper ZQ calibration)

MR1 A9, A6, A2	RTT	Resistor	Vout	Min	Nom	Max (DDR3)	Max (DDR3L)	Unit	Notes
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1	1.1	1.15	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	1.45	RZQ	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1	1.4	1.45	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	1.15	RZQ	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1	1.6	1.65	RZQ/2	1,2,5
0,0,1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1	1.1	1.15	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	1.45	RZQ/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1	1.4	1.45	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	1.15	RZQ/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1	1.6	1.65	RZQ/4	1,2,5
0,1,1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1	1.1	1.15	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	1.45	RZQ/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1	1.4	1.45	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	1.15	RZQ/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1	1.6	1.65	RZQ/6	1,2,5
1,0,1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1	1.1	1.15	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	1.45	RZQ/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1	1.4	1.45	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	1.15	RZQ/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1	1.6	1.65	RZQ/8	1,2,5
1,0,0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1	1.1	1.15	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	1.45	RZQ/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1	1.4	1.45	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	1.15	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	1.15	RZQ/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1	1.6	1.65	RZQ/12	1,2,5
Deviation of VM w.r.t VDDQ/2, DVM				-5	-	+5	+5	%	1,2,5,6

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
   Apply VIH(ac) to pin under test and measure current I(VIH(ac)), then apply VIL(ac) to pin under test and measure current I(VIL(ac)) respectively.
   RTT = [VIH(ac) - VIL(ac)] / [I(VIH(ac)) - I(VIL(ac))]
6. Measurement definition for VM and DVM:
   Measure voltage (VM) at test pin (midpoint) with no load:
   Delta $V_M = [2V_M / VDDQ - 1] \times 100$

5.8.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.
Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

5.8.3.1 ODT Sensitivity Definition

	min	max	Unit
RTT	0.9 - dRTTdT*lDelta Tl - dRTTdV*lDelta Vl	1.6 + dRTTdT*lDelta Tl + dRTTdV*lDelta Vl	RZQ/2,4,6,8,12

5.8.3.2 ODT Voltage and Temperature Sensitivity

	Min	Max	Unit
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

Note: These parameters may not be subject to production test. They are verified by design and characterization

5.9 ODT Timing Definitions

5.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in the following figure.

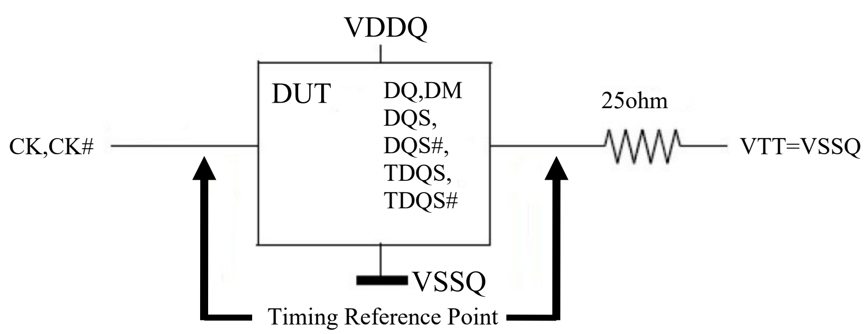


Figure 5.9.1 ODT Timing Reference Load

5.9.2 ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD}, and t_{ADC} are provided in the following table and subsequent figures.

Symbol	Begin Point Definition	End Point Definition
t_{AON}	Rising edge of CK - CK defined by the end point of ODTLon	Extrapolated point at VSSQ
t_{AONPD}	Rising edge of CK - CK with ODT being first registered high	Extrapolated point at VSSQ
t_{AOF}	Rising edge of CK - CK defined by the end point of ODTLoff	End point: Extrapolated point at V_{RTT_Nom}
t_{AOFPD}	Rising edge of CK - CK with ODT being first registered low	End point: Extrapolated point at V_{RTT_Nom}
t_{ADC}	Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	End point: Extrapolated point at V_{RTT_Wr} and V_{RTT_Nom} respectively

Reference Settings for ODT Timing Measurements

Measured Parameter		RTT_Nom Setting	RTT_Wr Setting	VSW1[V]	VSW2[V]
t_{AON}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{AONPD}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{AOFPD}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{ADC}	DDR3	RZQ/12	RZQ/2	0.20	0.30
	DDR3L	RZQ/12	RZQ/2	0.20	0.25

Figure 5.9.2.1 Definition of t_{AON}

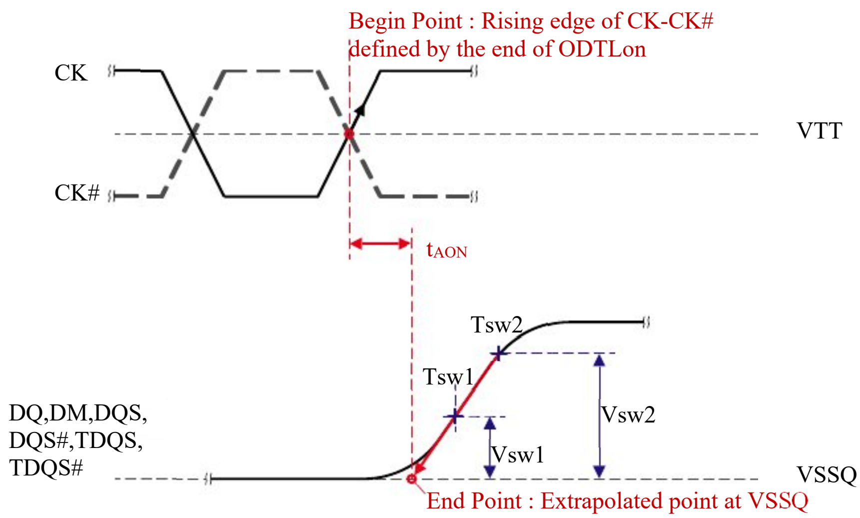


Figure 5.9.2.2 Definition of t_{AONPD}

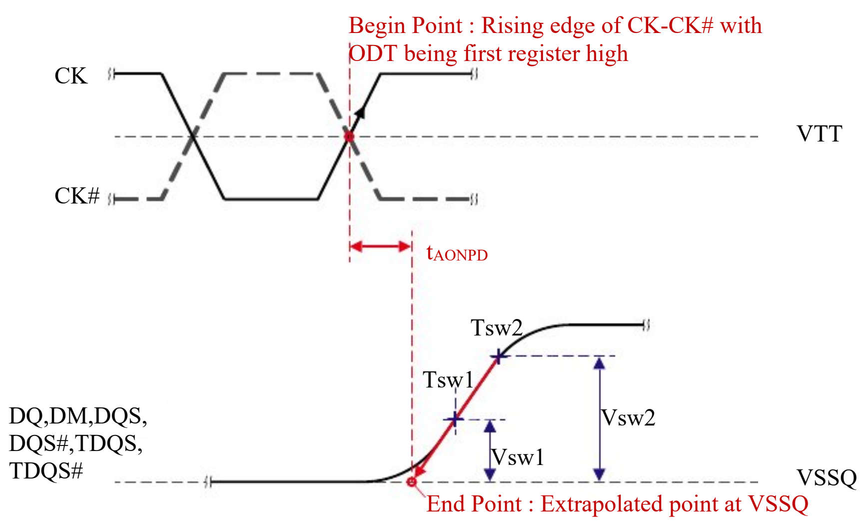


Figure 5.9.2.3 Definition of t_{AOF}

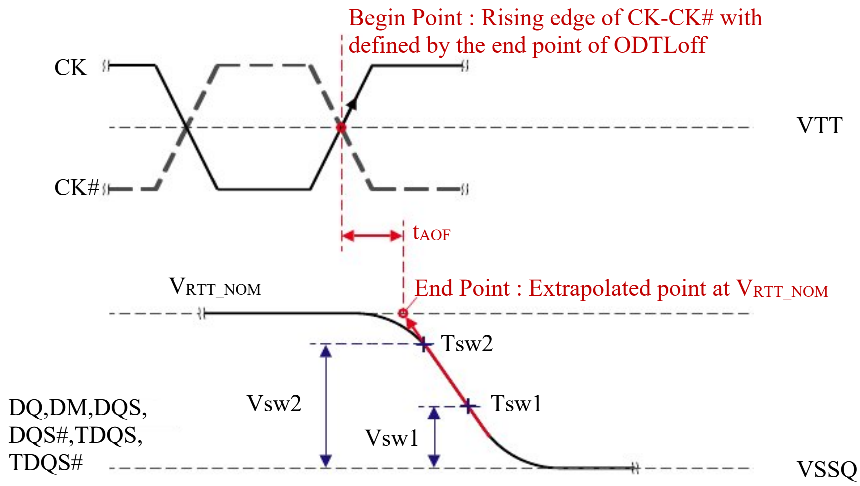


Figure 5.9.2.4 Definition of t_{AOFPD}

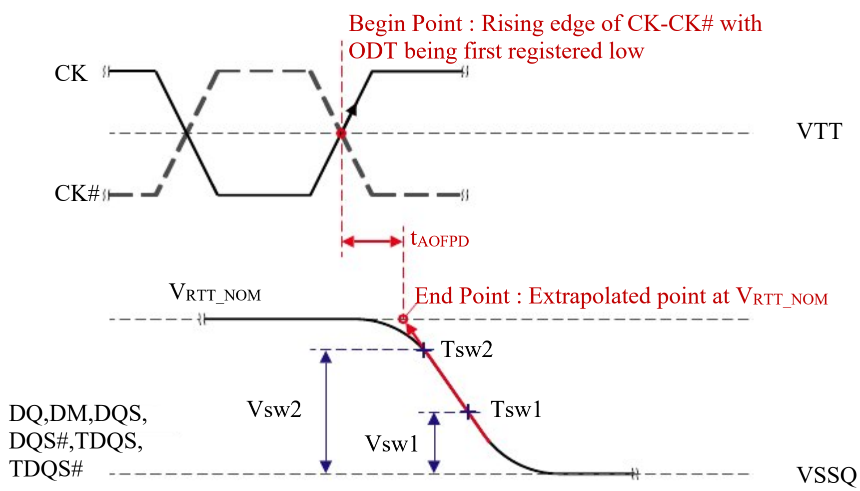
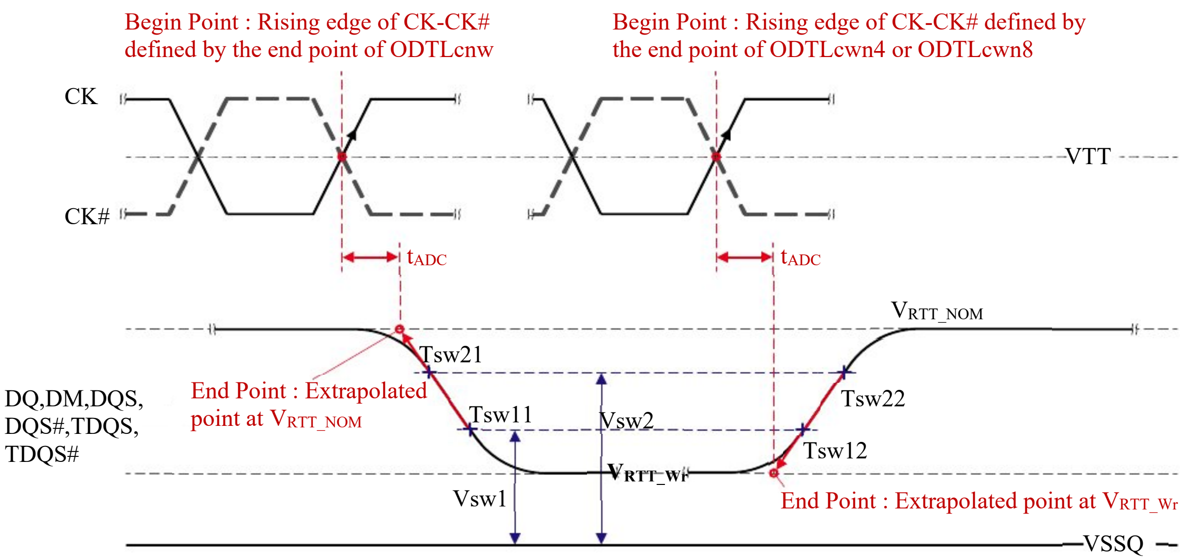


Figure 5.9.2.5 Definition of t_{ADC}



6. INPUT / OUTPUT CAPACITANCE

Symbol	Parameter		DDR3/ DDR3L-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		DDR3/ DDR3L-1866		DDR3-2133		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#,TDQS,TDQS#)	DDR3	1.4	3	1.4	2.7	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
		DDR3L	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	-	-		
C_{CK}	Input capacitance, CK and CK#		0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta, DQS and DQS#		0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance, CTRL, ADD, command input-only pins	DDR3	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,7, 8
		DDR3L	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	-	-		
C_{DI_CTRL}	Input capacitance delta, all CTRL input-only pins		-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7, 8
$C_{DI\_ADD\_CMD}$	Input capacitance delta, all ADD/CMD input-only pins		-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9, 10
C_{DIO}	Input/output capacitance delta, DQ, DM, DQS, DQS# TDQS,TDQS#		-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	-	3	-	3	-	3	-	3	pF	2,3,12

Notes:
1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-$C_{CK\#}$
5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS#)
6. C_I applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#,CAS#,WE#.
7. C_{DI_CTRL} applies to ODT, CS# and CKE
8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CK)+C_I(CK#))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CK)+C_I(CK#))
11. C_{DIO}=C_{IO}(DQ,DM) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.
13. For I/O capacitance of I^2C and ERR, refer to Section 10.7.1 DC Electrical Characteristics.

7. IDD SPECIFICATIONS AND MEASUREMENT CONDITIONS

IDD Specifications (x8), 1.5 Operation Voltage

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
		Max.	Max.	Max.	Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	89	91	100	105	mA
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	99	106	115	121	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	37	37	37	38	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	41	42	43	43	mA
IDD2PQ	Precharge Quiet Standby Current	60	63	67	69	mA
IDD2N	Precharge Standby Current	62	65	70	72	mA
IDD3P	Active Power-Down Current Always Fast Exit	56	58	61	62	mA
IDD3N	Active Standby Current	78	83	92	98	mA
IDD4R	Operating Current Burst Read	128	146	167	211	mA
IDD4W	Operating Current Burst Write	194	219	254	289	mA
IDD5B	Burst Refresh Current	165	168	172	173	mA
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	43	43	43	43	mA
IDD6ET	Self-Refresh Current: extended temperature range	48	48	48	48	mA
IDD7	All Bank Interleave Read Current	208	224	242	269	mA

Note:
1. 1066 and 1333 is for reference only
2. Values applicable for operation with Tc ≤ +95ºC. When Tc > +95ºC, all IDD values must be derated by 30%. When Tc > +105ºC, all IDD values must be derated by 50%. The specification and notes shown in Component Operating Temperature Range, section 3.2 always apply.

IDD Specifications (x16), 1.5 Operation Voltage

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
		Max.	Max.	Max.	Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	89	91	100	105	mA
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	99	106	115	121	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	37	37	37	38	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	41	42	43	43	mA
IDD2PQ	Precharge Quiet Standby Current	60	63	67	69	mA
IDD2N	Precharge Standby Current	62	65	70	72	mA
IDD3P	Active Power-Down Current Always Fast Exit	56	58	61	62	mA
IDD3N	Active Standby Current	78	83	92	98	mA
IDD4R	Operating Current Burst Read	128	146	167	211	mA
IDD4W	Operating Current Burst Write	194	219	254	289	mA
IDD5B	Burst Refresh Current	165	168	172	173	mA
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	43	43	43	43	mA
IDD6ET	Self-Refresh Current: extended temperature range	48	48	48	48	mA
IDD7	All Bank Interleave Read Current	208	224	242	269	mA

Note:
1. 1066 and 1333 is for reference only
2. Values applicable for operation with Tc ≤ +95ºC. When Tc > +95ºC, all IDD values must be derated by 30%. When Tc > +105ºC, all IDD values must be derated by 50%. The specification and notes shown in Component Operating Temperature Range, section 3.2 always apply.

IDD Specifications (x8), 1.35 Operation Voltage

Symbol	Parameter/Condition	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
		Max.	Max.	Max.	Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	83	87	96	101	mA
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	96	102	112	118	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	33	34	34	34	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	37	37	39	40	mA
IDD2PQ	Precharge Quiet Standby Current	54	57	61	64	mA
IDD2N	Precharge Standby Current	56	59	64	67	mA
IDD3P	Active Power-Down Current Always Fast Exit	51	52	56	58	mA
IDD3N	Active Standby Current	73	77	89	95	mA
IDD4R	Operating Current Burst Read	124	141	162	206	mA
IDD4W	Operating Current Burst Write	186	211	246	281	mA
IDD5B	Burst Refresh Current	149	152	156	159	mA
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	39	39	39	39	mA
IDD6ET	Self-Refresh Current: extended temperature range	44	44	44	44	mA
IDD7	All Bank Interleave Read Current	165	222	239	264	mA

Note:
1. 1066 and 1333 is for reference only
2. Values applicable for operation with Tc ≤ +95ºC. When Tc > +95ºC, all IDD values must be derated by 30%. When Tc > +105ºC, all IDD values must be derated by 50%. The specification and notes shown in Component Operating Temperature Range, section 3.2 always apply.

IDD Specifications (x16), 1.35 Operation Voltage

Symbol	Parameter/Condition	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
		Max.	Max.	Max.	Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	83	87	96	101	mA
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	96	102	112	118	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	33	34	34	34	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	37	37	39	40	mA
IDD2PQ	Precharge Quiet Standby Current	54	57	61	64	mA
IDD2N	Precharge Standby Current	56	59	64	67	mA
IDD3P	Active Power-Down Current Always Fast Exit	51	52	56	58	mA
IDD3N	Active Standby Current	73	77	89	95	mA
IDD4R	Operating Current Burst Read	124	141	162	206	mA
IDD4W	Operating Current Burst Write	186	211	246	281	mA
IDD5B	Burst Refresh Current	149	152	156	159	mA
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	39	39	39	39	mA
IDD6ET	Self-Refresh Current: extended temperature range	44	44	44	44	mA
IDD7	All Bank Interleave Read Current	165	222	239	264	mA

Note:
1. 1066 and 1333 is for reference only
2. Values applicable for operation with Tc ≤ +95ºC. When Tc > +95ºC, all IDD values must be derated by 30%. When Tc > +105ºC, all IDD values must be derated by 50%. The specification and notes shown in Component Operating Temperature Range, section 3.2 always apply.

8. Electrical Characteristics and AC timing for DDR3-800 to DDR3-1600

8.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

8.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCKj \right) / N$$

Where N=200

8.1.2 Definition for tCK(abs)

tCK(abs) is defind as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

8.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj \right) / (N \text{ x } tCK(avg)$$

Where N=200

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj \right) / (N \text{ x } tCK(avg)$$

Where N=200

8.1.4 Definition for note for tJIT(per), tJIT(per, lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
tJIT(per) = min/max of {tCKi-tCK(avg) where i=1 to 200}
tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
tJIT(per) and tJIT(per,lck) are not subject to production test.

8.1.5 Definition for tJIT(cc), tJIT(cc, lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |{tCKi+1-tCKi}|

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not subject to production test.

8.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

8.2 Refresh Parameters

Refresh parameters(1,2)

Parameter	Symbol			Units
All Bank Refresh to active/refresh cmd time	tRFC		350	ns
Average periodic refresh interval	tREFI	-40°C ≤ TCASE ≤ 85°C	7.8	µs
		85°C < TCASE ≤ 95°C	3.9	µs
		95°C < TCASE ≤ 105°C	1.95	µs
		105°C < TCASE ≤ 115°C	0.97	µs
		115°C < TCASE ≤ 125°C	0.488	µs

Notes:

1. The permissible Tcase (Tc) operating temperature is specified by temperature grade. The maximum Tc is 95°C unless:
   a. A2 grade, for which the maximum is 105°C.
   b. A25 grade, for which the maximum is 115°C.
   c. A3 grade, for which the maximum is 125°C
   Refer to 3.2 Component Operating Temperature Range.
2. In general, the Refresh command needs to be issued at the tREFI interval. For flexibility, a maximum of 8 Refresh commands may be postponed or pulled-in (done in advance). However, in either case, the maximum interval between any two consecutive Refresh commands is 9 x tREFI

8.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

DDR3-1600MT/s

Speed Bin			DDR3/DDR3L-1600		Unit
CL-nRCD-nRP			12-11-11 (-125L)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	15.00	20	ns
ACT to internal read or write delay		tRCD	13.75	-	ns
PRE command period		tRP	13.75	-	ns
ACT to ACT or REF period		tRC	48.75	-	ns
ACT to PRE command period		tRAS	35	9*tREFI	ns
CL=5	CWL =5	tCK(AVG)	3.0	3.3	ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=6	CWL =5	tCK(AVG)	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns

CL=7	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=8	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=9	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=10	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	1.5	<1.875	ns
	CWL =8	tCK(AVG)	Reserved		ns
CL=11	CWL =5	tCK(AVG)	Reserved		ns
	CWL= 6	tCK(AVG)	Reserved		ns
	CWL= 7	tCK(AVG)	Reserved		ns
	CWL =8	tCK(AVG)	Reserved		ns
CL=12	CWL =5	tCK(AVG)	Reserved		ns
	CWL= 6	tCK(AVG)	Reserved		ns
	CWL= 7	tCK(AVG)	Reserved		ns
	CWL =8	tCK(AVG)	1.250	<1.5	ns
Supported CL Settings			5,6,7,8,9,10,11,12		nCK
Supported CWL Settings			5,6,7,8		nCK

Note : *: Optional

DDR3-1600MT/s

Speed Bin			DDR3/DDR3L-1600		Unit
CL-nRCD-nRP			11-11-11 (-125K)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	13.75	20	ns
ACT to internal read or write delay		tRCD	13.75	-	ns
PRE command period		tRP	13.75	-	ns
ACT to ACT or REF period		tRC	48.75	-	ns
ACT to PRE command period		tRAS	35	9*tREFI	ns
CL=5	CWL =5	tCK(AVG)	3.0	3.3	ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=6	CWL =5	tCK(AVG)	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=7	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=8	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=9	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	1.5	<1.875	ns
	CWL=8	tCK(AVG)	Reserved		ns
CL=10	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	1.5	<1.875	ns
	CWL =8	tCK(AVG)	Reserved		ns
CL=11	CWL =5	tCK(AVG)	Reserved		ns
	CWL= 6	tCK(AVG)	Reserved		ns
	CWL= 7	tCK(AVG)	Reserved		ns
	CWL =8	tCK(AVG)	1.250	<1.5	ns
Supported CL Settings			5,6,7,8,9,10,11		nCK
Supported CWL Settings			5,6,7,8		nCK

Note : *: Optional

DDR3-1866MT/s

Speed Bin			DDR3/DDR3L-1866		Unit
CL-nRCD-nRP			14-13-13 (-107N)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	14.98	20	ns
ACT to internal read or write delay		tRCD	13.91	-	ns
PRE command period		tRP	13.91	-	ns
ACT to ACT or REF period		tRC	47.91	-	ns
ACT to PRE command period		tRAS	34	9*tREFI	ns
CL=5	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8,9	tCK(AVG)	Reserved		ns
CL=6	CWL =5	tCK(AVG)	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8,9	tCK(AVG)	Reserved		ns
CL=7	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8,9	tCK(AVG)	Reserved		ns
CL=8	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8,9	tCK(AVG)	Reserved		ns
CL=9	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8,9	tCK(AVG)	Reserved		ns
CL=10	CWL =5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	1.5	<1.875	ns
	CWL =8,9	tCK(AVG)	Reserved		ns
CL=11	CWL=5,6,7,8,9	tCK(AVG)	Reserved		ns
CL=12	CWL =5,6	tCK(AVG)	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		ns
	CWL=8	tCK(AVG)	1.25	<1.5	ns
	CWL =9	tCK(AVG)	Reserved		ns
CL=13	CWL=5,6,7,8	tCK(AVG)	Reserved		ns
	CWL =9	tCK(AVG)	Reserved		ns
CL=14	CWL=5,6,7,8	tCK(AVG)	Reserved		ns
	CWL =9	tCK(AVG)	1.07	<1.25	ns
Supported CL Settings			5,6,7,8,9,10,11,12,13,14		nCK
Supported CWL Settings			5,6,7,8,9		nCK

Note :In these tables in section 8.3, grey shading is for readability purposes only.

9. ELECTRICAL CHARACTERISTICS & AC TIMING

9.1 Timing Parameter by Speed Bin (DDR3-800, DDR3-1066)

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	5	7800	5	7800	ns	6,35
Average Clock Period	tCK(avg)	Refer to Standard Speed Bins				ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min				ps	
		Max.: tCK(avg)max + tJIT(per)max					
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	tJIT(per)	-100	100	-90	90	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200	200	180	180	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180	180	160	160	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	ps	
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	ps	
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	ps	
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	ps	
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	ps	
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	ps	
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	ps	
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	ps	
Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	ps	
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	ps	

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max				ps	24
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13,g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-800	400	-600	300	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	ps	13,14,f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175 or AC160	See table for Data Setup and Hold				ps	d,17
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150 or AC135					ps	d,17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100 or DC90					ps	d,17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	ps	28
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	13,19,g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	tCK(avg)	13,g
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	tCK(avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	1
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-400	400	-300	300	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-800	400	-600	300	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	ps	13,14,f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	tCK(avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	tCK(avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -					e,33
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:					e,18
WRITE recovery time	tWR	15	-	15	-	ns	e,18, 33,34
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:					
ACT to internal read or write delay time	tRCD	Standard Speed Bins					e
PRE command period	tRP	Standard Speed Bins					e
ACT to ACT or REF command period	tRC	Standard Speed Bins					e
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					e,33
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 10ns)	-	max(4nCK, 10ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175 or AC160	See table for ADD/CMD setup and hold				ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150 or AC135					ps	b,16,27
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100 or DC90					ps	b,16
Control and Address Input pulse width for each input	tIPW	900	-	780	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max (512 nCK, 640ns)	-	max (512 nCK, 640ns)	-		
Normal operation Full calibration time	tZQoper	max (256 nCK, 320ns)	-	max (256 nCK, 320ns)	-		
Normal operation Short calibration time	tZQCS	max (64 nCK, 80ns)	-	max (64 nCK, 80ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -					
Self Refresh Timings							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -				nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -					
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -					
Power Down Timings							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 7.5ns) tXPmax.: -				nCK	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -					2
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 7.5ns) tCKEmax.: -		tCKEmin.: max(3nCK 5.625ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmax.: -					
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI					15

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	10
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timings							
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	ps	
Write leveling output delay	tWLO	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

9.2 Timing Parameter by Speed Bin (DDR3-1333, DDR3-1600)

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	5	7800	5	7800	ns	6,35
Average Clock Period	tCK(avg)	Refer to Standard Speed Bins				ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	tJIT(per)	-80	80	-70	70	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	160	160	140	140	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140	140	120	120	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-118	118	-103	103	ps	
Cumulative error across 3 cycles	tERR(3per)	-140	140	-122	122	ps	
Cumulative error across 4 cycles	tERR(4per)	-155	155	-136	136	ps	
Cumulative error across 5 cycles	tERR(5per)	-168	168	-147	147	ps	
Cumulative error across 6 cycles	tERR(6per)	-177	177	-155	155	ps	
Cumulative error across 7 cycles	tERR(7per)	-186	186	-163	163	ps	
Cumulative error across 8 cycles	tERR(8per)	-193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	-200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	-205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	-210	210	-184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	-215	215	-188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max				ps	24
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13,g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-500	250	-450	225	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	250	-	225	ps	13,14,f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	See table for Data Setup and Hold				ps	d,17
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC135					ps	d,17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100 or DC90					ps	d,17
DQ and DM Input pulse width for each input	tDIPW	400	-	360	-	ps	28
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	13,19,g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential output low time	tQSL	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	1
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	-225	225	ps	13,f

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-500	250	-450	225	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	250	-	225	ps	13,14,f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.27	0.27	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.18	-	tCK(avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.18	-	tCK(avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -					e,33
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:					e,18
WRITE recovery time	tWR	15	-	15	-	ns	e,18,33,34
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:					
ACT to internal read or write delay time	tRCD	Standard Speed Bins					e
PRE command period	tRP	Standard Speed Bins					e
ACT to ACT or REF command period	tRC	Standard Speed Bins					e
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					e,33
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Four activate window for 1KB page size	tFAW	30	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	45	-	40	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175 or AC160	See table for ADD/CMD Setup and Hold				ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150 or AC135					ps	b,16,27
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100 or DC90					ps	b,16
Control and Address Input pulse width for each input	tIPW	620	-	560	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max (512 nCK, 640ns)	-	max (512 nCK, 640ns)	-		
Normal operation Full calibration time	tZQoper	max (256 nCK, 320ns)	-	max (256 nCK, 320ns)	-		
Normal operation Short calibration time	tZQCS	max (64 nCK, 80ns)	-	max (64 nCK, 80ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -					
Self Refresh Timings							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -					

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -				nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -					
Power Down Timings							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -					
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -					2
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 5.625ns) tCKEmax.: -		tCKEmin.: max(3nCK 5ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmax.: -				nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI					15
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	10
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timings							
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-250	250	-225	225	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	195	-	165	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	195	-	165	-	ps	
Write leveling output delay	tWLO	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

9.3 Timing Parameter by Speed Bin (DDR3-1866, DDR3-2133)

Parameter	Symbol	DDR3/DDR3L-1866		DDR3-2133		Units	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	5	7800	5	7800	ns	6,35
Average Clock Period	tCK(avg)	Refer to Standard Speed Bins				ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	tJIT(per)	-60	60	-50	50	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-40	40	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	120	120	100	100	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100	100	80	80	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-88	88	-74	74	ps	
Cumulative error across 3 cycles	tERR(3per)	-105	105	-87	87	ps	
Cumulative error across 4 cycles	tERR(4per)	-117	117	-97	97	ps	
Cumulative error across 5 cycles	tERR(5per)	-126	126	-105	105	ps	
Cumulative error across 6 cycles	tERR(6per)	-133	133	-111	111	ps	
Cumulative error across 7 cycles	tERR(7per)	-139	139	-116	116	ps	
Cumulative error across 8 cycles	tERR(8per)	-145	145	-121	121	ps	
Cumulative error across 9 cycles	tERR(9per)	-150	150	-125	125	ps	
Cumulative error across 10 cycles	tERR(10per)	-154	154	-128	128	ps	
Cumulative error across 11 cycles	tERR(11per)	-158	158	-132	132	ps	
Cumulative error across 12 cycles	tERR(12per)	-161	161	-134	134	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max				ps	24
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	85	-	75	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13,g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-390	195	-360	180	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	195	-	180	ps	13,14,f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC135	See table for Data Setup and Hold				ps	d,17
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC130					ps	d,17

Parameter	Symbol	DDR3/DDR3L-1866		DDR3/DDR3L-2133		Units	Notes
		Min.	Max.	Min.	Max.		
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100 or DC90	See table for Data Setup and Hold				ps	d,17
DQ and DM Input pulse width for each input	tDIPW	320	-	280	-	ps	28
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	13,19,g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential output low time	tQSL	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	1
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-195	195	-180	180	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-390	195	-360	180	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	195	-	180	ps	13,14,f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	tCK(avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	tCK(avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -					e,33
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:					e,18
WRITE recovery time	tWR	15	-	15	-	ns	e,18,33,34
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:					
ACT to internal read or write delay time	tRCD	Standard Speed Bins					e
PRE command period	tRP	Standard Speed Bins					e
ACT to ACT or REF command period	tRC	Standard Speed Bins					e
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					e,33
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 5.0ns)	-	max(4nCK, 5.0ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 6.0ns)	-	max(4nCK, 6.0ns)	-		
Four activate window for 1KB page size	tFAW	27	-	25	-	ns	e
Four activate window for 2KB page size	tFAW	35	-	35	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC135	See table for ADD/CMD setup and hold				ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC125					ps	b,16
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100 or DC90					ps	b,16

Parameter	Symbol	DDR3/DDR3L-1866		DDR3/DDR3L-2133		Units	Notes
		Min.	Max.	Min.	Max.		
Control and Address Input pulse width for each input	tIPW	535	-	470	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max (512 nCK, 640ns)	-	max (512 nCK, 640ns)	-		
Normal operation Full calibration time	tZQoper	max (256 nCK, 320ns)	-	max (256 nCK, 320ns)	-		
Normal operation Short calibration time	tZQCS	max (64 nCK, 80ns)	-	max (64 nCK, 80ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -					
Self Refresh Timings							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -				nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -				nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -				nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -				nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -				nCK	
Power Down Timings							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -					
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -					2
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 5 ns) tCKEmax.: -					
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmax.: -				nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI					15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	2	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	2	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	2	-	nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timings							
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	

Parameter	Symbol	DDR3/DDR3L-1866		DDR3/DDR3L-2133		Units	Notes
		Min.	Max.	Min.	Max.		
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-195	195	-180	180	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	140	-	125	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	140	-	125	-	ps	
Write leveling output delay	tWLO	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

9.4. Timing Notes

9.4.1 Jitter

Specific Note a
Unit “tCK(avg)” represents the actual tCK(avg) of the input clock under operation. Unit “nCK” represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD=4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) + tERR(4per), min.

Specific Note b
These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c
These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)) crossing to its respective clock signal (CK, CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d
These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)) crossing.

Specific Note e
For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP =RU{tRP/tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP/tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6-Tm) is less than 15ns due to input clock jitter.

Specific Note f

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <=12. (output derating are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = -172ps and tERR(mper),act,max = 193ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = -400ps - 193ps = -593ps and tDQSCK,max(derated) = tDQSCK,max - ERR(mper),act,min = 400ps + 172ps = 572ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = -800ps - 193ps = -993ps and tLZ(DQ),max(derated) = 400ps + 172ps = 572ps. (Caution on the min/max usage!)

Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note g

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act=2500ps, tJIT(per),act,min = -72ps and tJIT(per),act,max = 93ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500ps - 72ps = 2178ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500ps - 72ps = 878ps. (Caution on the min/max usage!)

9.4.2 Timing Parameters

1. Actual value dependent upon measurement level definitions.
2. Commands requiring a locked DLL are: READ (and RAP) are synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rouned-up to next higher integer value.
6. The refresh interval, tREFI must be satisfied. Normal Mode Timings or functionality is not guaranteed when DLL off.
7. For definition of RTT-on time tAON See “Timing Parameters”.
8. For definition of RTT-off time tAOF See “Timing Parameters”.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles are programmed in MR0.
11. The maximum read postamble is bonded by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. tREFI depends on TOPER.
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
18. Start of internal write transaction is defined as follows:
    a. For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
    b. For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
    c. For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by tLZ(DQS)max on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.

22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. the interval could be defined by the following formula:

    ZQCorrection / [(TSens x Tdriftrate) + (VSens x Vdriftrate)]

    , where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

    For example, if TSens = 1.5%/C, VSens = 0.15%/mV, Tdriftrate = 1 C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as

    0.5 / [(1.5x1)+(0.15x15)] = 0.133 ≈ 128ms

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower altemate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150mV) / 1V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
33. The tRAS(min) is required in order to complete the internal Precharge during a Read or Write with Auto Precharge.
34. During DLL off (Disable), tWR(min) is the greater of 4nCK or 15ns.
35. For DLL off (Disable)
    a. Any Auto Refresh Command must have at least one NOP Command before the next Auto Refresh.
    b. If tCK < 40ns, any Auto Refresh Command must be followed by a Precharge All Command.
    c. For 85ºC < tCASE ≤ 95ºC, tCK(max) = 3.9µs. DLL off is not specified for tCASE > 95ºC

9.5 Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the datasheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value, respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value . If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF (dc) level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF (dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed in the tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

9.5.1 ADD/CMD Setup and Hold Base-Values for 1V/ns

DDR3/ DDR3L	Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
DDR3	tIS(base) AC175	VIH/L(ac)	200	125	65	45	-	-	ps
	tIS(base) AC150	VIH/L(ac)	350	275	190	170	-	-	ps
	tIS(base) AC135	VIH/L(ac)	-	-	-	-	65	60	ps
	tIS(base) AC125	VIH/L(ac)	-	-	-	-	150	135	ps
	tIH(base) DC100	VIH/L(dc)	275	200	140	120	100	95	ps
DDR3L	tIS(base) AC160	VIH/L(ac)	215	140	80	60	-	-	ps
	tIS(base) AC135	VIH/L(ac)	365	290	205	185	65	-	ps
	tIS(base) AC125	VIH/L(ac)	-	-	-	-	150	-	ps
	tIH(base) DC90	VIH/L(dc)	285	210	150	130	110	-	ps

Note:
1. (AC/DC referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)

9.5.2 Derating values [ps] for DDR3L-800/1066/1333/1600 tIS/tIH - AC/DC based AC160 Threshold

AC160 Threshold -> VIH(ac) = VREF(dc) + 160mV, VIL(ac) = VREF(dc) - 160mV																	
DDR3L		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

9.5.3 Derating values [ps] for DDR3L-800/1066/1333/1600 tIS/tIH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV																	
DDR3L		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

9.5.4 Derating values [ps] for DDR3L-1866 tIS/tIH - AC/DC based AC125 Threshold

AC125 Threshold -> VIH(ac) = VREF(dc) + 125mV, VIL(ac) = VREF(dc) - 125mV																	
DDR3L		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	-4	40	4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

9.5.5 Derating values [ps] for DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based AC175 Threshold

AC175 Threshold -> VIH(ac) = VREF(dc) + 175mV, VIL(ac) = VREF(dc) - 175mV																	
DDR3		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

9.5.6 Derating values [ps] for DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based AC150 Threshold

AC150 Threshold -> VIH(ac) = VREF(dc) + 150mV, VIL(ac) = VREF(dc) - 150mV																	
DDR3		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

9.5.7 Derating values [ps] for DDR3-1866/2133 tIS/tIH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV																	
DDR3		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

9.5.8 Derating values [ps] for DDR3-1866/2133 tIS/tIH - AC/DC based AC125 Threshold

AC125 Threshold -> VIH(ac) = VREF(dc) + 125mV, VIL(ac) = VREF(dc) - 125mV																	
DDR3		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

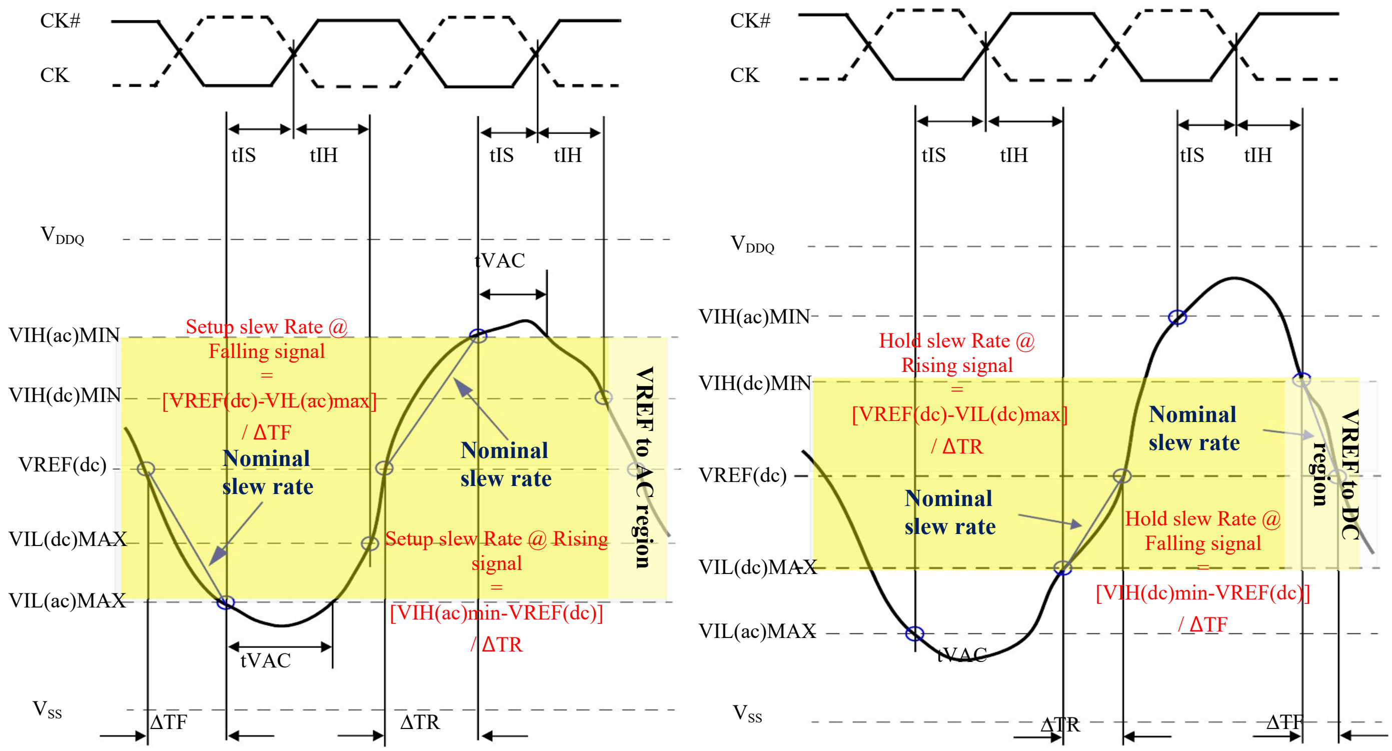
9.5.9 Required minimum time tVAC above VIH(ac) {below VIL(ac)} for valid ADD/CMD transition

Slew Rate [V/ns]	DDR3				DDR3L			
	800/1066/1333/1600		1866/2133		800/1066/1333/1600		1866	
	175mV [ps]	150mV [ps]	135mV [ps]	125mV [ps]	160mV [ps]	135mV [ps]	135mV [ps]	125mV [ps]
> 2.0	75	175	168	173	200	213	200	205
2	57	170	168	173	200	213	200	205
1.5	50	167	145	152	173	190	178	184
1	38	130	100	110	120	145	133	143
0.9	34	113	85	96	102	130	118	129
0.8	29	93	66	79	80	111	99	111
0.7	22	66	42	56	51	87	75	89
0.6	Note	30	10	27	13	55	43	59
0.5	Note	Note	Note	Note	Note	10	Note	18
< 0.5	Note	Note	Note	Note	Note	10	Note	18

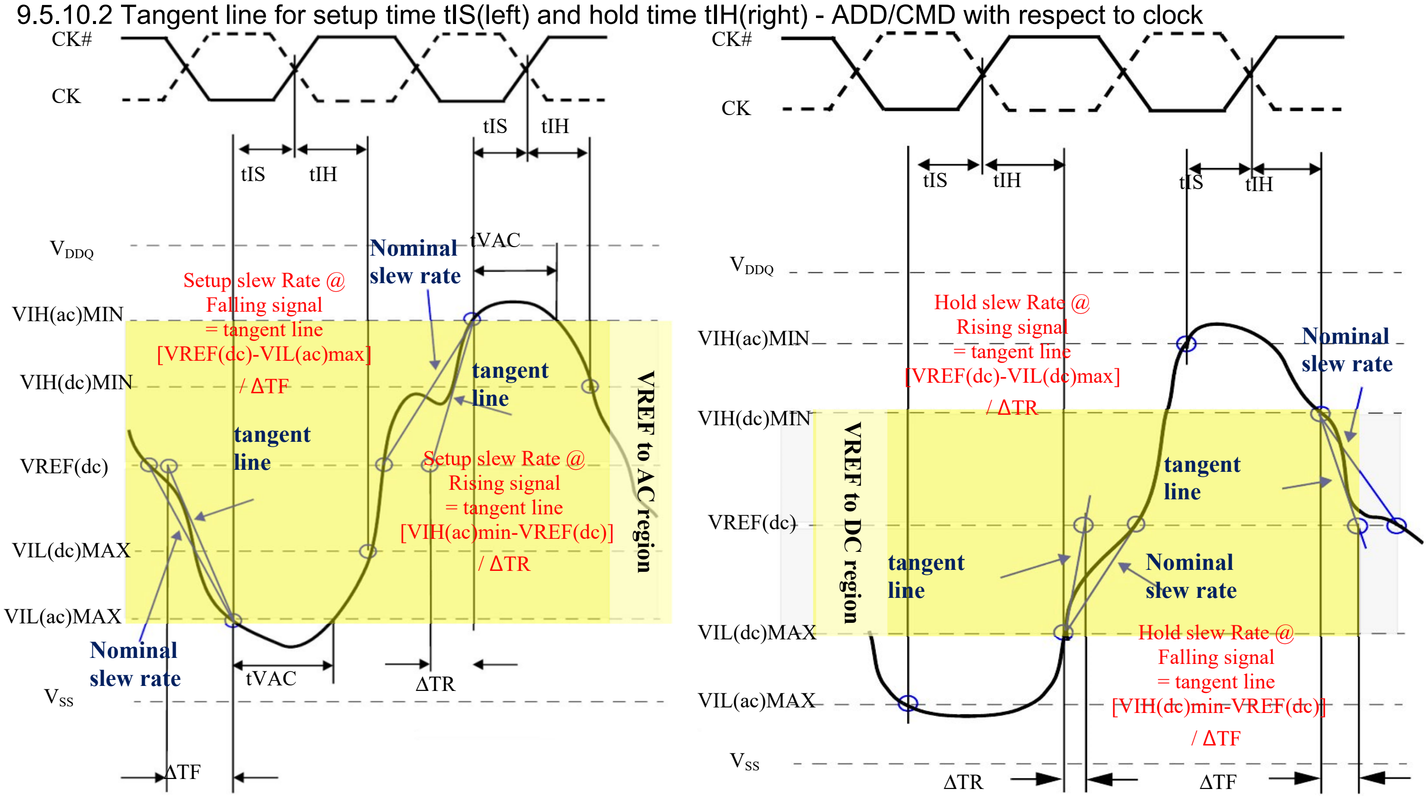
Note:
The rising input signal shall become equal to or greater than VIH(ac) level; and the falling input signal shall become equal to or less than VIL(ac) level.

9.5.10 Address / Command Setup, Hold and Derating

9.5.10.1 Nominal slew rate and tVAC for setup time tIS(left) and hold time tIH(right) – ADD/CMD with respect to clock



9.5.10.2 Tangent line for setup time tIS(left) and hold time tIH(right) - ADD/CMD with respect to clock



9.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see corresponding tables) to the ∆tDS and ∆tDH (see corresponding tables) derating value respectively. Example: tDS (total setup time) = tDS(base) + ∆tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of V IH(ac) min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF(dc) level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc) max and the first crossing of VREF(dc) . Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc) min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V REF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac) .

For slew rates in between the values listed in the tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

9.6.1 Data Setup and Hold Base-Values

	Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
DDR3	tDS(base) AC175	VIH/L(ac), SR= 1V/ns	75	25	-	-	-	-	ps
	tDS(base) AC150	VIH/L(ac), SR= 1V/ns	125	75	30	10	-	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 1V/ns	165	115	60	40	-	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 2V/ns	-	-	-	-	68	53	ps
	tDH(base) DC100	VIH/L(dc), SR= 1V/ns	150	100	65	45	-	-	ps
	tDH(base) DC100	VIH/L(dc), SR= 2V/ns	-	-	-	-	70	55	ps
DDR3L	tDS(base) AC160	VIH/L(ac), SR= 1V/ns	90	40	-	-	-	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 1V/ns	140	90	45	25	-	-	ps
	tDS(base) AC130	VIH/L(ac), SR= 2V/ns	-	-	-	-	70	-	ps
	tDH(base) DC90	VIH/L(dc), SR= 1V/ns	160	110	75	55	-	-	ps
	tDH(base) DC90	VIH/L(dc), SR= 2V/ns	-	-	-	-	75	-	ps

NOTE: (Note: AC/DC referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate, or 1V/ns DQ-slew rate and 2V/ns DQS slew rate, as shown.

9.6.2 Derating values [ps] for DDR3L-800/1066 tDS/tDH - AC/DC based AC160

AC160 Threshold -> VIH(ac) = VREF(dc) + 160mV, VIL(ac) = VREF(dc) - 160mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

9.6.3 Derating values [ps] for DDR3L-800/1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

9.6.4 Derating values [ps] for DDR3L-1866 tDS/tDH - AC/DC based AC130 Threshold

AC130 Threshold -> VIH(ac) = VREF(dc) + 130mV, VIL(ac) = VREF(dc) - 130mV																									
DDR3L		DQS, DQS# Differential Slew Rate																							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	4	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
	1	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

9.6.5 Derating values [ps] for DDR3-800/1066 tDS/tDH - AC/DC based AC175 Threshold

AC175 Threshold -> VIH(ac) = VREF(dc) + 175mV, VIL(ac) = VREF(dc) - 175mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

9.6.6 Derating values [ps] for DDR3-800/1066/1333/1600 tDS/tDH - AC/DC based AC150 Threshold

AC150 Threshold -> VIH(ac) = VREF(dc) + 150mV, VIL(ac) = VREF(dc) - 150mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

9.6.7 Derating values [ps] for DDR3-1866/2133 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV DC100 Threshold -> VIH(dc) = VREF(dc) + 100mV, VIL(dc) = VREF(dc) - 100mV																									
DDR3		DQS, DQS# Differential Slew Rate																							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	4	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-36	-76	-30	-60

9.6.8 Derating values [ps] for DDR3-800/1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV
DC100 Threshold -> VIH(dc) = VREF(dc) + 100mV, VIL(dc) = VREF(dc) - 100mV

DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

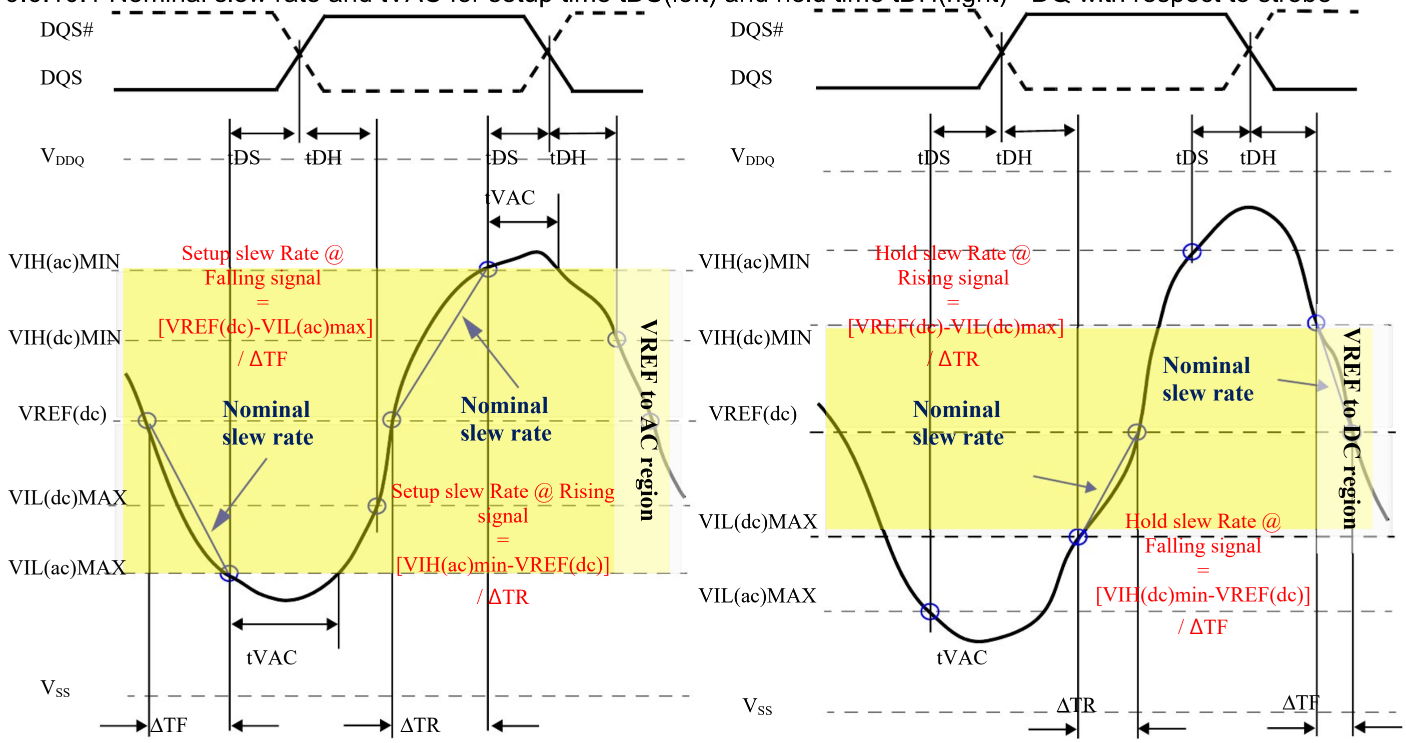
9.6.9 Required minimum time tVAC [ps] above VIH(ac) {below VIL(ac)} for valid DQ transition

Slew Rate [V/ns]	DDR3					DDR3L		
	800/1066	800/1066/1333/1600	800/1066/1333/1600	1866	2133	800/1066	800/1066/1333/1600	1866
	AC175	AC150	AC135			AC160	AC135	AC130
> 2.0	75	105	113	93	73	165	113	95
2	57	105	113	93	73	165	113	95
1.5	50	80	90	70	50	138	90	73
1	38	30	45	25	5	85	45	30
0.9	34	13	30	Note	Note	67	30	16
0.8	29	Note	11	Note	Note	45	11	Note
0.7	Note	Note	Note	-	-	16	Note	-
0.6	Note	Note	Note	-	-	Note	Note	-
0.5	Note	Note	Note	-	2	Note	Note	-
< 0.5	Note	Note	Note	-	-	Note	Note	-

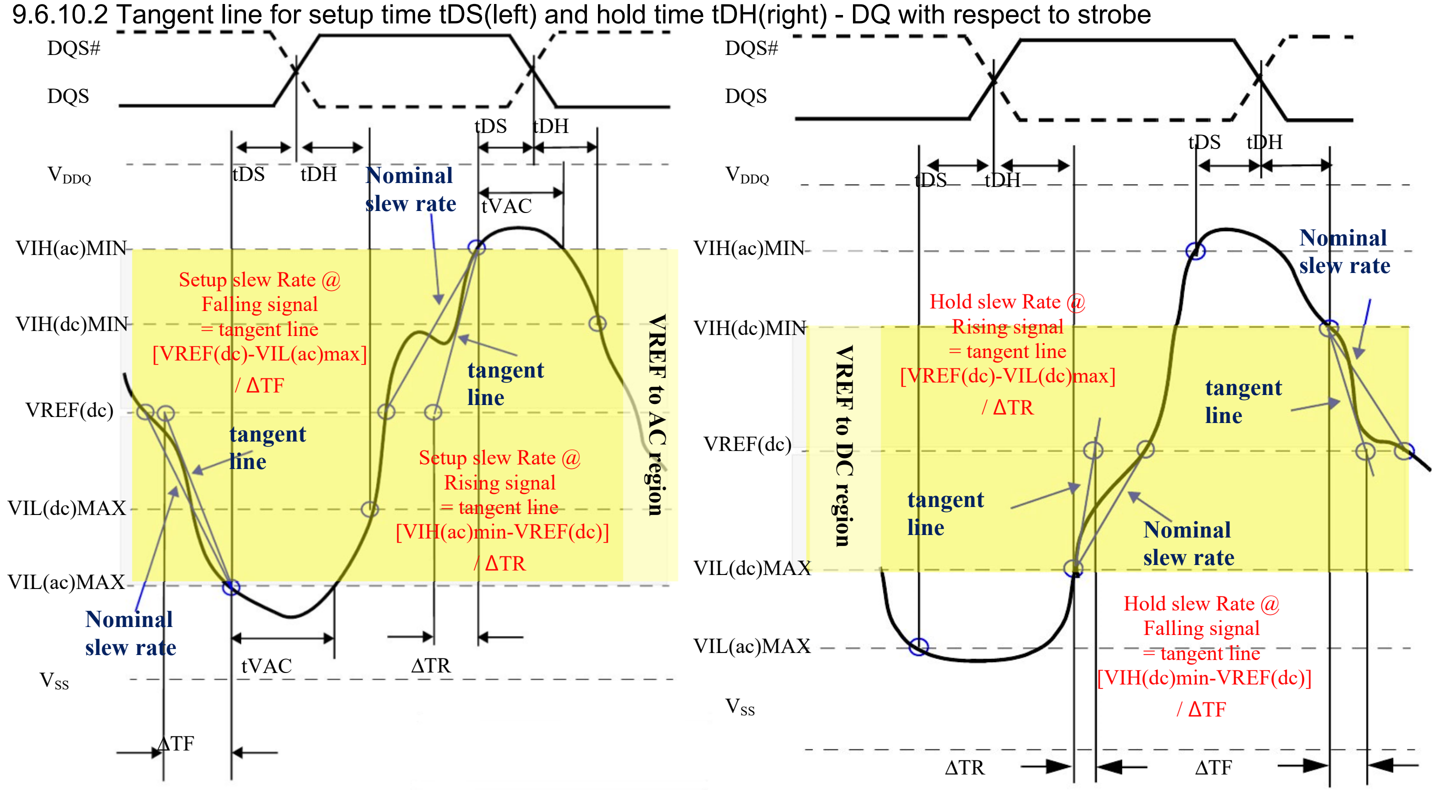
Note:
The rising input signal shall become equal to or greater than VIH(ac) level; and the falling input signal shall become equal to or less than VIL(ac) level.

9.6.10 Data Setup, Hold and Slew Rate Derating

9.6.10.1 Nominal slew rate and tVAC for setup time tDS(left) and hold time tDH(right) - DQ with respect to strobe



9.6.10.2 Tangent line for setup time tDS(left) and hold time tDH(right) - DQ with respect to strobe



10. DDR3 DRAM with On-Chip ECC (Error Correction Code)

ISSI's 4Gb DDR3 DRAM implements an On-Chip ECC function (SEC-DED Code: Single Error Correction, Double Error Detection) that detects and corrects single bit errors, and detects double bit errors, including those introduced by SER events such as cosmic rays, alpha particles, etc. ECC is implemented across 4-bit data quantum using 4 ECC parity bits for a total of 8 bits per ECC quantum, to maximize reliability (ECC chunk size = 4 bit). In x16 organization, it could correct up to maximum 4 bits out of 16 bits.

Key features of ECC function.

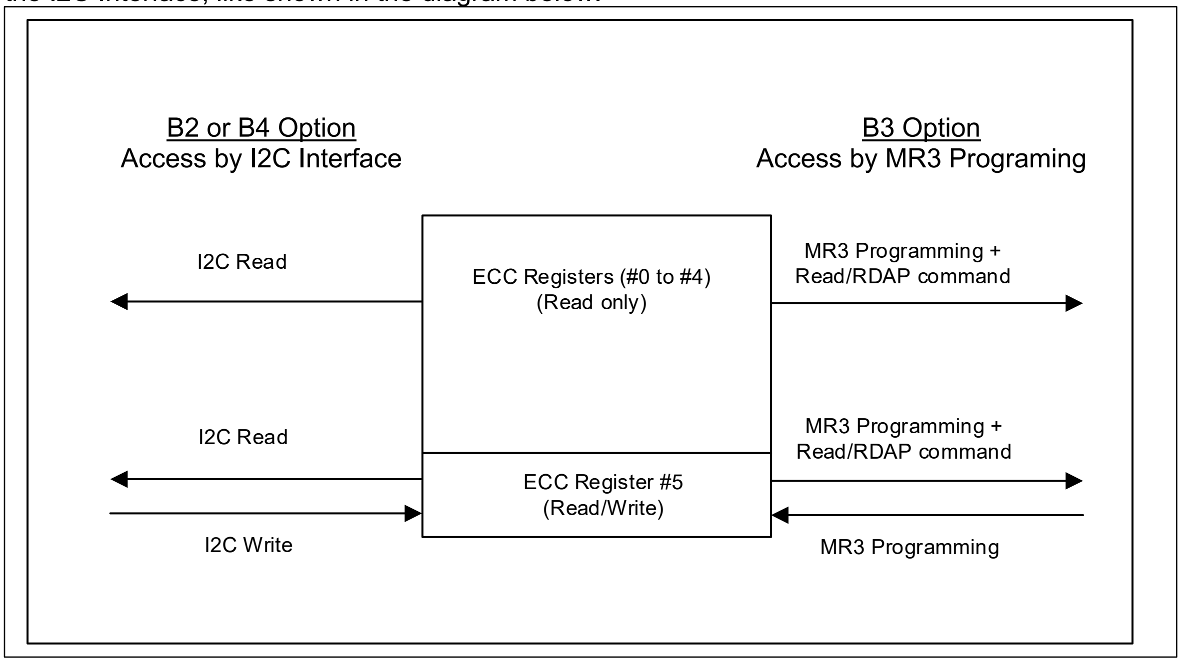
- Independent ECC parity bits per 4–bits (each Half-Byte)
  - Detect and correct one bit error per individual half-byte or detect 2-bit error per individual half-byte. Max. 4 single- bit can be detected and corrected in x16 device at a time.
- Programmable ECC ON/OFF function:
  - ECC can be disabled by setting A5 bit in MR3 to "0". Default value is "1".
  - Even though ECC is OFF, the previous data value in ECC parity bits can be valid.
- Store first ECC Event location:
  - ER1 to ER4 will store first ECC Event location (address) regardless of ECC Event type (1-bit fix or 2-bit error detection). Stored address will be cleared when ECC Clear bit (OP4 bit of ER5 register) is set to "1".
- Optional ERR Signal ON/OFF function: Optional ERR signal indicates ECC event. It can be enabled by setting ERRON bit (OP1 of ER5 register) to "1". Default value is "0".
- Optional ERR Signal location is H9 in 78 BGA(x8), and L9 in 96 BGA(x16).

ECC registers are located in the MPR (Multi-Purpose Registers), which is controlled by either MR3 programming or the optional I2C Interface. The **B2** ordering option only supports ECC register access via I^2C protocol, and the **B3** ordering option only supports ECC register access via MR3 programming. The ECC feature setting and ECC Event status can be handled by ECC Registers (ER0 to ER5)

- ECC Event Counter will store Cumulative ECC Event occurrence in ER0.
- ECC Event location information will be stored in ER1 to ER4.
- ECC feature can be set by ER5 programming, which can be also read out.

10.1 ECC Registers

ECC registers are part of MPR (Multipurpose Register), and include ECC configuration and ECC Event information. Depending on the ordering option, ECC registers can be accessed by MR3 programming via the Load Mode command, or the I2C Interface, like shown in the diagram below.



Note: The B2 and B4 options support the I2C, but not MR3 access to the ECC register. The B3 option supports the MR3, but not I2C access to the ECC regsiters.

There are 6 ECC registers: ER0 to ER5.
ER0 ~ER4 are Read only registers, and ER5 is a Read/Write Register.

ECC Register 0

ER#	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	**R**	2-Bit ERROR Counter			1-Bit ERROR Counter			ECC Type	ECC Event

- ECC Event bit [OP0]) : 0 = No ECC Event , 1 = Yes ECC Event

- ECC Type bit [OP1] : 0 = 2-bit ERROR , 1 = 1-bit ERROR
  - Even though ERRON bit is disabled (bit [OP1] = 0 in ER5), ECC Event occurrence & ECC Type can be verified by ER0
  - ECC Type bit should be ignored when ECC Event bit [OP0] = “0”.

- ERROR Counter [OP7:OP2] - Store Cumulative ECC Event Occurrence until clear it in ER5.
  - 3 bits (Max 7 ECC Event) for 1-bit ERROR. More than 7 ECC Event cannot be counted.
  - 3 bits (Max 7 ECC Event) for 2-bit ERROR. More than 7 ECC Event cannot be counted.
  - Each Error Counter can increment by a maximum of one per Read burst.

- ECC Event status can be monitored by accessing (Reading out) OP1 bit and OP0 bit of ER0 register to check ECC Event record.

The registers ER1 to ER4 store the first ECC Event location (address), which is either 1-bit correction or 2-bit error detection. Only a single ECC Event location (address) can be stored.

ECC Register 1

ER#	Access	OP7 (CA4)	OP6 (CA3)	OP5 (CA2)	OP4 (CA1)	OP3 (CA0)	OP2 (BA2)	OP1 (BA1)	OP0 (BA0)
1	R	Column Address		Reserved			Bank Address ([BA0] : OP0)		

ECC Register 2

ER#	Access	OP7	OP6	OP5	OP4 (CA9)	OP3 (CA8)	OP2 (CA7)	OP1 (CA6)	OP0 (CA5)
2	R	Reserved			Column Address				

ECC Register 3

ER#	Access	OP7 (RA7)	OP6 (RA6)	OP5 (RA5)	OP4 (RA4)	OP3 (RA3)	OP2 (RA2)	OP1 (RA1)	OP0 (RA0)
3	R	Row Address ([ROW0]:OP0)							

ECC Register 4

ER#	Access	OP7	OP6[(1)] (RA14)	OP5 (RA13)	OP4 (RA12)	OP3 (RA11)	OP2 (RA10)	OP1 (RA9)	OP0 (RA8)
4	R	Reserved	Row Address						

Note:

1. OP6 bit is don't care at x16 org.
2. **READ command must be provided to ACTIVE BANK only to store valid ECC Event location.**

ECC Register 5

ER#	Access	OP7	OP6	OP5	OP4	OP3(1)	OP2(1)	OP1(1)	OP0
5	**R/W**	Reserved			CLRECC	ERR TYPE		ERRON	ECCON

Note:

1. OP1, OP2, and OP3 will be valid for the B2, B3 packages only because B2, and B3 packages support ERR pin. See the Ordering Information details.

ER5 is the only register to allow both Write and Read operations. When the ER5 register is accessed by MR3 programming, Read Data can be accessed through DQ pins with READ or RDAP command after MPR selection, but write data must be input via A5 to A9 address pins during MR3 programming.

- ECCON (OP0): ECC Circuit ON when OP0= 1, OFF when OP0 = 0.
  - Default : OP0 ="1"
  - When ECC is disabled (ECCON is "0"), ERR Signal is disabled. ECC functionality disabled.

Note: ECC is permitted to turn On (OP0 0 → 1), or turn Off (OP 1 → 0) only when DRAM is idle.

- ERRON (OP1): ERR Signal ON when OP1 = 1, OFF when OP1 = 0.
  - Default OP1 is "0"; it means ERR Signal is disabled

Note: ERR signal will be Enabled only when both OP0 and OP1 are "11".

- ERR TYPE OP [3:2]: Set ECC Event type for ERR signal; 1-bit ECC Event, 2-bit ECC Event, or any of ECC Event.
  - 00: 1-bit ECC Event **(Default)**
  - 01: 2-bit ECC Event
  - 10: Any kind of ECC Event
  - 11: Reserved.

- CLR ECC (OP4): ECC Event Record will be Cleared when OP4 = "1". Default value for OP4 is "0", do not clear event record.
  - When a clear ECC operation has completed, OP4 is returned to "0" automatically. This clears the ER0 OP[7:0] bits (ECC Event, ECC Type, 1-Bit counter, and 2-Bit counter). Also, the ERR will be cleared, if High.

10.2 ECC Register Selection by MR3 Programming

ECC registers can be accessed by MR3 programming of BA0, BA1, A0, A1, A3, A4 together with A2=1 like shown in the table below. The values of A0, A1, A3, A4 are used to select among the specific MPR registers.

A2	A0, A1, A3, A4
Enable MPR when A2=1	**Select one of the MPR Registers**

When accessing an ECC register for a Read operation, valid inputs to A0 to A4 are required for specific ECC register selection. After that, Read (RD) or RDA command will output the ECC register values through the DQ pins.

While accessing ER 5 register for write operation, valid input data through A9 to A5 pins must be inserted simultaneously with MR3 programming of valid inputs (A4 to A0 = **11111**).

BA1	BA0	A4	A3	A2	A1	A0	MPR Location
1	1	0	0	1	x	x	Select "Predefined Pattern" for training
1	1	0	1	1	0	0	Select ECC Register 0 for Read
1	1	0	1	1	0	1	Select ECC Register 1 for Read
1	1	0	1	1	1	0	Select ECC Register 2 for Read
1	1	0	1	1	1	1	Select ECC Register 3 for Read
1	1	1	0	1	0	0	Select ECC Register 4 for Read
1	1	1	0	1	0	1	Select ECC Register 5 for Read(1)
1	1	1	1	1	0	0	Reserved
1	1	1	1	1	0	1	Reserved
1	1	1	1	1	1	0	Reserved
1	1	1	1	1	1	1	Write ECC Register 5 (1, 2) by MR3 Programming (Write)

Notes:

1. When ER5 register is accessed by MR3 programming, Read Data can be accessed through DQ pins with READ or RDAP command after MPR selection by MR3 programming, but write data must be input via A9 to A5 address pins **simultaneously with MR3 programming**.
   When ER5 Register is accessed through optional I2C interface, read/write operation can be performed through I2C interface.
2. BA2, A5-A15 must be programmed to 0 during MRS except for Write ECC Register 5 operation. During Write ECC Register 5 operation, BA2, A10-A15 must be programed to 0. A5-A9 will be used for write data into ECC Register 5.

10.3 ECC Register Read, Write Operation with MR3 Programming.

READ OPERATION

Once MPR is enabled (MR3 bit A2 = 1), any subsequent RD or RDA commands will redirected to the Multi-Purpose Register. The MR3 bits A0, A1, A3, and A4 are used to select a specific MPR register, including any ECC register.

When MPR is enabled, RD or RDA commands are allowed for MPR read operation.

The ECC registers store the below information, and can read out:

- ECC Event information (ER0)
- ECC Event location (ER1~ER4)
- ECC Setting Confirmation (ER5)

Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After any command to MR3 where A2 = 1 (enabling the MPR features), it is necessary to set the MR3 with A2 = 0 before resuming normal operation of the DRAM.

REGISTER VS DQ MAPPING TABLE FOR ECC REGISTER READ OPERATION

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

The above mapping is used for all register read operations.

WRITE OPERATION

ER5 Register write operation is performed simultaneously with MR3 programming (setting of BA0, BA1, A0-A9).

- ER5 Register Selection for Write Operation: MR3 programming of **[A4:A0] = 11111 and [BA0:BA1] = 11.**
- Write Data Input into ER5 Register: MR3 programming of **[A9:A5].**

MODE REGISTER 3 SETTING FOR ER5 REGISTER WRITE OPERATION

BA2	BA1	BA0	A15-A10	A9	A8(2)	A7(2)	A6(2)	A5	A4	A3	A2	A1	A0
0(1)	1	1	0(1)	CLR ECC	ERR TYPE		ERRON	ECCON	1	1	1 MPR Enable	1	1

Notes:

1. **BA2, A10 – A15 are RFU and must be programmed to 0 during MRS.**
2. **MR3 bits A6, A7, A8 are for ERR signal settings. They apply for B2, B3 packages only because these packages support ERR pin. See the Ordering Information for details.**

Below is the mapping table between MR3 bits (A5 - A9) and ECC Register OP Codes for ER5 register write operation.

REGISTER ER5 VS MR3 BIT MAPPING TABLE FOR ECC REGISTER 5 WRITE OPERATION

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved			A9	A8	A7	A6	A5
			CLRECC	ERR TYPE		ERRON	ECCON

10.4 The ERR Signal

The ERR Signal indicates an ECC Event occurrence, and the type of event depend on the ECC Type setting of OP [3:2] in the ER5 register. It is an Asynchronous signal, and it goes HIGH between Q0 of N-1 address and Q7 of address N when ECC Event occurred at ECC Chunk N, and remains HIGH until being cleared by CLR ECC bit “1” (Sticky bit).

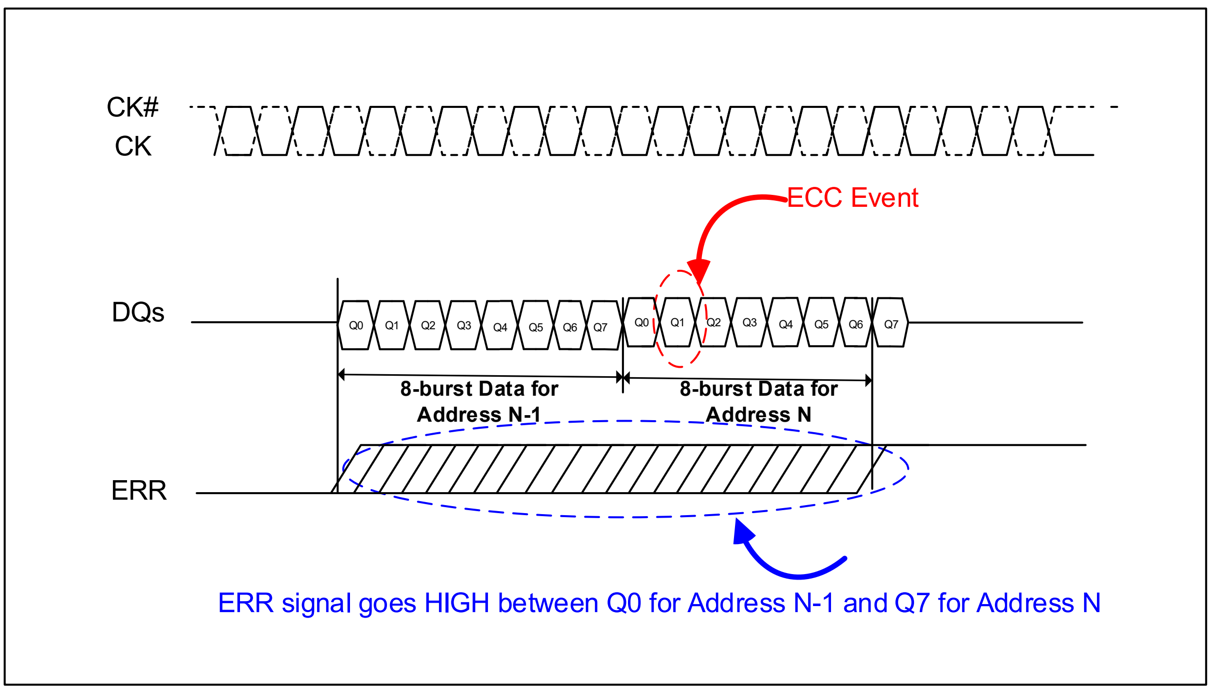
- Enabled by setting ERRON bit of OP1 to “1” in ER5 register
- ERR signal drives “LOW” when ECCON bit (OP0) is “1” & ERRON bit (OP1) is “1”, and no ECC Event.
- ERR signal is HIGH-Z when ECCON bit (OP0) is “0”, or ERRON bit (OP1) is “0”.
- Pin location for ERR pin is H9 in 78 BGA(x8), and L9 in 96 BGA(x16), which is NC in JEDEC DDR3 pin-out.

Below table is for ERR Signal Behavior, and ERR Signal Timing Diagram.

ERR Signal

ER5 Register OP[3:2]	ERR Signal	Status	Remark
00	LOW	No 1-bit Error	
00	HIGH	1-bit Error Detected and Corrected per Half-Byte	Stays HIGH until being cleared by CLR ECC bit.
01	LOW	No 2-bit Error	
01	HIGH	2-bit Error detected per Half-Byte	Stays HIGH until being cleared by CLR ECC bit.
10	LOW	No 1-Bit Error nor 2-bit Error	
10	HIGH	1-Bit Error or 2-bit Error per Half-Byte	Stays HIGH until being cleared by CLR ECC bit. ECC Event type can be verified with ER0.

ERR Signal timing diagram



10.5 I2C and ERR I/O Descriptions

The optional ERR Signal will require the additional connection to an external device, beyond that of standard DDR3. There are 3 connections required, if implementing the I^2C interface.

BALL DESCRIPTIONS for ECC FUNCTIONS

SYMBOL	Pin Location		TYPE	DESCRIPTION
	X8	X16		
SDA	F9	J9	INPUT/ OUTPUT	**Serial Data Address:** This is a bidirectional pin for the two-wire interface. It is open-drain and is intended to be wire-AND'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity. The pin is pulled up internally.
SCL	F1	J1	INPUT	**Serial Clock:** The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input incorporates a Schmitt trigger input for noise immunity. The pin is pulled up internally.
AD0	H1	L1	INPUT	**Device Select Address**: The pin is used to select one of two devices of the same type on the same two-wire bus. To select the device, the address value on the pin must match the corresponding bits contained in the slave address. The pin is pulled up internally, but needs an external pull-up or pull-down connection.
ERR	H9	L9	OUTPUT	**Optional ERR Signal:** Indicates ECC event occurrence. Can be left floating

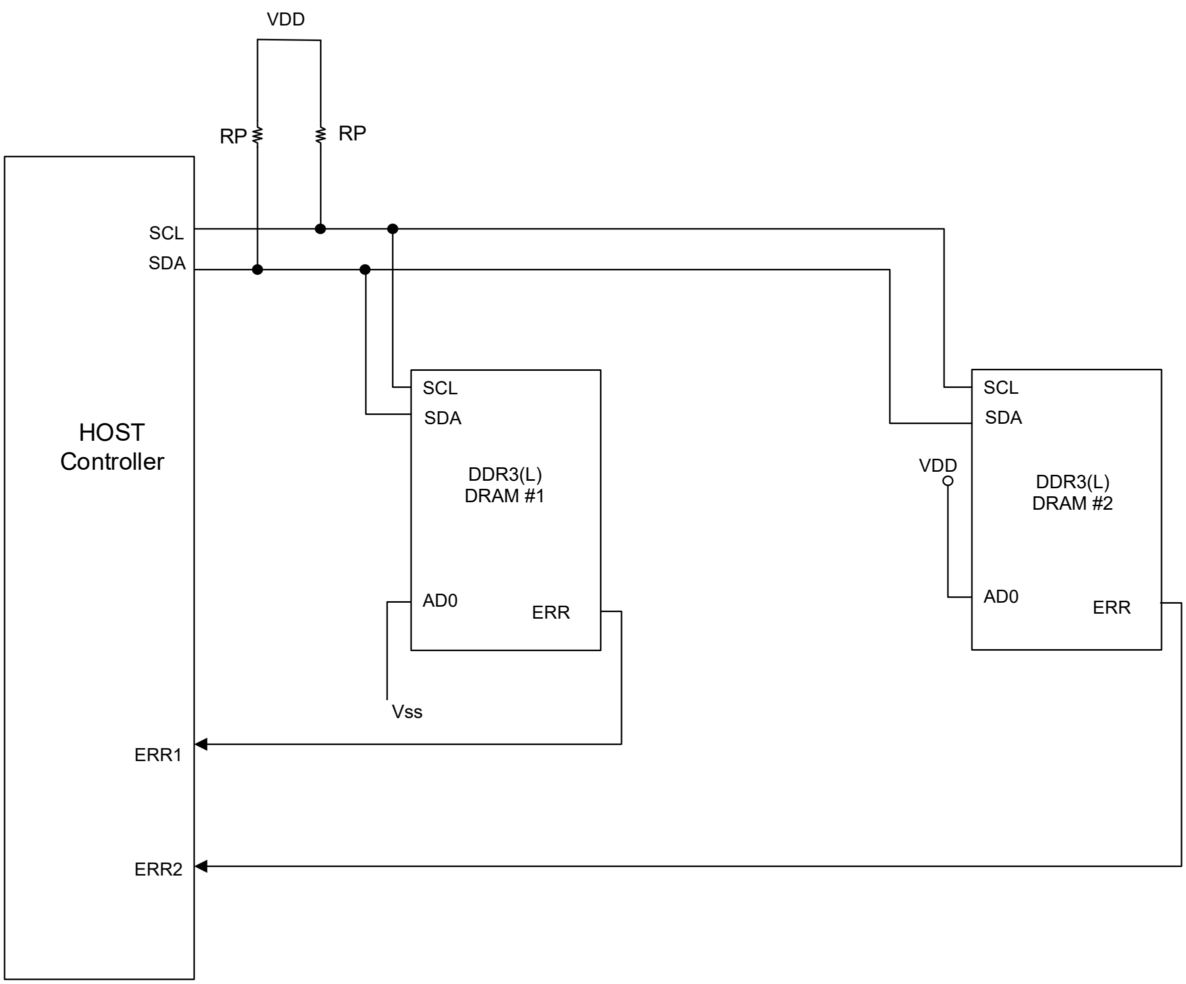
Note: For B3 option, the SDA, SCL, and AD0 are treated as NC (leave floating).

10.6 Two-Wire Interface

ECC registers can be also accessed (R/W) through bidirectional two-wire bus protocol.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are for conditions including START, STOP, data bit, or acknowledge. The device supports both Fast Mode (400 KHz) and Fast Mode Plus (1000 KHz)

System Configuration Using Serial (I^2C) Bus



Notes:

1. Typical Value of Rp is 1K ohm.
2. The VDD and Vss shown above must be at Common levels with VDD and Vss for the DDR3(DDR3L), respectively.

10.6.1 Basic Operations

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will be ready for a new operation.

STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations must be ended with a STOP condition.

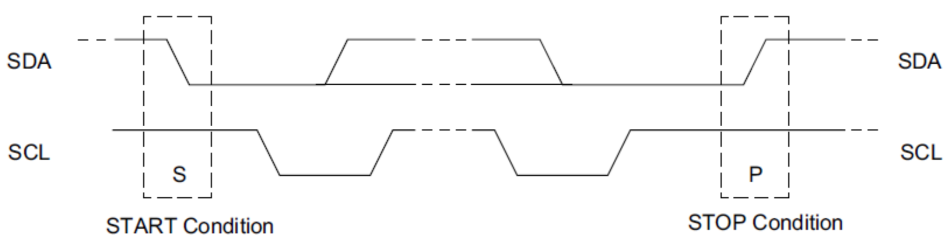
Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the SCL signal. The data on the line must be changed while SCL is LOW.

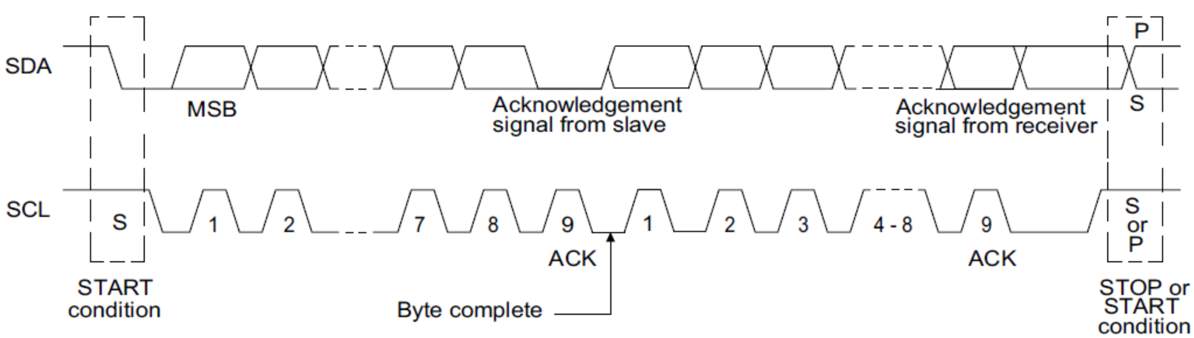
In read operation, no register address is required for current address read operation. If the acknowledge occurs, the device will transfer the next sequential byte. If the acknowledge is not sent, the device will end the read operation.

In write operation, register address is required after slave address. Then the device will accept 8 data bits from the master and sends acknowledge. All data transfer occurs MSB first.

START and STOP Conditions



Data Transfer on the I²C Bus



Acknowledge / No-acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state, the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is no-acknowledge and the operation is aborted in write operation, and end the operation in read operation.

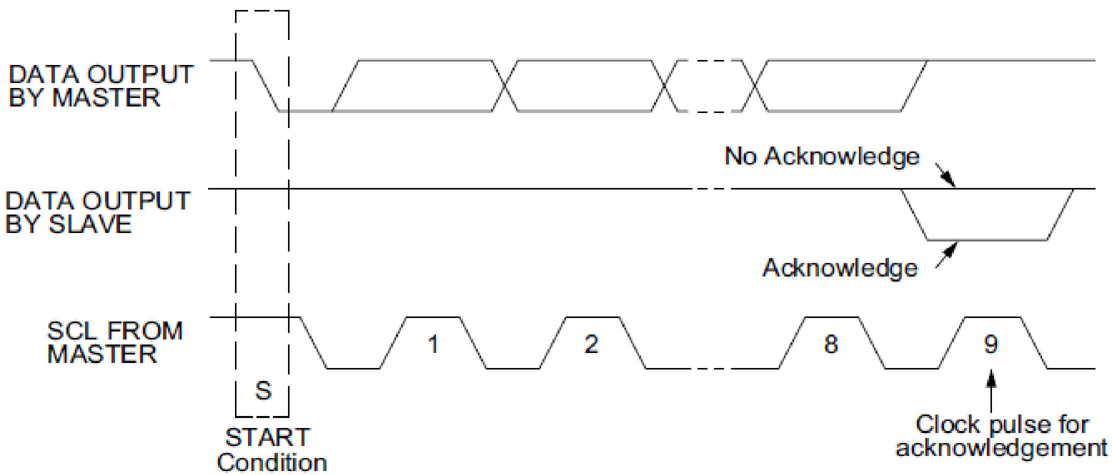
For example, during a read operation, the device will continue to place data on the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte.

If the receiver acknowledges the last byte, this causes the device to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Note:

Acknowledge or No Acknowledge can be followed after normal Read Operation, but Acknowledge only can be followed after normal Write Operation.

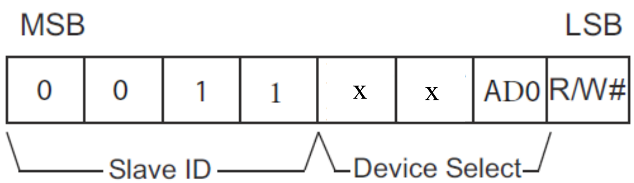
Acknowledge on the I²C Bus



10.6.2 Slave Address

The first byte that the device expects after a START condition is the slave address. As shown in the diagram below, the slave address contains slave ID, the device select address bits, and a bit that specifies if a transaction is a read or a write. Bits 7-4 are device type (Slave ID) and should be set to 0011b for the device. Bits [3:1] are the device select address bits. They must match the corresponding value on the external address pin to select the device. There is one device select address (AD0), bit [1]. Bits[3:2] are "Don't' Care", but are recommended to be set to 00b for consistency. Up to 2 devices can reside on the same two-wire bus by assigning a different address to each. Bit [0] is the read/write bit. R/W#="1" indicates a read operation and R/W#="0" indicates a write operation.

Memory Slave Device Address

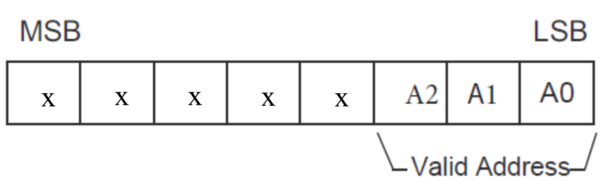


10.6.3 Register Address

After the device acknowledges the slave address, the master can place the register address on the bus for register write operation. The address requires one byte to access the registers (ECC Register 0 ~5).
Only Bits [2:0] are valid register address, and remaining bits [7:3] are "Don't Care", but are recommended to be set to 00000b for consistency.

Note:
Register Address is required after Slave Address in Write Operation (R/W#=0).
But no Register Address is required after Slave Address in Read Operation (R/W#=1).

Register Address



10.6.4 Read Operation

All 6 registers (ER0~ER5) can be accessed with Read Operation.
There are two basic types of read operations. They are current address read and random address read.
In a current address read, the device uses the internal address latch to supply the address.
In a random address read, the user performs a procedure to set the address to a specific value.

Current Address Read and Sequential Read

A current address read uses the existing value in the address latch as a starting place for read operation. The system reads from the address immediately following that of the last operation.

The bus master supplies a slave address to select DRAM with the R/W# bit to a '1' after Start condition for a Read Operation. After that, the device begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

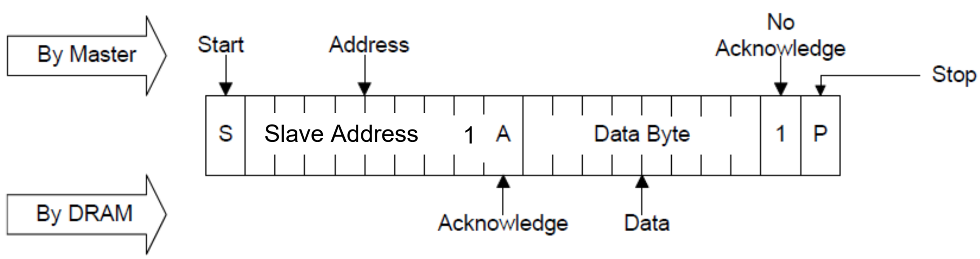
Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte, the internal address counter will be incremented. After each byte of Read data, the bus master acknowledges a byte, then the internal address counter will be incremented. If the internal address reaches 101b, then it will wrap around to 000b on the next read cycle

Termination of Read Operation

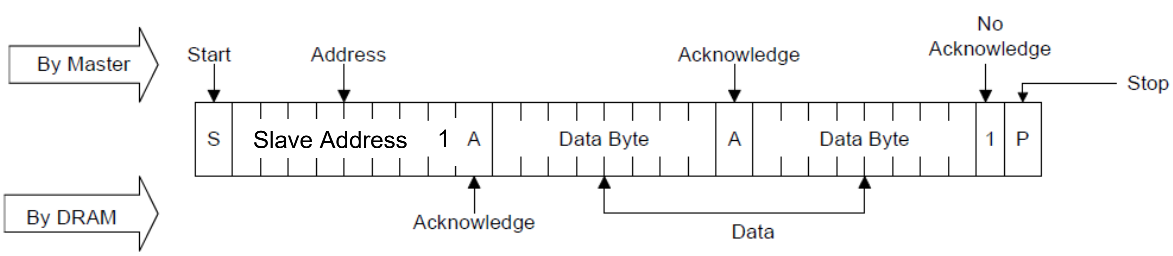
There are 2 ways to terminate a read operation.

1. The bus master issues no acknowledge (1) in the 9th clock cycle and a STOP in the 10th clock cycle.
2. The bus master issues no acknowledge (1) in the 9th clock cycle and a START in the 10th clock cycle.

Current Address Read



Sequential Read



Random Read Operation

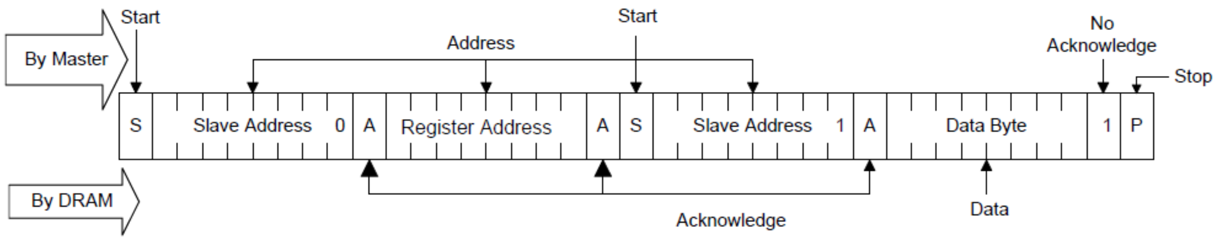
Random read operation allow the master to access any register location in a random manner. This involves using **first two bytes of a write operation to set the internal register address followed by subsequent read operations**.

To perform it, the master sends out the slave address with R/W# bit set to "0". Then the bus master sends the register address to the device as part of a write operation

After the device acknowledges the register address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with slave address bit R/W# set to "1".

The operation is now a random read operation.

Random Read Operation



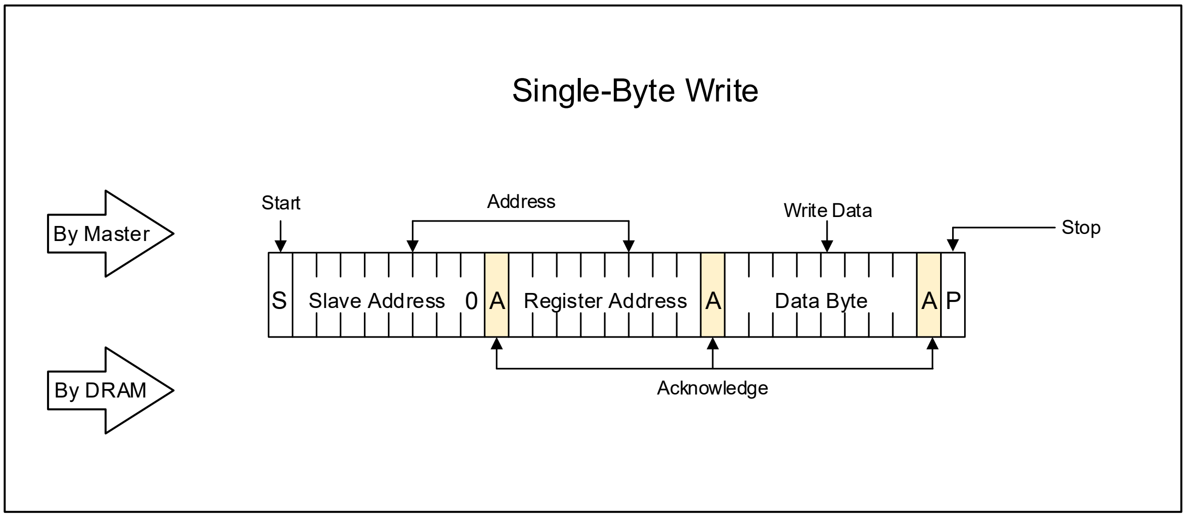
10.6.5 Write Operation

ER5 register (101b) is the only R/W register, so master can perform write operation to ER5 register only. Also no sequential write operation is allowed.
But register address for another registers (ER0~ER4) can be following slave address (R/W#=0) for Random Read Operation.

Write Operation

Write operation begins with a slave address, then followed by a register address. The bus master indicates a write operation by setting the LSB of the slave address (R/W# bit) to a “0”.

After addressing of 101b, the bus master sends a byte of data. Only 1 register (ECC5) can be accessed with write operation, **there is no sequential write operation**.
After a byte write operation, DRAM device must issue an acknowledge (0) in the 9th clock cycle and a STOP or START in the 10th clock to terminate write operation.



10.7 Electrical Characteristics

10.7.1 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Leakage Current (Except for AD0)	V_{IN} = 0V to V_{DD}		-	5	µA
I_{LO}	Output Leakage Current (Except for AD0)	V_{IN} = 0V to V_{DD}		-	5	µA
V_{IL}	Input Low Voltage		-0.3	-	0.3V_{DD}	V
V_{IH}	Input High Voltage		0.7V_{DD}	-	V_{DD} + 0.3	V
V_{OL} (1)	Output Low Voltage (ERR and SDA)	I_{OL} = 3 mA	-	-	0.4	V
Rin (2)	Input Resistance for AD0	For V_{IN} = V_{IL} (Max)	50	-		K ohm
		For V_{IN} = V_{IH} (Min)	1	-		M ohm

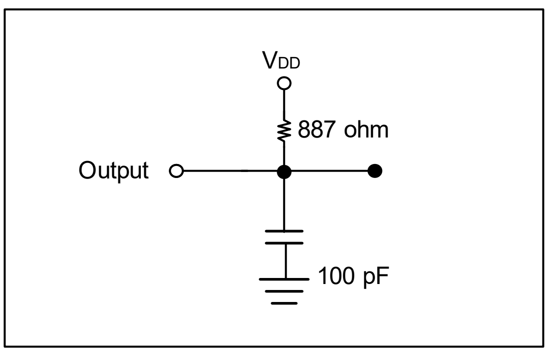
Notes:

1. The device does not meet NXP I2C specification in the Fast-Mode Plus (1MHz) for IOL of 20mA at VOL of 0.4V.
2. The input pull-down circuit is strong (50 Kohm) when input voltage is below V_{IL} and weak (1 M.ohm) when input voltage is above V_{IH}.

PIN CAPACITANCE

Parameter	Symbol	Test Condition	Max	Units
Input capacitance (SCL)	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
I/O capacitance (SDA)	$C_{I/O}$		8	pF

AC TEST LOADS



AC TEST CONDITIONS

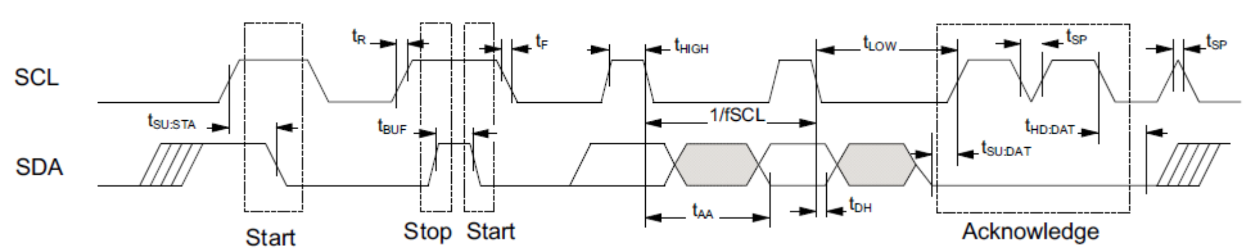
Input pulse levels…………………………………………10% and 90% of VDD
Input rise and fall times………………………………..10ns
Input and Output timing reference levels ……..0.5 x VDD
Output load capacitance ………………………………..100pF

10.7.2 AC Switching Characteristics

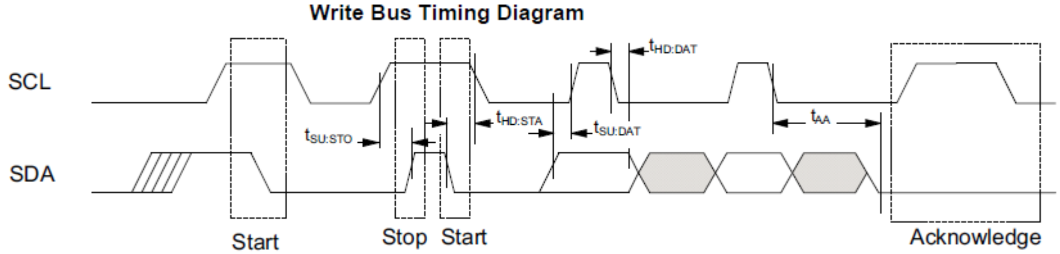
Parameter[1]	Symbol	Fast-mode		Fast-mode+[3]		unit	notes
		Min	Max	Min	Max		
SCL Clock frequency	tSCL	-	0.4	-	1.0	MHz	2
Start condition Setup time for repeated Start	tSU, STA	600	-	260	-	ns	
Start condition Hold time	tHD, STA	600	-	260	-	ns	
Clock LOW period	tLOW	1300	-	500	-	ns	
Clock HIGH period	tHIGH	600	-	260	-	ns	
Data in Setup time	tSU, DAT	100	-	50	-	ns	
Data in Hold time	tHD, DAT	0	-	0	-	ns	
Data output Hold time (from SCL at V_{IL})	tDH	0	-	0	-	ns	
Input Rise time	tR	20	300	-	120	ns	4
Input Fall time	tF	20*(VDD/5.5V)	300	20*(VDD/5.5V)	120	ns	4
Stop condition Setup time	tSU, STO	260	-	260	-	ns	
SCL LOW to SDA Data Out Valid	tAA	-	900	-	450	ns	
ACK Output Valid time	tVD, ACK	-	900	-	450	ns	
Output Fall time from V_{IH}min to V_{IL} max	tOF	20*(VDD/5.5V)	300	20*(VDD/5.5V)	120	ns	4
Bus Free before new transmission	tBUF	1300	-	500	-	ns	
Noise suppression time constant on SCL, SDA	tSP	0	50	0	50	ns	

Notes:
1. Test conditions assume signal condition time of 10ns or less, timing reference levels of VDD/2, input pulse levels of 0V to VDD (typ), and output loading of specified IOL and 100pF load capacitance.
2. The speed related specifications are guaranteed characteristics points along a continuous curve of operation from DC to fSCL (max).
3. Bus Load Considerations (C_B) : C_B < 550 pF for I2C Clock Frequency (SCL) = 1000KHz
4. These parameters are guaranteed by design, and not tested.

Read Bus Timing Diagram



Write Bus Timing Diagram



ORDERING INFORMATION – Valid Part Numbers

IS 43 TR 16256 E C L - 125K B L I

TEMPERATURE RANGE
I = Industrial (-40°C to +95°C)
A1 = Automotive A1 Grade (-40°C to +95°C)
A2 = Automotive A2 Grade (-40°C to +105°C)
A25 = Automotive A25 Grade (-40°C to +115°C)
A3 = Automotive A3 Grade (-40°C to +125°C)

PACKAGING CONTENT
L = **RoHS compliant**

Package Type
B **= BGA**
B2 =BGA with ERR, I2C Interface
B3 = BGA with ERR, MR3 Interface
B4 = BGA with I2C Interface

Speed Grade
125L = 1600MT/s, CL=12
125K = 1600MT/s, CL=11
107N = 1866MT/s, CL=14

VDD
L = 1.35V DDR3
Blank = 1.5V DDR3

Die Rev.
C = Die Rev. C

ECC support
E = On Chip ECC
Blank = No ECC

ORG. & Density
16256 = 256Mb x 16 (4Gb)
85120 = 512Mb x 8 (4Gb)

Device Type
TR = DDR3 DRAM

Product Family
43 = DDR DRAM
46 = Automotive DDR DRAM

ISSI Prefix
IS = Integrated Silicon Solution Inc.

ORDERING INFORMATION, 256Mbx16, 1.5V (DDR3)

256Mb x 16 - Industrial Range: (-40°C < Tc < 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS43TR16256EC-125LB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256EC-125LB3LI	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS43TR16256EC-125KB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256EC-125KB3LI	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS43TR16256EC-107NB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256EC-107NB3LI	96-ball BGA, green, ERR, MR3

256Mb x 16 – A1 Range: (-40°C < Tc < 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256EC-125LB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125LB3LA1	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256EC-125KB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125KB3LA1	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256EC-107NB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-107NB3LA1	96-ball BGA, green, ERR, MR3

256Mb x 16 – A2 Range: (-40°C < Tc < 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256EC-125LB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125LB3LA2	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256EC-125KB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125KB3LA2	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256EC-107NB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-107NB3LA2	96-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 256Mbx16, 1.5V (DDR3)

256Mb x 16 – A25 Range: (-40°C ≤ Tc ≤ 115°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256EC-125LB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125LB3LA25	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256EC-125KB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-125KB3LA25	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256EC-107NB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256EC-107NB3LA25	96-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 256Mbx16, 1.35V (DDR3)

256Mb x 16 - Industrial Range: (-40°C ≤ Tc ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS43TR16256ECL-125LB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256ECL-125LB3LI	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS43TR16256ECL-125KB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256ECL-125KB3LI	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS43TR16256ECL-107NB2LI	96-ball BGA, green, ERR, I2C
		IS43TR16256ECL-107NB3LI	96-ball BGA, green, ERR, MR3

256Mb x 16 – A1 Range: (-40°C ≤ Tc ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256ECL-125LB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125LB3LA1	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256ECL-125KB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125KB3LA1	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256ECL-107NB2LA1	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-107NB3LA1	96-ball BGA, green, ERR, MR3

256Mb x 16 – A2 Range: (-40°C ≤ Tc ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256ECL-125LB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125LB3LA2	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256ECL-125KB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125KB3LA2	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256ECL-107NB2LA2	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-107NB3LA2	96-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 256Mbx16, 1.35V (DDR3)

256Mb x 16 – A25 Range: (-40°C ≤ Tc ≤ 115°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256ECL-125LB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125LB3LA25	96-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR16256ECL-125KB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-125KB3LA25	96-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR16256ECL-107NB2LA25	96-ball BGA, green, ERR, I2C
		IS46TR16256ECL-107NB3LA25	96-ball BGA, green, ERR, MR3

256Mb x 16 – A3 Range: (-40°C ≤ Tc ≤ 125°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR16256ECL-125LB2LA3	96-ball BGA, green, ERR, I2C
1600MT/s	11-11-11	IS46TR16256ECL-125KB2LA3	96-ball BGA, green, ERR, I2C
1866MT/s	14-13-13	IS46TR16256ECL-107NB2LA3	96-ball BGA, green, ERR, I2C

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 512Mbx8, 1.5V (DDR3)

512Mb x 8 - Industrial Range: (-40°C ≤ Tc ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS43TR85120EC-125LB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120EC-125LB3LI	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS43TR85120EC-125KB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120EC-125KB3LI	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS43TR85120EC-107NB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120EC-107NB3LI	78-ball BGA, green, ERR, MR3

512Mb x 8 – A1 Range: (-40°C ≤ Tc ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120EC-125LB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125LB3LA1	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120EC-125KB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125KB3LA1	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120EC-107NB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-107NB3LA1	78-ball BGA, green, ERR, MR3

512Mb x 8 – A2 Range: (-40°C ≤ Tc ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120EC-125LB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125LB3LA2	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120EC-125KB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125KB3LA2	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120EC-107NB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-107NB3LA2	78-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 512Mbx8, 1.5V (DDR3)

512Mb x 8 – A25 Range: (-40°C ≤ Tc ≤ 115°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120EC-125LB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125LB3LA25	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120EC-125KB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-125KB3LA25	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120EC-107NB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120EC-107NB3LA25	78-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 512Mbx8, 1.35V (DDR3)

512Mb x 8 - Industrial Range: (-40°C < Tc < 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS43TR85120ECL-125LB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120ECL-125LB3LI	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS43TR85120ECL-125KB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120ECL-125KB3LI	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS43TR85120ECL-107NB2LI	78-ball BGA, green, ERR, I2C
		IS43TR85120ECL-107NB3LI	78-ball BGA, green, ERR, MR3

512Mb x 8 – A1 Range: (-40°C < Tc < 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120ECL-125LB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125LB3LA1	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120ECL-125KB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125KB3LA1	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120ECL-107NB2LA1	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-107NB3LA1	78-ball BGA, green, ERR, MR3

512Mb x 8 – A2 Range: (-40°C < Tc < 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120ECL-125LB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125LB3LA2	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120ECL-125KB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125KB3LA2	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120ECL-107NB2LA2	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-107NB3LA2	78-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

ORDERING INFORMATION, 512Mbx8, 1.35V (DDR3)

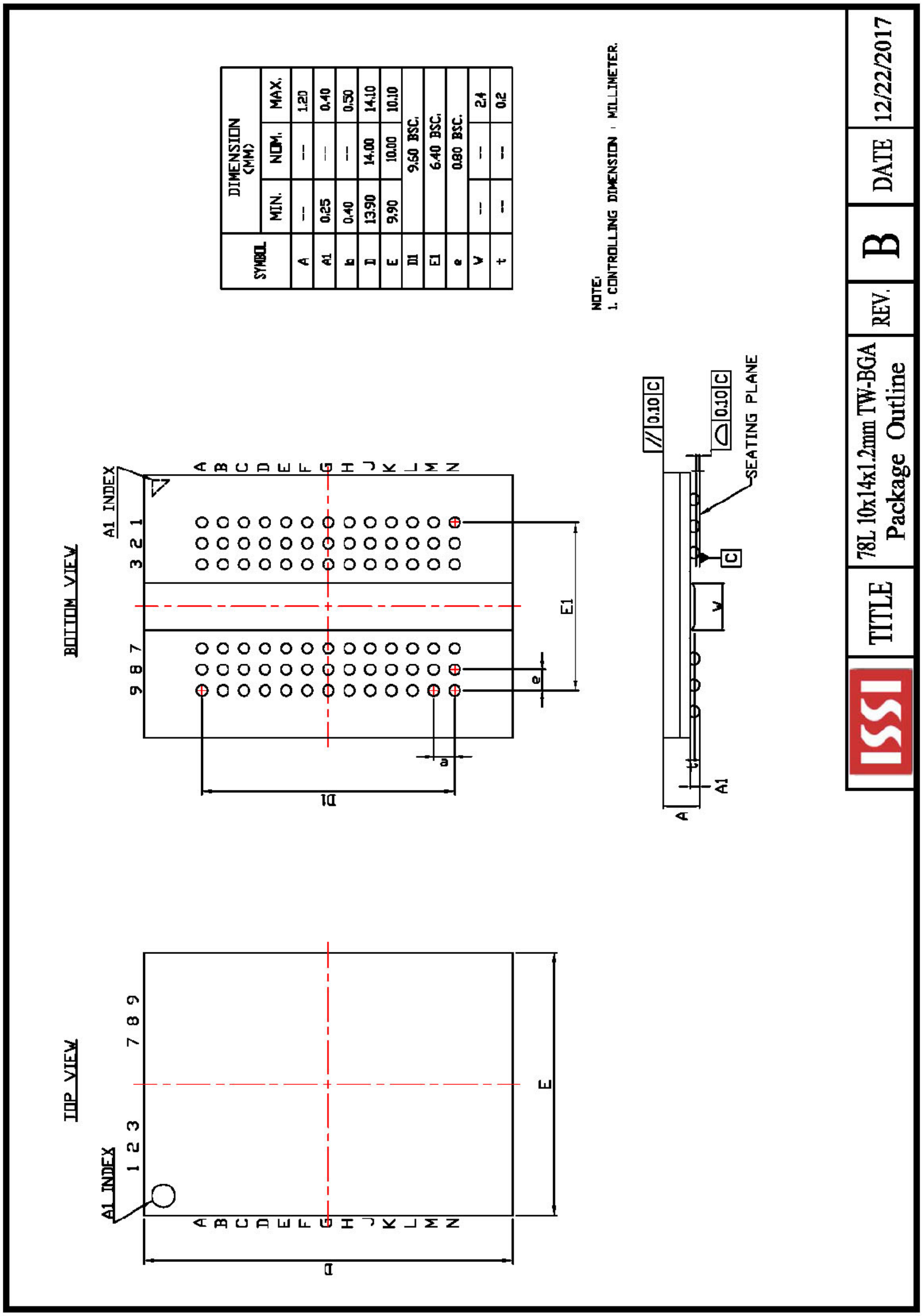
512Mb x 8 – A25 Range: (-40°C ≤ Tc ≤ 115°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1600MT/s	12-11-11	IS46TR85120ECL-125LB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125LB3LA25	78-ball BGA, green, ERR, MR3
1600MT/s	11-11-11	IS46TR85120ECL-125KB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-125KB3LA25	78-ball BGA, green, ERR, MR3
1866MT/s	14-13-13	IS46TR85120ECL-107NB2LA25	78-ball BGA, green, ERR, I2C
		IS46TR85120ECL-107NB3LA25	78-ball BGA, green, ERR, MR3

Notes:
Contact ISSI for availability of options.
The terminology "green" refers to the package being (RoHS Compliant, Halogen-free) and TSCA Compliant.

PACKAGE OUTLINE DRAWING

78-ball BGA (10mm x 14mm)

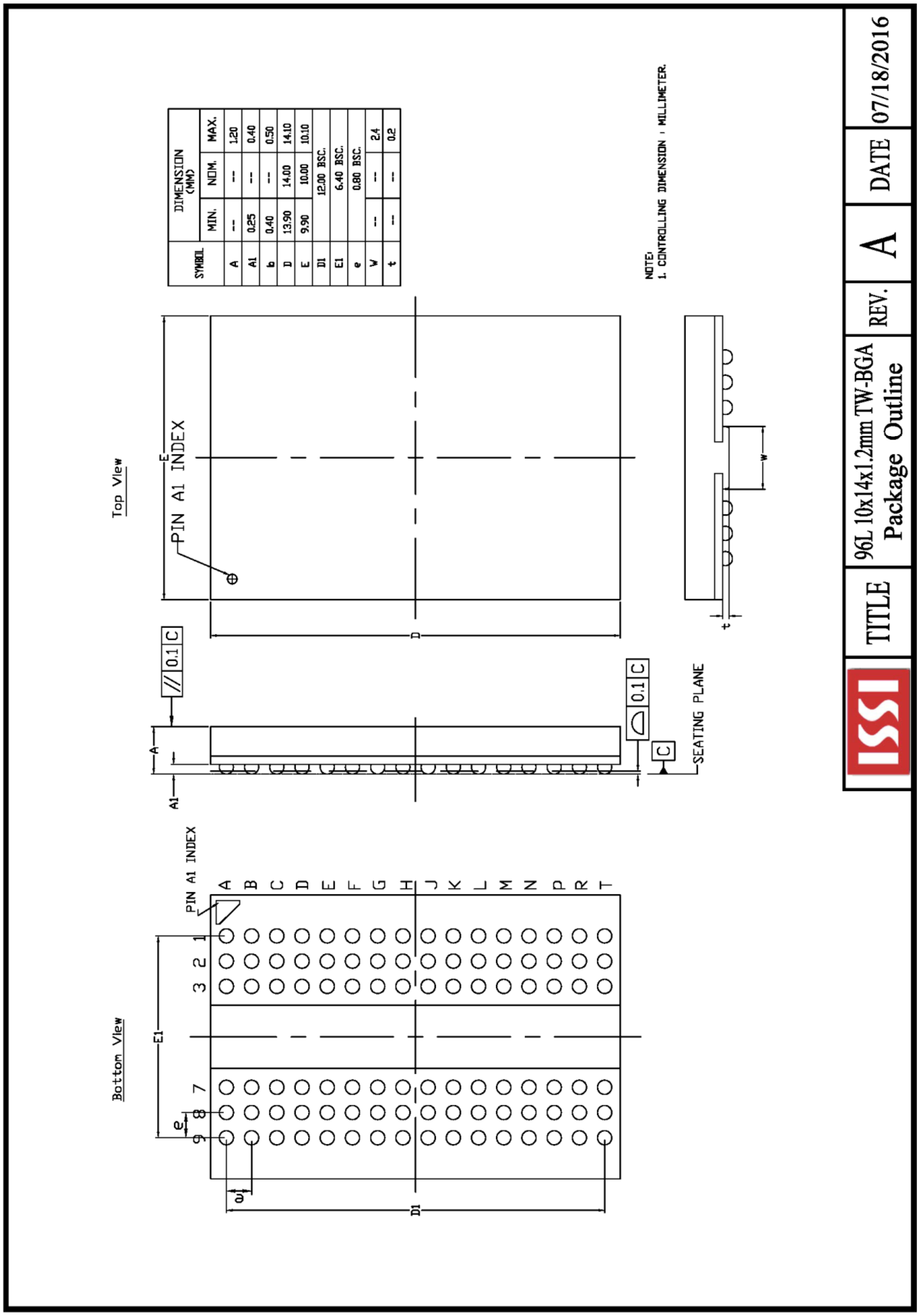


SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.25	--	0.40
b	0.40	--	0.50
D	13.90	14.00	14.10
E	9.90	10.00	10.10
D1		9.50 BSC.	
E1		6.40 BSC.	
e		0.80 BSC.	
v	--	--	2.4
t	--	--	0.2

Long-term Support
World Class Quality

PACKAGE OUTLINE DRAWING

96-ball BGA (10mm x 14mm): 0.8mm x 0.8mm Pitch (x16)



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.25	--	0.40
b	0.40	--	0.50
D	13.90	14.00	14.10
E	9.90	10.00	10.10
D1		12.00 BSC.	
E1		6.40 BSC.	
e		0.80 BSC.	
W	--	--	2.4
t	--	--	0.2