REF50xx Low-Noise, Very Low Drift, Wide V_{IN} Precision Voltage Reference

1 Features

- Low temperature drift (maximum):
  - **Enhanced-grade (new): 2.5ppm/°C**
  - High-grade: 3ppm/°C
  - Standard-grade: 8ppm/°C
- High accuracy (maximum):
  - Enhanced-grade: 0.025%
  - High-grade: 0.05%
  - Standard-grade: 0.1%
- Low noise:
  - Enhanced-grade: 0.5µV_{PP}/V
  - High/standard-grade: 3µV_{PP}/V
- Excellent long-term stability:
  - 22ppm after first 1000 hours (SOIC-8)
  - 50ppm after first 1000 hours (VSSOP-8)
- Wide input voltage support:
  - Enhanced-grade: 42V
  - High/standard-grade: 18V
- High-output current: ±10mA
- Temperature range: -40°C to 125°C

2 Applications

- Precision data acquisition systems
- Semiconductor test equipment
- Industrial process controls
- Medical instrumentation
- Pressure and temperature transmitters
- Lab and field instrumentation

3 Description

The REF50xx is a family of low-noise, low-drift, very high precision voltage references. The references are capable of both sinking and sourcing current, and have excellent line and load regulation.

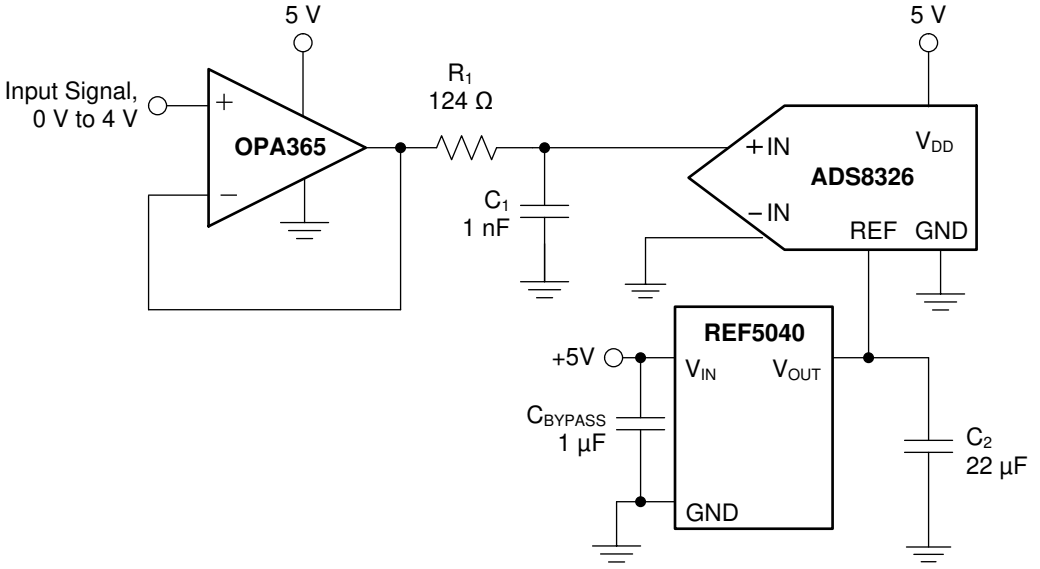
Achieve excellent temperature drift (2.5ppm/°C) and high accuracy (0.025%) using proprietary design techniques. These features, combined with very low flicker noise (0.5µV_{PP}/V), make the REF50xx family an excellent choice for use in high-precision data acquisition systems. REF50 family is available in enhanced grade (REF50xxEI), high grade (REF50xxI), and standard grade (REF50xxAI). The reference voltages are offered in 8-pin SOIC and VSSOP packages and are specified from –40°C to 125°C.

For detailed comparison across various grades, refer to Table 4-2.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
REF50xxI REF50xxAI	D (SOIC, 8)	4.90mm × 3.91mm
	DGK (VSSOP, 8)	3.00mm × 3.00mm
REF50xxEI	D (SOIC, 8)	4.90mm × 3.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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Simplified Schematic

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4 Device Comparison Table

Table 4-1. Device V_{OUT} Comparison

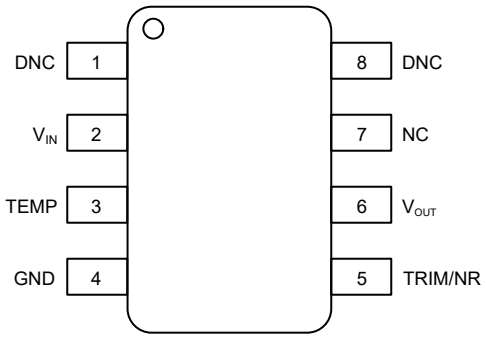
PRODUCT					Voltage
SOIC (8)			VSSOP (8)		
N/A	REF5020ID	REF5020AID	REF5020IDGK	REF5020AIDGK	2.048V
REF5025EID	REF5025ID	REF5025AID	REF5025IDGK	REF5025AIDGK	2.5V
REF5030EID	REF5030ID	REF5030AID	REF5030IDGK	REF5030AIDGK	3V
REF5040EID	REF5040ID	REF5040AID	REF5040IDGK	REF5040AIDGK	4.096V
REF5045EID	REF5045ID	REF5045AID	REF5045IDGK	REF5045AIDGK	4.5V
REF5050EID	REF5050ID	REF5050AID	REF5050IDGK	REF5050AIDGK	5.0V
N/A	REF5010ID	REF5010AID	REF5010IDGK	REF5010AIDGK	10.0V

Table 4-2. Device Performance Comparison

Device	Grade	Temperature Coefficient	Initial Accuracy	Noise	V_{IN} Max	Quiescent Current Max
REF50xxEI	Enhanced	2.5ppm/ºC	±0.025%	$0.5\mu V_{PP}/V$	42V	480µA
REF50xxI	High	3ppm/ºC	±0.05%	$3\mu V_{PP}/V$	18V	1.2mA
REF50xxAI	Standard	8ppm/ºC	±0.1%	$3\mu V_{PP}/V$	18V	1.2mA

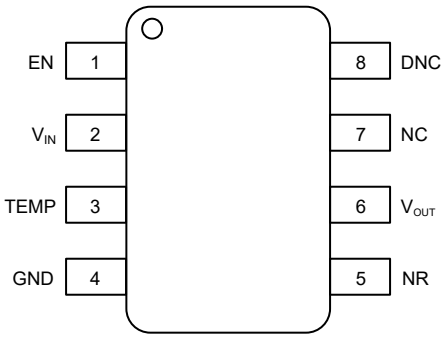
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5 Pin Configuration and Functions



Not to scale

Figure 5-1. REF50xxAI, REF50xxI
8-Pin SOIC, VSSOP
Top View



Not to scale

Figure 5-2. REF50xxEI
8-Pin SOIC
Top View

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	REF50xxI, REF50xxAI	REF50xxEI	
DNC	1, 8	8	Do not connect
EN	-	1	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V or leaving the EN pin floating.
GND	4	4	Ground
NC	7		No internal connection
NC		7	Leave floating or connect to GND
NR	-	5	Noise reduction pin
TEMP	3	3	Temperature monitoring pin. Provides a temperature-dependent output voltage
TRIM/NR	5	-	Output adjustment or noise reduction pin
V_{IN}	2	2	Input supply voltage
V_{OUT}	6	6	Reference voltage output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN} (2)	-0.3	18	V
	V_{IN} (3)	-0.3	48	
Output Voltage	V_{OUT}	-0.3	5.5	V
Operating temperature	(T_A)	–55	125	°C
Junction temperature	(T_J max)		150	
Storage temperature range	(T_{stg})	-65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Specification for REF5xxI and REF50xxAI.
(3) Specification for REF50xxEI.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (3)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	± 3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	± 1000	
	Electrostatic discharge (4)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	± 2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	± 500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) Specification for REF50xxI and REF50xxAI.
(4) Specification for REF50xxEI.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (2)	V_{OUT} + 0.2(1)		18	V
	Input voltage (3)	V_{OUT} + 0.2		42	V
NR	Noise reduction (3)	0		6	V
I_{OUT}	Output current	–10		10	mA
T_A	Operating ambient temperature	–40	25	125	°C

(1) Except for the REF5020, where V_{IN} (minimum) = 2.7V.
(2) Specification for REF50xxI and REF50xxAI.
(3) Specification for REF50xxEI.

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6.4 Thermal Information

THERMAL METRIC[1]		REF50xxEI	REF50xxI , REF50xxAI		UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	115	160.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	63.4	53.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66	57.1	82.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	15.4	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.7	56.2	80.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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6.5 Electrical Characteristics REF50xxI and REF50xxAI

At T_A = 25°C, I_{LOAD} = 0, C_L = 1µF and V_{IN} = (V_{OUT} + 0.2V) to 18V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
V_{OUT}	Output Voltage	REF5020 (V_{OUT} = 2.048V) (1), 2.7V < V_{IN} < 18V		2.048		V
		REF5025		2.5		
		REF5030		3.0		
		REF5040		4.096		
		REF5045		4.5		
		REF5050		5		
		REF5010		10		
Initial Accuracy	High Grade	All voltage options (1)	-0.05		0.05	%
	Standard Grade	All voltage options (1)	–0.1		0.1	%
NOISE						
e_{npp}	Low Frequency noise	f = 0.1Hz to 10Hz		3		μV_{PP}/V
e_n	Output Voltage Noise	f = 10Hz to 1kHz		0.9		μV_{rms}/V
OUTPUT VOLTAGE TEMPERATURE DRIFT						
dV_{OUT}/dT	High grade	T_A = –40°C to 125°C		2.5	3	pm/°C
	Standard grade			3	8	
LINE REGULATION						
$\Delta V_{O(\Delta VI)}$	Line regulation	V_{IN} = (V_{OUT} + 0.2V) to 18V(1)		1	3	ppm/V
		V_{IN} = (V_{OUT} + 0.2V) TO 18V, T_A = –40°C to 125°C(1)		1	5	
LOAD REGULATION						
$\Delta V_{O(\Delta IL)}$	Load regulation	–10mA < I_{OUT} < 10mA, V_{IN} = V_{OUT} + 0.75V(2)		20	30	ppm/mA
		10mA < I_{OUT} < 10mA, V_{IN} = V_{OUT} + 0.75V(2), T_A = –40°C to 125°C			50	
SHORT-CIRCUIT CURRENT						
I_{SC}	Short circuit current	V_{OUT} = 0		25		mA
THERMAL HYSTERESIS						
High grade	VSSOP-8	Cycle 1		50		ppm
		Cycle 2		40		
	SOIC-8	Cycle 1		70		
		Cycle 2		50		
Standard grade	VSSOP-8	Cycle 1		70		
		Cycle 2		40		
	SOIC-8	Cycle 1		90		
		Cycle 2		50		
LONG-TERM STABILITY						
ΔV_{OUT_LTD}	VSSOP-8	0 to 1000 hours		50		ppm
		1000 to 2000 hours		25		
	SOIC-8	0 to 1000 hours		22		
		1000 to 2000 hours		18		
TEMP PIN						
Voltage output				575		mV
Temperature sensitivity		T_A = -40°C to 125°C		2.64		mV/°C

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6.5 Electrical Characteristics REF50xxI and REF50xxAI (continued)

At T_A = 25°C, I_{LOAD} = 0, C_L = 1µF and V_{IN} = (V_{OUT} + 0.2V) to 18V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
TURN-ON SETTLING TIME						
Turn-on settling time		To 0.1% with C_L = 1µF		200		µs
POWER SUPPLY						
V_S	Supply voltage	See note (1)	VOUT + 0.2		18	V
Quiescent current				0.8	1	mA
		–40°C ≤ T_A ≤ 125°C			1.2	
TEMPERATURE RANGE						
Specified range			–40		125	°C
Operating range			–55		125	°C

(1) For VOUT ≤ 2.5V, the minimum supply voltage is 2.7V.
(2) Except for REF5020, where VIN = 3V.

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6.6 Electrical Characteristics REF50xxEI

At T_A = 25°C, I_{LOAD} = 0, C_L = 1µF and V_{IN} = V_{EN} = (V_{OUT} + 0.25V) , unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
V_{OUT}	Output Voltage	REF5025E		2.5		V
		REF5030E		3.0		V
		REF5040E		4.096		V
		REF5045E		4.5		V
		REF5050E		5		V
IA	Initial accuracy	All voltage options	–0.025		0.025	%
dV_{OUT}/dT		T_A = –40°C to 125°C			2.5	ppm/°C
NOISE						
e_{npp}	Low Frequency noise	f = 0.1Hz to 10Hz		0.5		μV_{PP}/V
e_n	Output Voltage Noise	f = 10Hz to 1kHz		0.8		μV_{rms}/V
LINE REGULATION						
$\Delta V_{O(\Delta VI)}$	Line regulation	V_{IN} = (V_{OUT} + 0.2V) to 42V		1	3	ppm/V
		V_{IN} = V_{OUT} + 0.2V to 42V, T_A = –40°C to 125°C		1	5	
LOAD REGULATION						
$\Delta V_{O(\Delta IL)}$	Load regulation	–10mA < I_{OUT} < 10mA, V_{IN} = V_{OUT} + 0.75V		5	25	ppm/mA
		10mA < I_{OUT} < 10mA, V_{IN} = V_{OUT} + 0.75V, T_A = –40°C to 125°C			35	
SHORT-CIRCUIT CURRENT						
I_{SC}	Short circuit current	V_{OUT} = 0		21		mA
THERMAL HYSTERESIS AND LONG-TERM STABILITY						
TH	SOIC-8	Cycle 1		80		ppm
	SOIC-8	Cycle 2		20		ppm
LONG-TERM STABILITY						
ΔV_{OUT_LTD}	SOIC-8	0 to 1000 hours		25		ppm
		1000 to 2000 hours		10		ppm
TEMP PIN						
Voltage output				625		mV
Temperature sensitivity		T_A = -40°C to 125°C		2.64		mV/°C
TURN-ON SETTLING TIME						
Turn-on settling time		To 0.1% with C_L = 1µF		400		µs
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C	0.1			µF
C_L	Stable output capacitor range	–40°C ≤ T_A ≤ 125°C	1		100	µF
POWER SUPPLY						
V_S	Supply voltage	See note	V_{OUT} + 0.2		42	V
Quiescent current				340		µA
		–40°C ≤ T_A ≤ 125°C			480	µA
Quiescent current	Shunt down current	V_{EN} = 0V		10		µA
Enable Voltage	V_{EN}	Active mode (EN = 1)	1.6			V
		Shutdown Mode (EN = 0)			0.5	V
TEMPERATURE RANGE						

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6.6 Electrical Characteristics REF50xxEI (continued)

At T_A = 25°C, I_{LOAD} = 0, C_L = 1µF and V_{IN} = V_{EN} = (V_{OUT} + 0.25V) , unless otherwise noted

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Specified range		–40		125	°C

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6.7 Typical Characteristics: REF50xxI, REF50xxAI

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7 V.

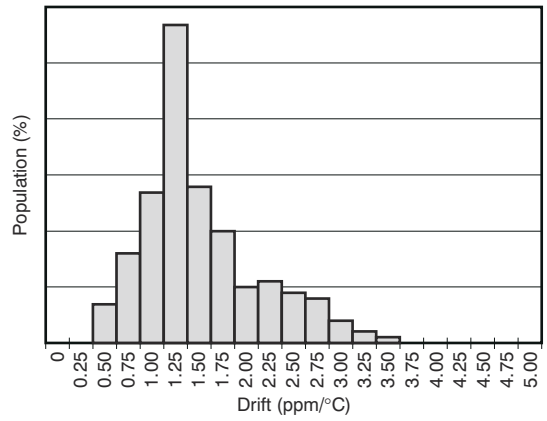


Figure 6-1. Temperature Drift

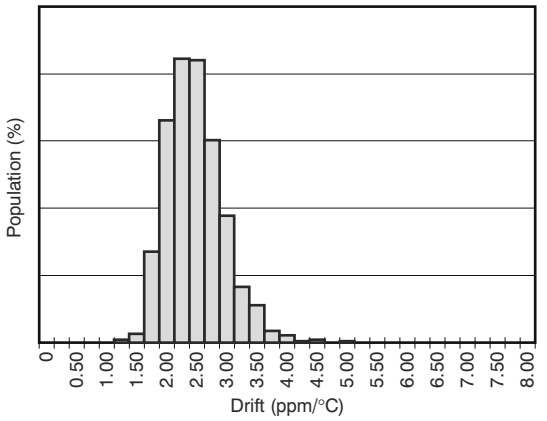


Figure 6-2. Temperature Drift

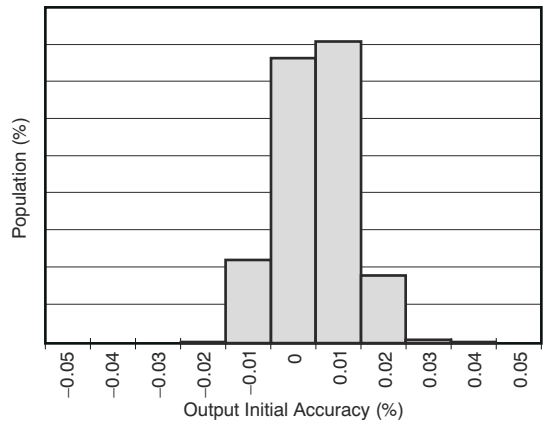


Figure 6-3. Output Voltage Initial Accuracy

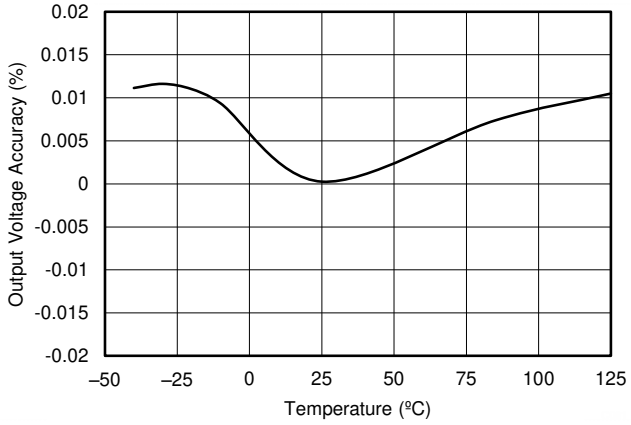


Figure 6-4. Output Voltage Accuracy vs Temperature

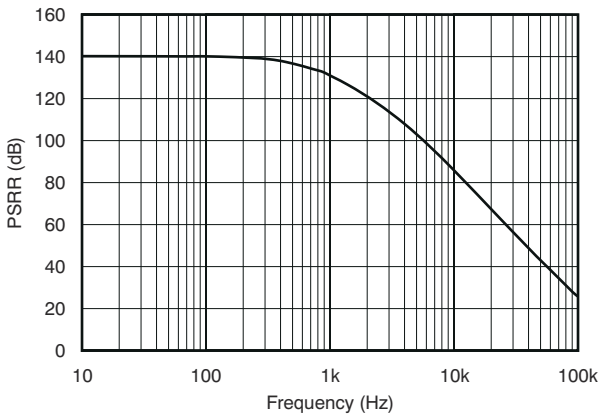


Figure 6-5. Power-Supply Rejection Ratio vs Frequency

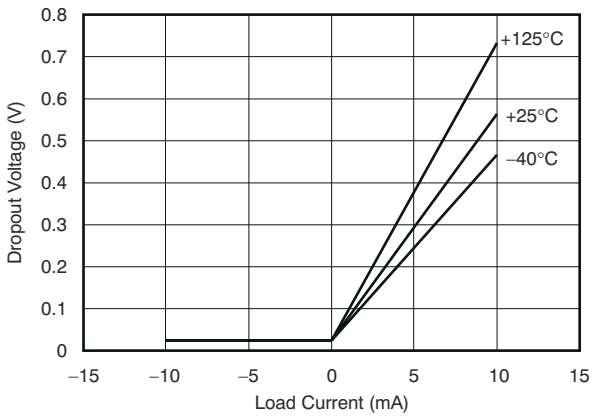


Figure 6-6. Dropout Voltage vs Load Current

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6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7 V.

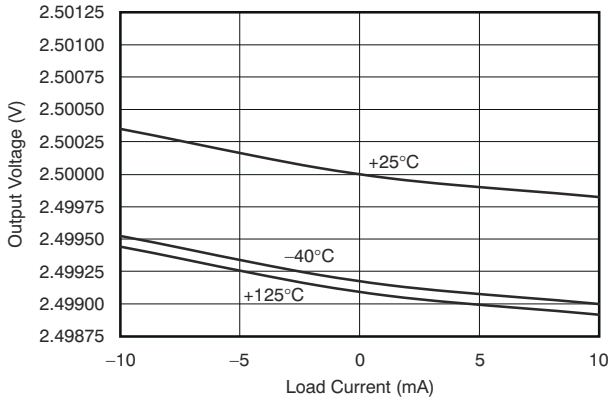


Figure 6-7. REF5025 Output Voltage vs Load Current

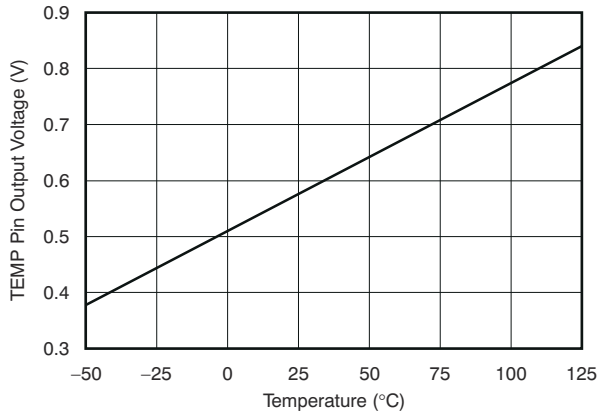


Figure 6-8. Temp Pin Output Voltage vs Temperature

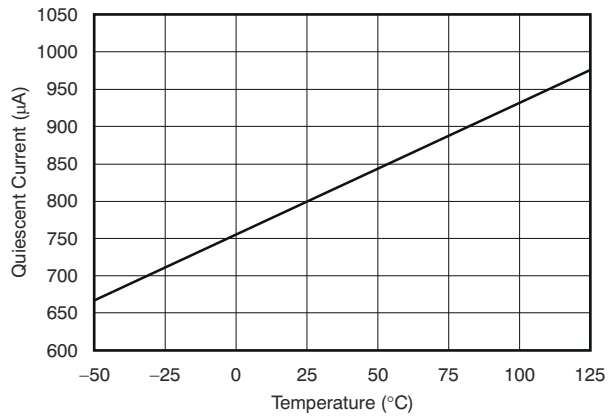


Figure 6-9. Quiescent Current vs Temperature

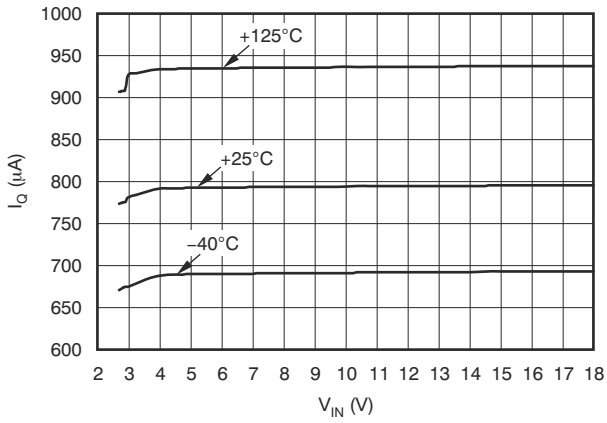


Figure 6-10. Quiescent Current vs Input Voltage

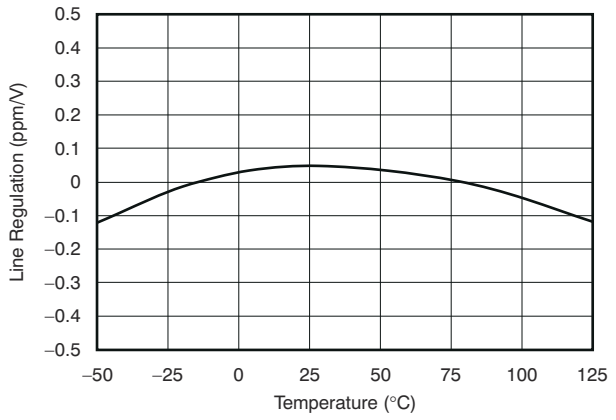


Figure 6-11. Line Regulation vs Temperature

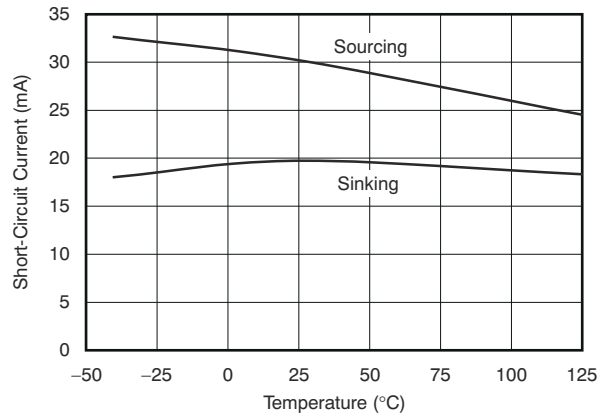


Figure 6-12. Short Circuit Current vs Temperature

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6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7 V.

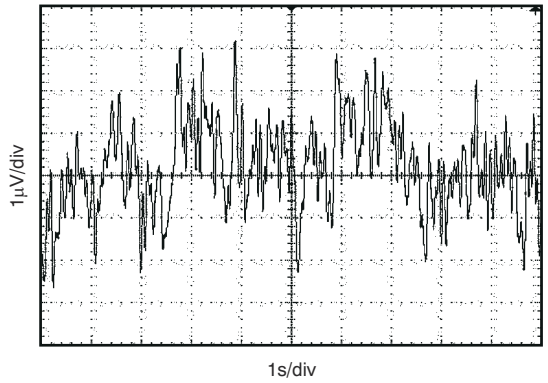


Figure 6-13. 0.1Hz to 10Hz Noise

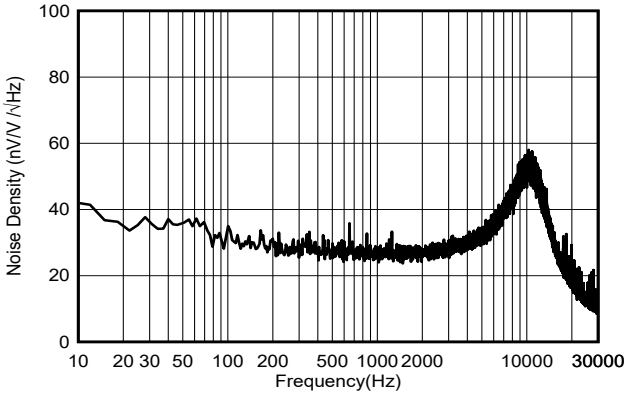
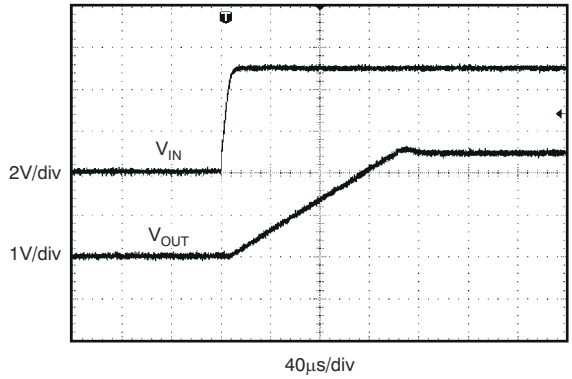
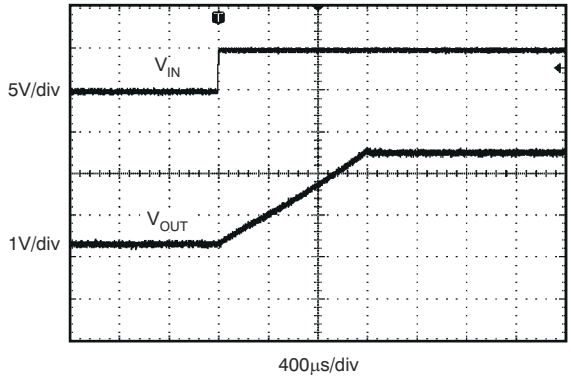


Figure 6-14. Noise Spectral Density



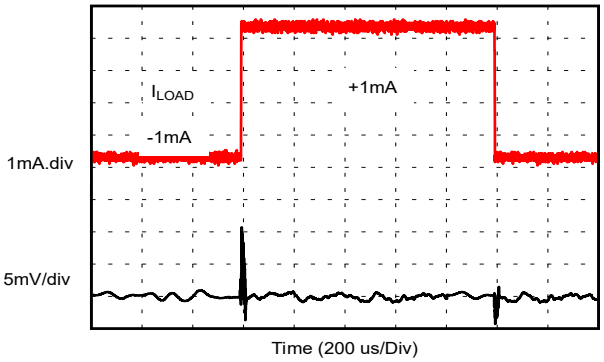
REF5025, C_L = 1µF

Figure 6-15. Start-Up



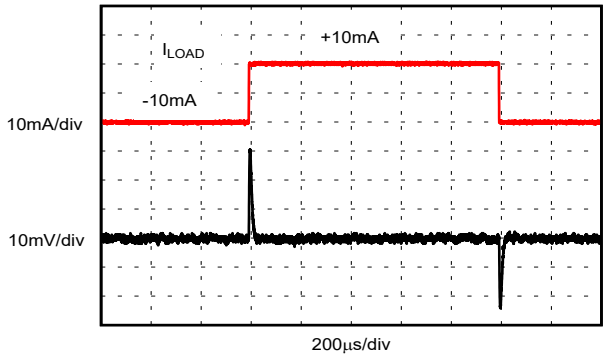
REF5025, C_L = 10µF

Figure 6-16. Start-Up



C_L = 1µF, I_{OUT} = 1mA

Figure 6-17. Load Transient

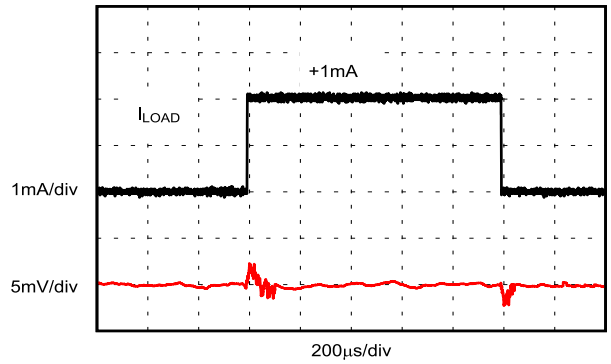


C_L = 1µF, I_{OUT} = 10mA

Figure 6-18. Load Transient

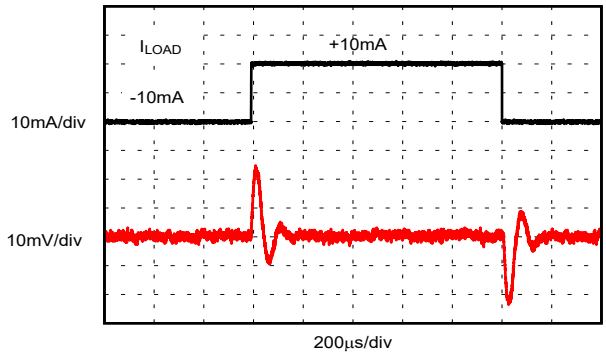
6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7 V.



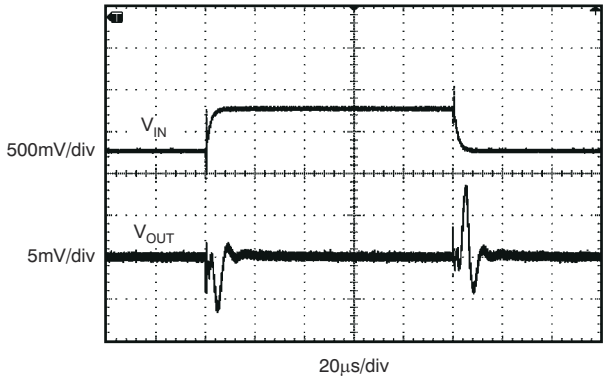
C_L = 10µF, I_{OUT} = 1mA

Figure 6-19. Load Transient



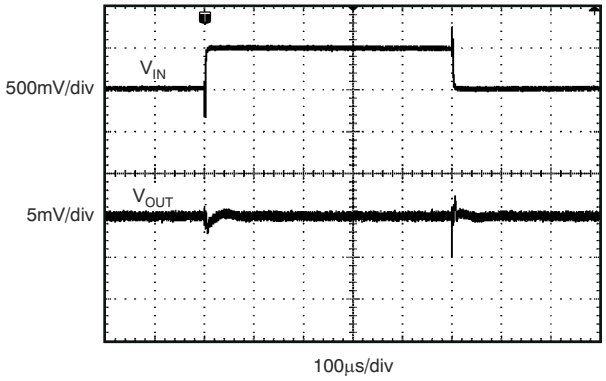
C_L = 10µF, I_{OUT} = 10mA

Figure 6-20. Load Transient



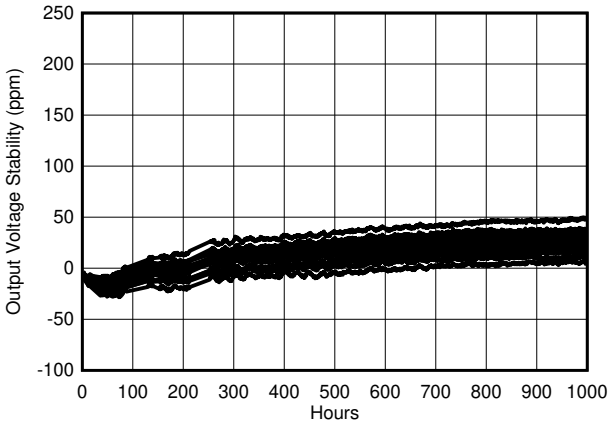
C_L = 1µF

Figure 6-21. Line Transient



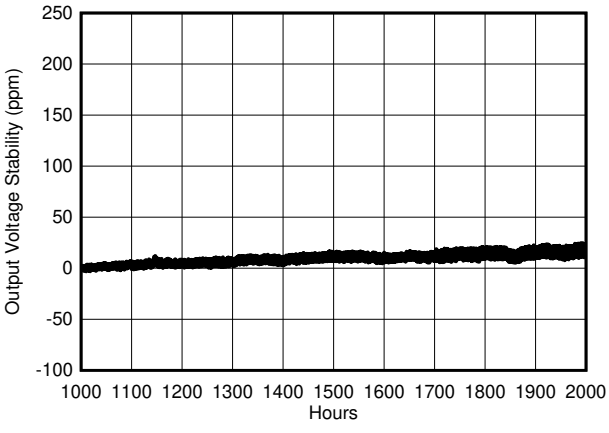
C_L = 10µF

Figure 6-22. Line Transient



VSSOP-8

Figure 6-23. REF50xx Long-Term Stability (First 1000 Hours)



VSSOP-8

Figure 6-24. REF50xx Long-Term Stability (Second 1000 Hours)

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6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7 V.

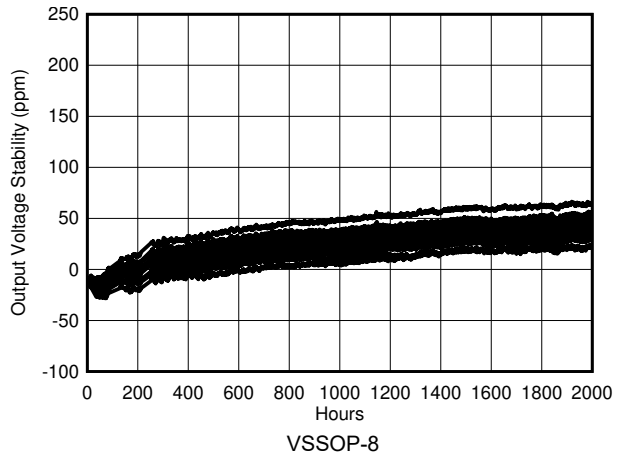


Figure 6-25. REF50xx Long-Term Stability (First 2000 Hours)

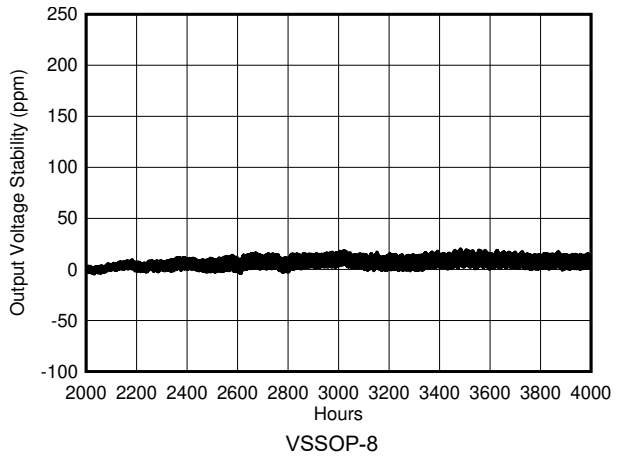


Figure 6-26. REF50xx Long-Term Stability (Second 2000 Hours)

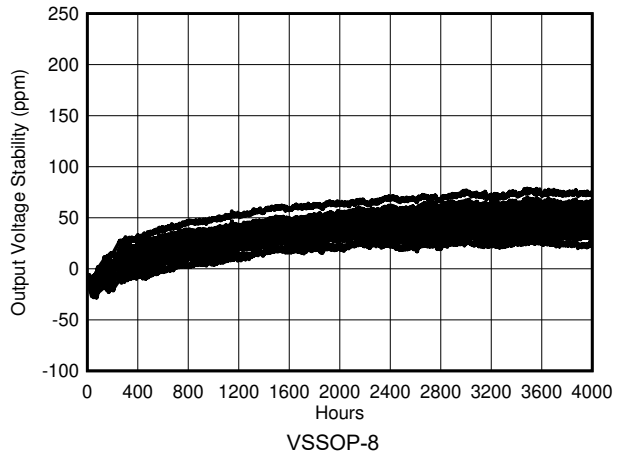


Figure 6-27. REF50xx Long-Term Stability (4000 Hours)

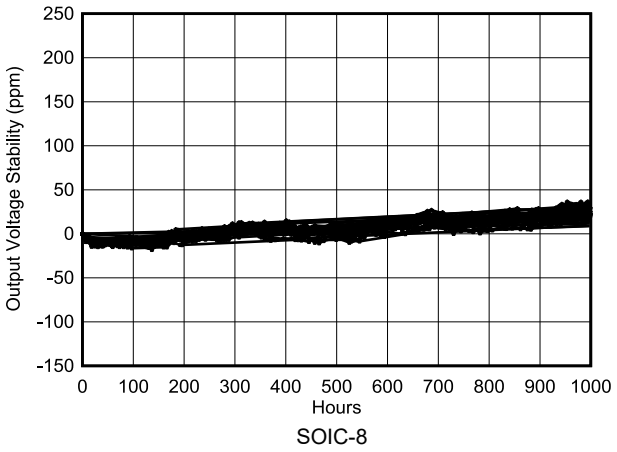


Figure 6-28. REF50xx Long-Term Stability (First 1000 Hours)

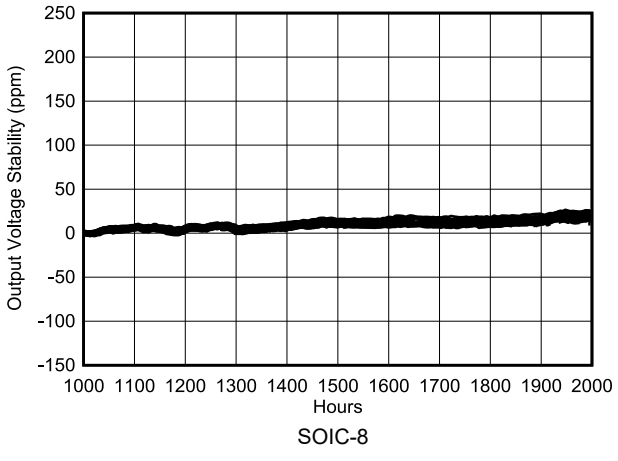


Figure 6-29. REF50xx Long-Term Stability (Second 1000 Hours)

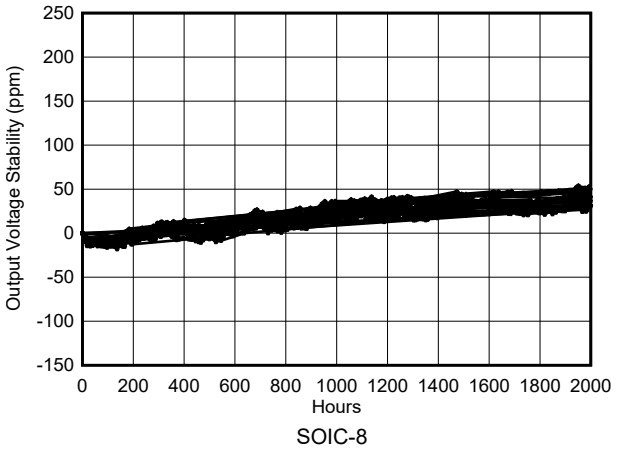


Figure 6-30. REF50xx Long-Term Stability (2000 Hours)

6.8 Typical Characteristics: REF50xxEI

at T_A = 25°C, V_{IN} = V_{EN} = V_{OUT} + 0.5V, I_L = 0mA, C_{Out} = 10µF, C_{NR} = Open, C_{IN} = 0.1µF,

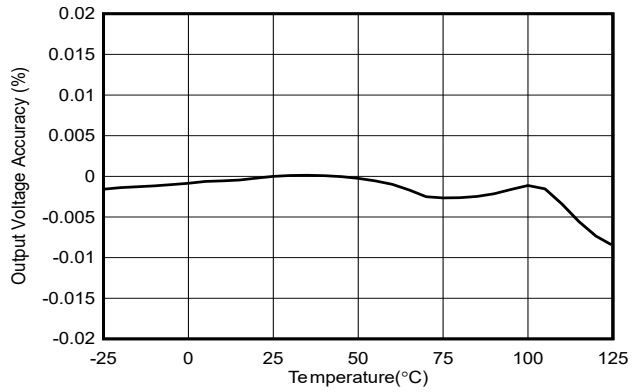


Figure 6-31. Output Voltage Vs Free-Air Temperature

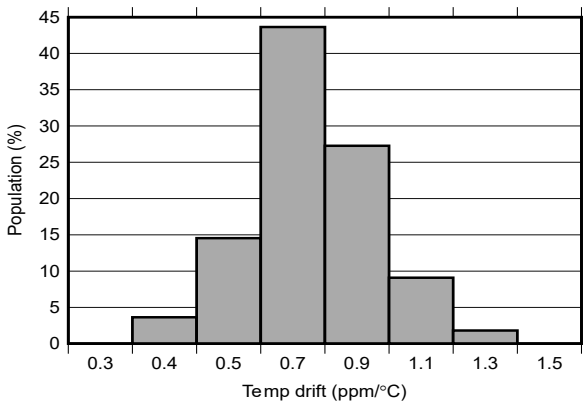


Figure 6-32. Temperature Drift Distribution

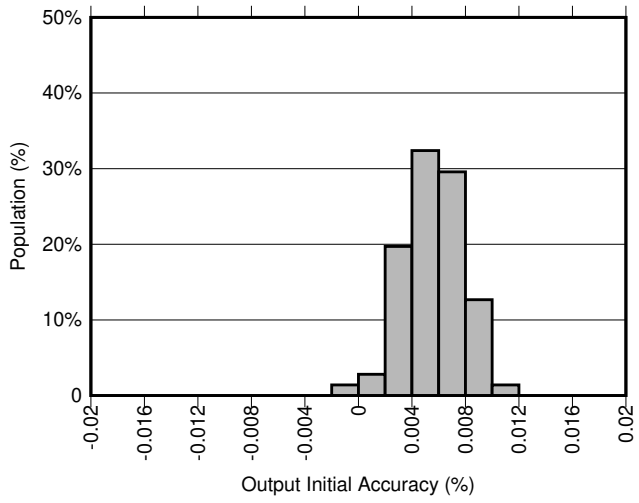


Figure 6-33. Accuracy Distribution

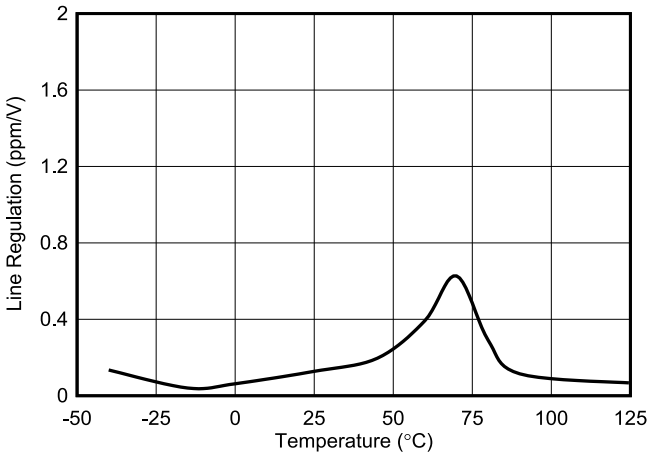


Figure 6-34. Line Regulation vs Temperature

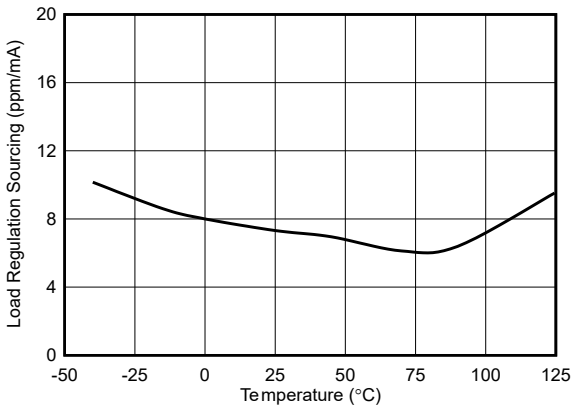


Figure 6-35. Load Regulation (Sourcing) vs Temperature

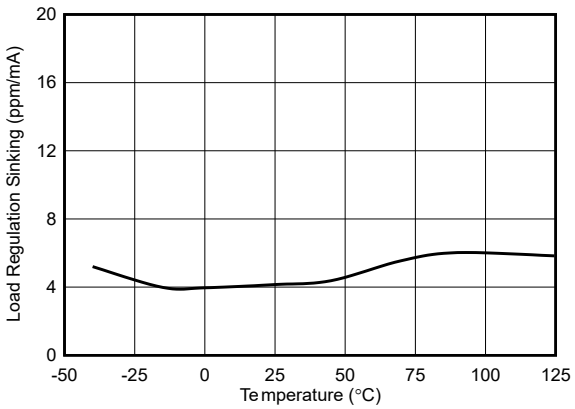


Figure 6-36. Load Regulation (Sinking) vs Temperature

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6.8 Typical Characteristics: REF50xxEI (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{OUT} + 0.5V, I_L = 0mA, C_{Out} = 10µF, C_{NR} = Open, C_{IN} = 0.1µF,

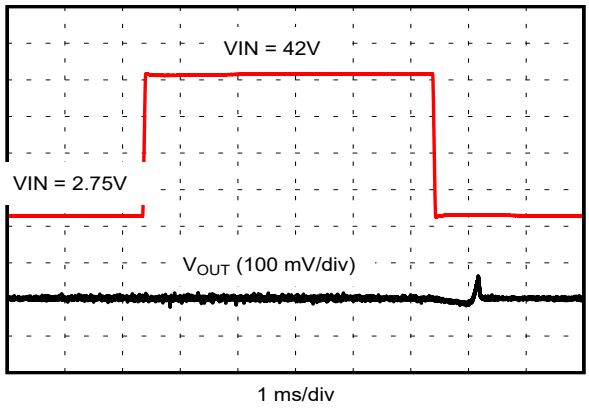


Figure 6-37. Line Transient Response

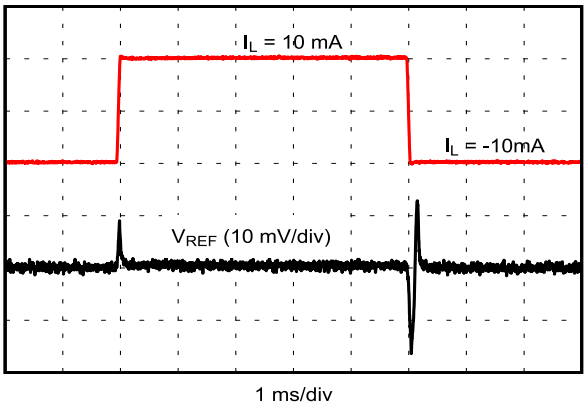


Figure 6-38. Load Transient Response (C_{OUT} = 10µF)

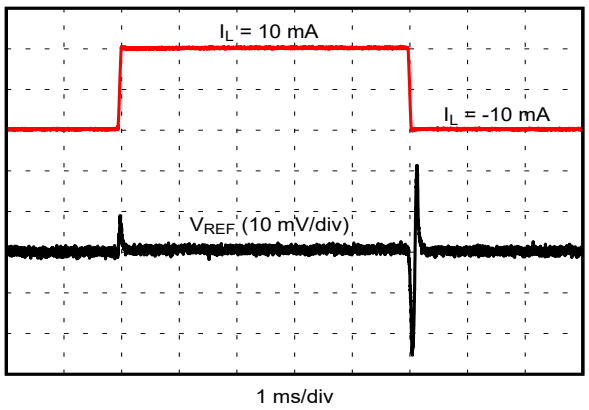


Figure 6-39. Load Transient Response (C_{OUT} = 1µF)

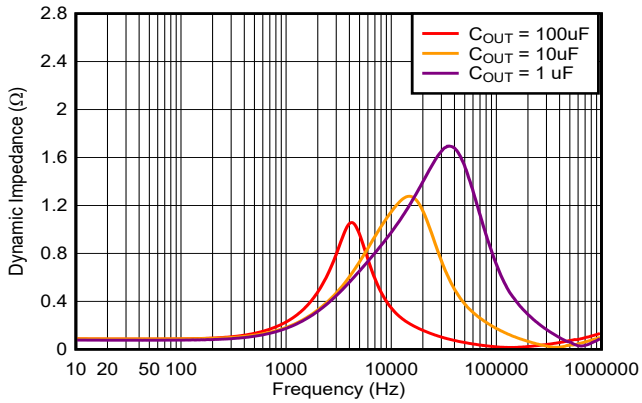


Figure 6-40. Output Impedance

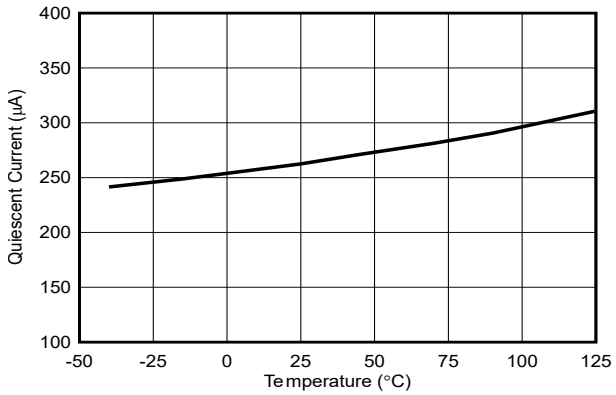


Figure 6-41. Quiescent Current vs Temperature

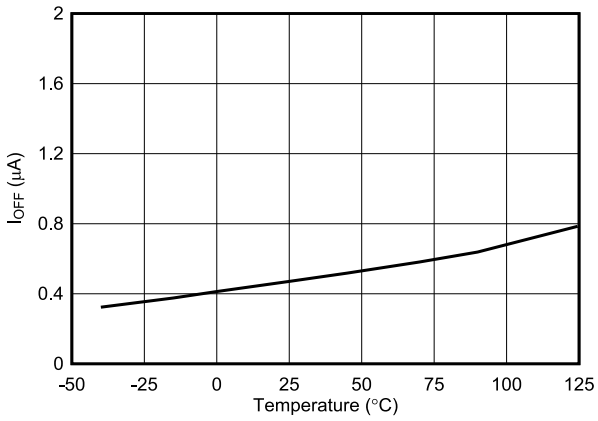


Figure 6-42. Shutdown Current vs Temperature

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6.8 Typical Characteristics: REF50xxEI (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{OUT} + 0.5V, I_L = 0mA, C_{Out} = 10µF, C_{NR} = Open, C_{IN} = 0.1µF,

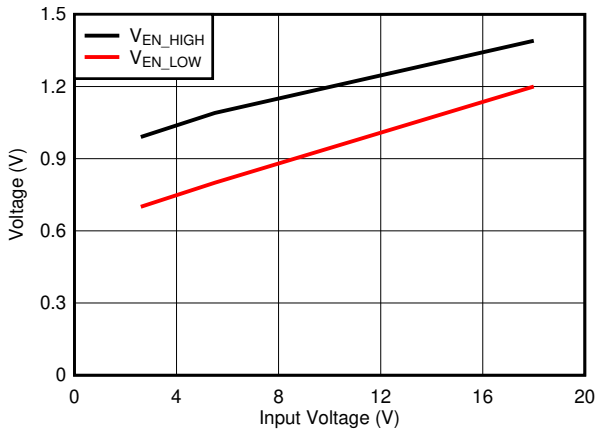


Figure 6-43. Enable Threshold vs V_{IN}

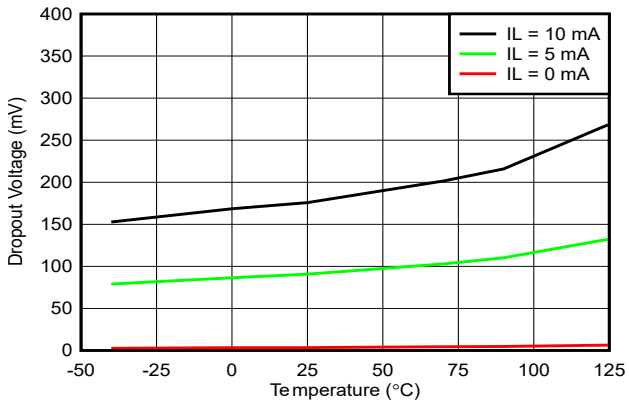


Figure 6-44. Dropout Voltage vs Temperature

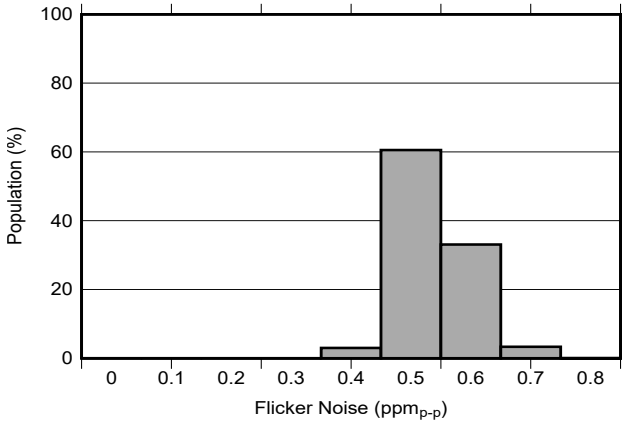


Figure 6-45. 0.1Hz to 10Hz Voltage Noise Distribution (C_{NR} = Open)

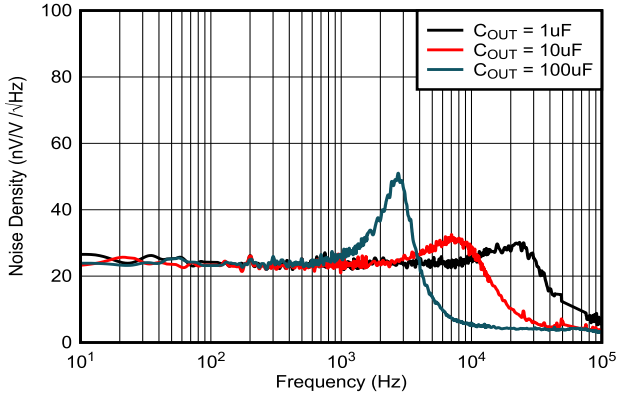


Figure 6-46. Noise Performance 10Hz to 100kHz (C_{NR} = Open)

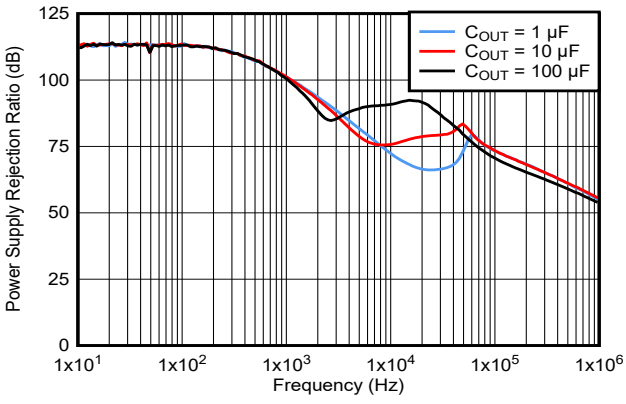


Figure 6-47. Power-Supply Rejection Ratio vs Frequency

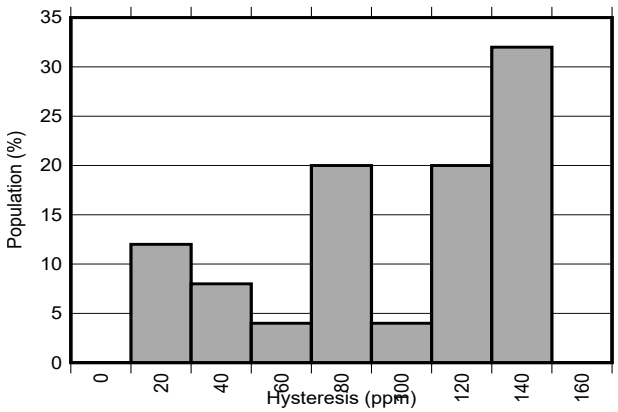


Figure 6-48. Thermal Hysteresis Distribution: Cycle 1 (-40°C to 125°C)

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6.8 Typical Characteristics: REF50xxEI (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{OUT} + 0.5V, I_L = 0mA, C_{Out} = 10µF, C_{NR} = Open, C_{IN} = 0.1µF,

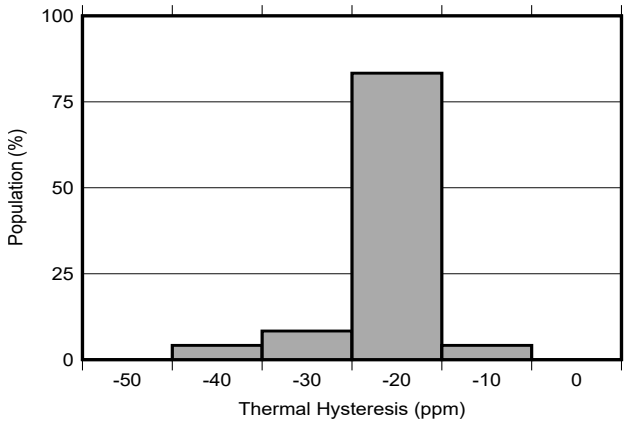


Figure 6-49. Thermal Hysteresis Distribution: Cycle 2 (-40°C to 125°C)

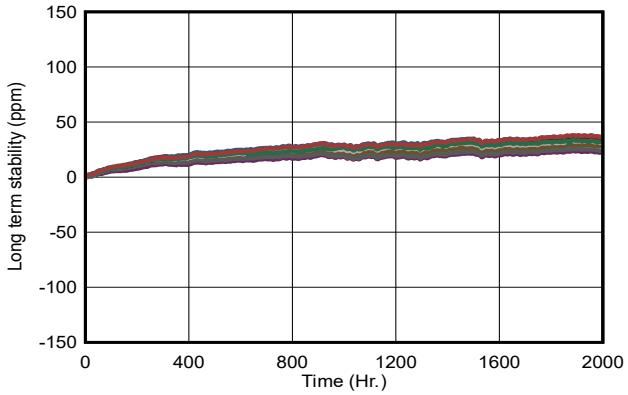


Figure 6-50. Long-Term Stability (First 2000 Hours)

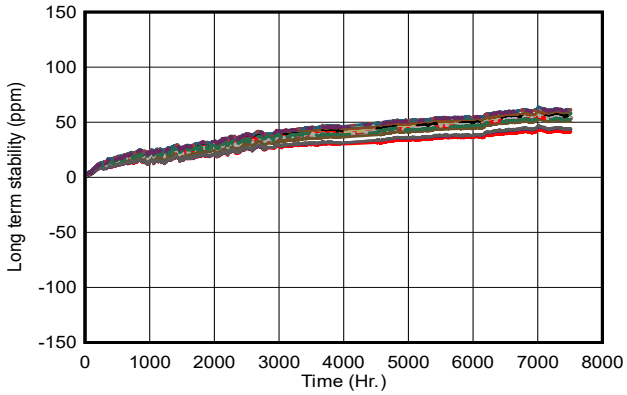


Figure 6-51. Long-Term Stability (7500 hours)

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7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in manufacturing the REF50xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device can cause the output voltages to shift, degrading the initial accuracy and drift specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, 36 devices are soldered on printed-circuit-boards using lead-free solder paste and the paste manufacturer suggested reflow profile. Figure 7-1 shows the reflow profile. The printed-circuit-board is comprised of FR4 material. The board thickness is 0.8mm and the area is 13mm × 13mm.

The reference voltage is measured before and after the reflow process across temperature; the typical shift of accuracy and drift is displayed in Figure 7-2 for REF50xxEI and Figure 7-3 through Figure 7-10 for REF50xx. Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed-circuit-board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on printed circuit boards (PCBs) with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, then solder the device in the last pass to minimize device exposure to thermal stress.

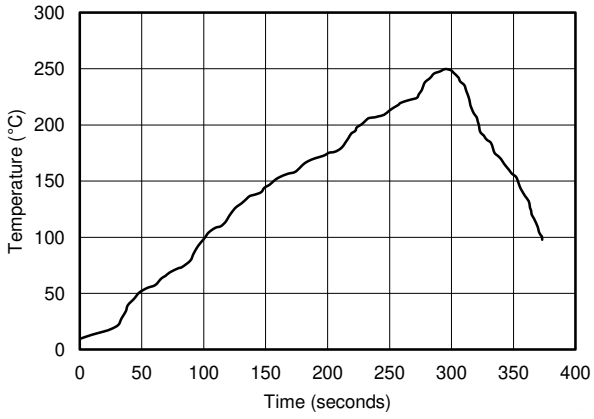


Figure 7-1. Reflow Profile

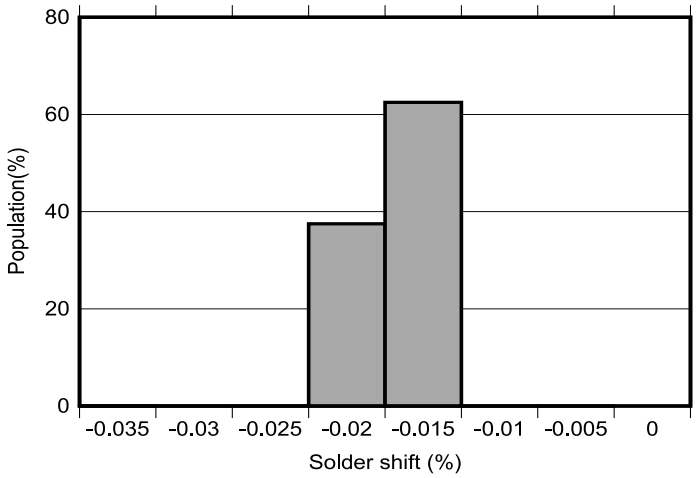


Figure 7-2. Solder Heat Shift Distribution (%), REF50xxEI

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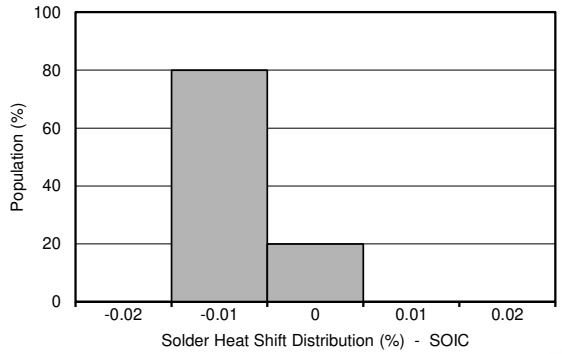


Figure 7-3. Solder Heat Shift Distribution (%), SOIC Package

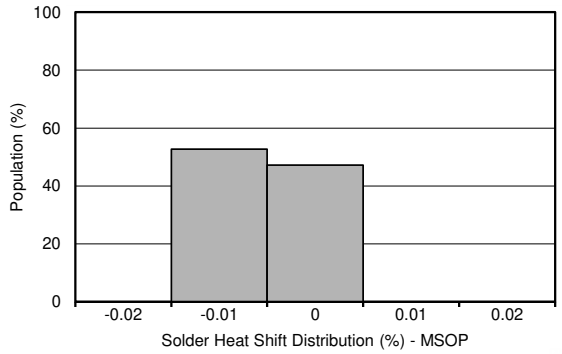


Figure 7-4. Solder Heat Shift Distribution (%), VSSOP Package

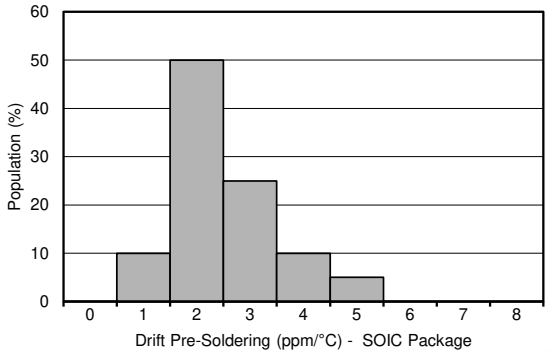


Figure 7-5. Drift Pre-Soldering Distribution, SOIC Package

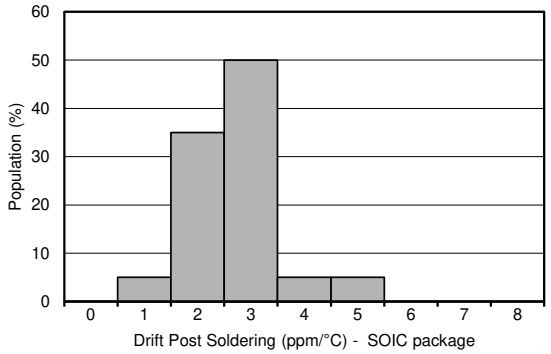


Figure 7-6. Drift Post Soldering Distribution, SOIC Package

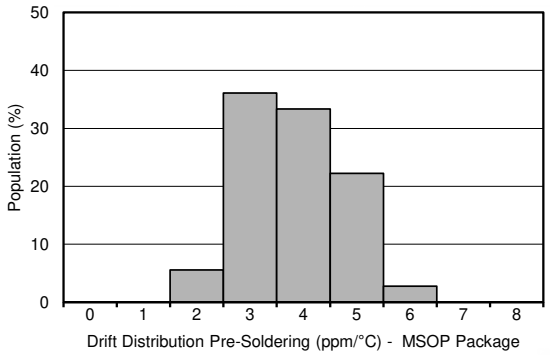


Figure 7-7. Drift Distribution Pre-Soldering, VSSOP Package

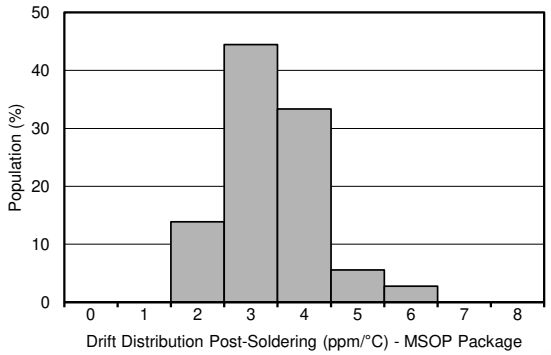


Figure 7-8. Drift Distribution Post-Soldering, VSSOP Package

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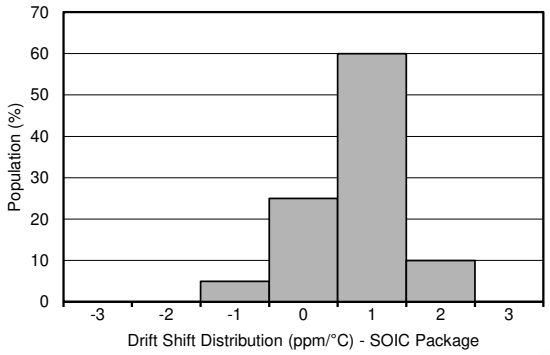


Figure 7-9. Drift Shift Distribution, SOIC Package

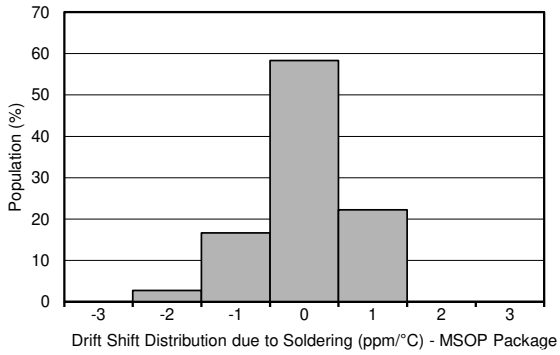


Figure 7-10. Drift Shift Distribution, VSSOP Package

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8 Detailed Description

8.1 Overview

The REF50xx is family of low-noise, precision band-gap voltage references designed for excellent initial voltage accuracy and drift. See Section 8.2 for a simplified block diagram of the REF50xx.

8.2 Functional Block Diagram

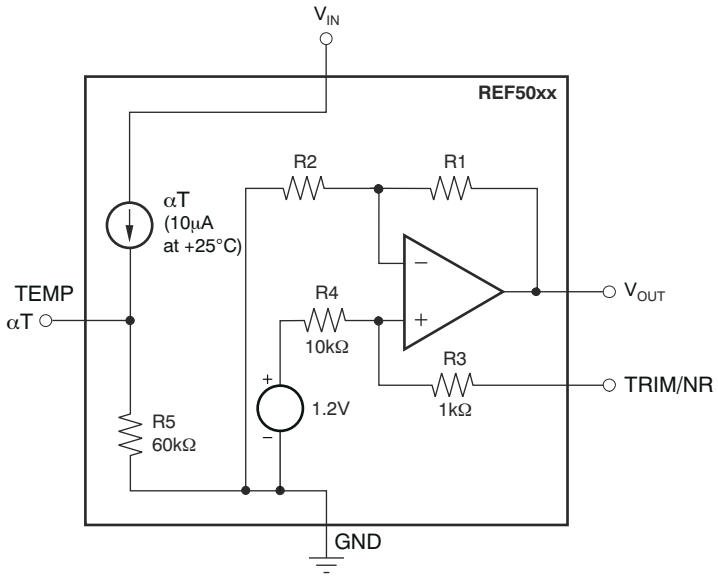


Figure 8-1. REF50xxI, REF50xxAI Block Diagram

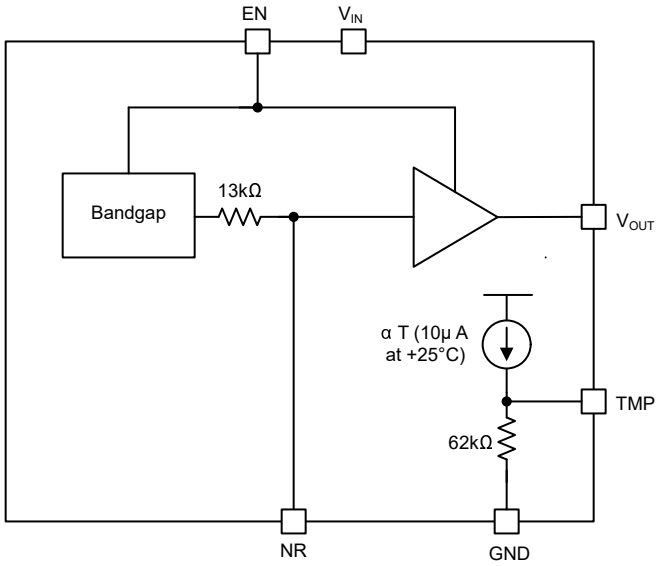


Figure 8-2. REF50xxEI Block Diagram

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8.3 Feature Description

8.3.1 Temperature Monitoring

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60kΩ source impedance. As illustrated in Figure 6-8, the output voltage follows the nominal relationship:

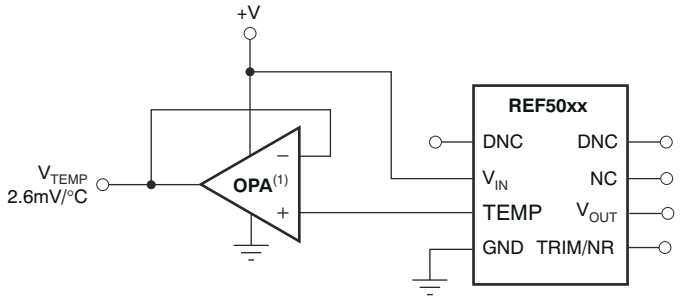
REF50xxI, REF50xxAI: $V_{TEMP\ PIN}$ = 509mV + 2.64 × T(°C) (1)

REF50xxEI: $V_{TEMP\ PIN}$ = 625mV + 2.64 × T(°C) (2)

The TEMP pin indicates general chip temperature, accurate to approximately ±15°C. Although not generally suitable for accurate temperature measurements, use the TEMP pin to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high-output impedance (see Section 8.2). Loading the TEMP pin with a low-impedance circuit induces a measurement error; however, the pin does not have any effect on V_{OUT} accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 8-3.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 8-3. Buffering the TEMP Pin Output

8.3.2 Temperature Drift

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as calculated in Equation 3.

$$\text{Drift} = \left[\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temperature Range}}\right] \times 10^6 (\text{ppm}) \quad (3)$$

The REF50xx features a maximum drift coefficient of 2.5ppm/°C for the enhanced-grade version, 3ppm/°C for the high-grade version, and 8ppm/°C for the standard-grade version.

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8.3.3 Thermal Hysteresis

Thermal hysteresis for the REF50xx is the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Equation 4 shows thermal hysteresis.

$$V_{HYST} = \left[\frac{|V_{PRE} - V_{POST}|}{V_{NOM}}\right] \times 10^6 (ppm) \quad (4)$$

where

- V_{HYST} = thermal hysteresis (ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measurement after the device cycles from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C

8.3.4 Noise Performance

Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified Section 6.5 and Section 6.6. The noise voltage increases with output voltage and operating temperature. Use additional filtering to improve output noise levels. If using additional filtering, verify that the output impedance does not degrade performance.

For additional information about minimizing noise and maximizing performance in mixed-signal applications, such as data converters, refer to the *How a Voltage Reference Affects ADC Performance Part 1*, *How a Voltage Reference Affects ADC Performance Part 2*, and *How a Voltage Reference Affects ADC Performance Part 3* analog design journals.

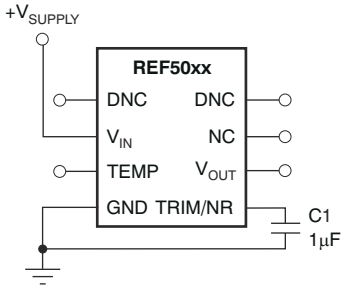


Figure 8-4. Noise Reduction Using the TRIM/NR Pin

8.3.5 Long-Term Stability

Due to aging and environmental effects, all semiconductor devices experience physical changes of the semiconductor die and the packaging material over time. Over time, the changes and the associated package stress on the die cause the output voltage in precision voltage references to deviate. The value of such change is specified in the data sheet by a parameter called the long-term stability (also known as the long-term drift (LTD)). Equation 5 shows how LTD is calculated. Note that the LTD value is positive if the output voltage drifts higher over time and negative if the voltage drifts lower over time. Figure 6-23 through Figure 6-30 show the drift of the output voltage for REF50xx over the first 4000 operating hours.

$$LTD(ppm)|_{t=n} = \frac{\left[V_{OUT}|_{t=0} - V_{OUT}|_{t=n}\right]}{V_{OUT}|_{t=0}} \times 10^6 \quad (5)$$

where

- $LTD(ppm)|_{t=n}$ = long-term stability (ppm)
- $V_{OUT}|_{t=0}$ = output voltage at time = 0 hr
- $V_{OUT}|_{t=n}$ = output voltage at time = n hr

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8.3.6 Output Adjustment Using the TRIM/NR Pin

The REF50xxI, REF50xxAI provides a very accurate, factory-trimmed voltage output. Adjust V_{OUT} using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 8-5 shows a typical circuit that allows an output adjustment of ±15mV.

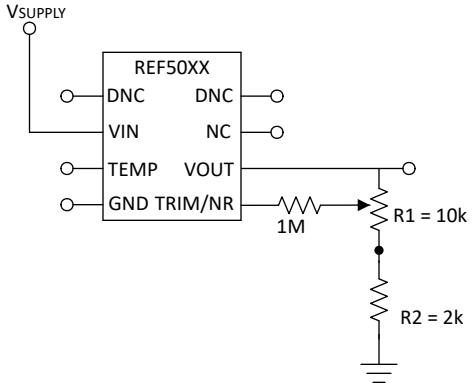


Figure 8-5. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the band-gap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (Figure 8-4) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1µF creates a low-pass filter with the corner frequency from 10Hz to 20Hz. A low-pass filter decreases the overall noise measured on the V_{OUT} pin by half. A higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Using this capacitor increases start-up time.

8.4 Device Functional Modes

8.4.1 Basic Connections

Figure 8-6 shows the typical connections for the REF50xx. TI recommends a supply bypass capacitor ranging from 1µF to 10µF. Confirm that a output capacitor (C_L) is connected from V_{OUT} to GND. For output stability, verify that the equivalent series resistance (ESR) value of C_L less than or equal to 1.5Ω. To minimize noise, the recommended ESR of C_L is from 1Ω and 1.5Ω.

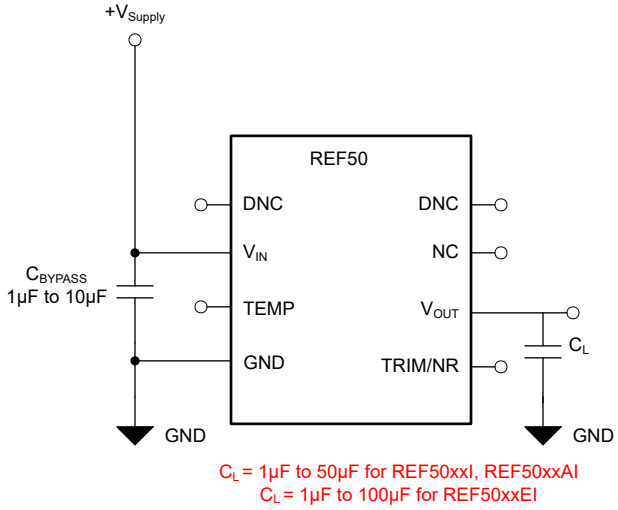


Figure 8-6. Basic Connections

8.4.2 Supply Voltage

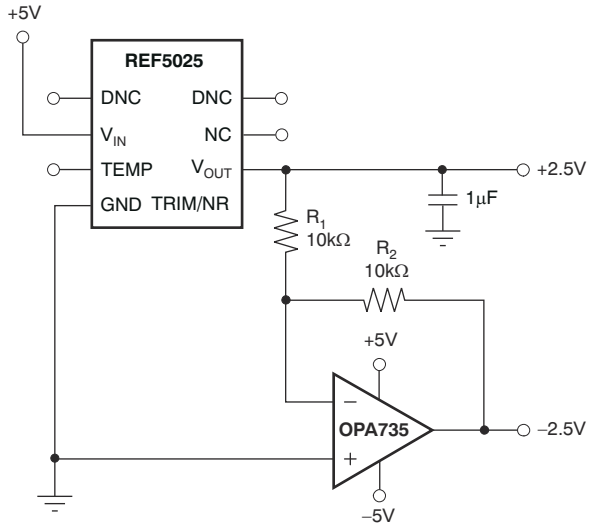
The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V, operate the family of references with a supply of

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200mV more than the output voltage in an unloaded condition. For loaded conditions, Figure 6-6 shows a typical dropout voltage versus load plot.

8.4.3 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, use REF50xx and OPA735 to provide a dual-supply reference from a 5V supply. Figure 8-7 shows the REF5025 used to provide a 2.5V supply reference voltage. The low-drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Verify that the temperature coefficients of R_1 and R_2 match.



NOTE: Bypass capacitors not shown.

Figure 8-7. REF5025 and OPA735 Create Positive and Negative Reference Voltages

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9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 9-1 shows the REF5040 in a basic data acquisition system.

9.2 Typical Applications

9.2.1 16-bit, 250KSPS Data Acquisition System

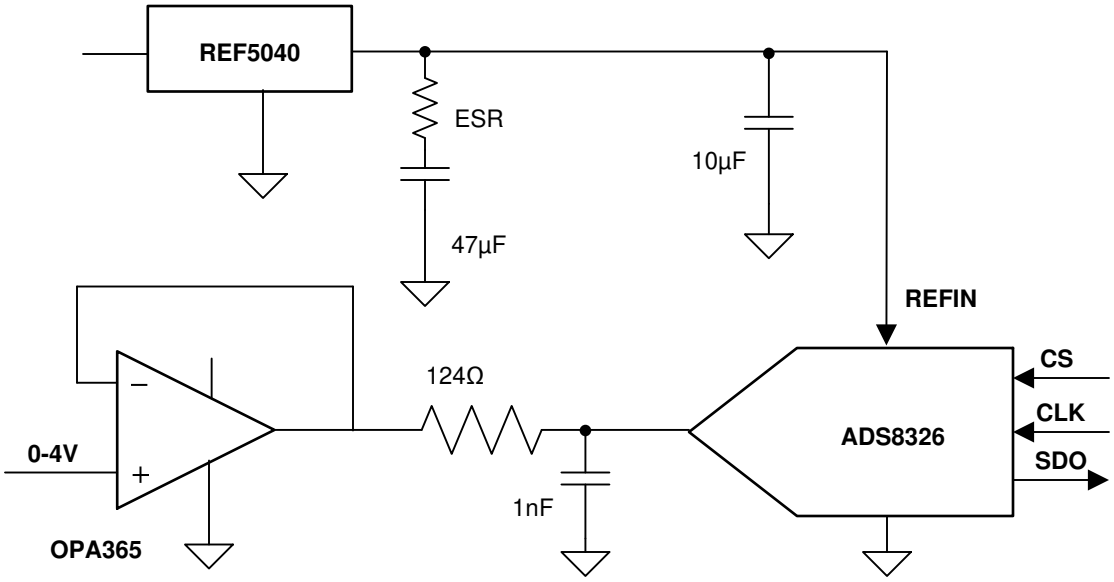


Figure 9-1. Complete Data Acquisition System Using the REF50xx

9.2.1.1 Design Requirements

When using the REF50xx in the design, select a proper output capacitor that does not create gain peaking, thereby increasing total system noise. At the same time, select a capacitor that provides the required filtering performance for the system. Add input bypass capacitor and noise reduction capacitors for peak performances. During the design of the data acquisition system, give equal consideration to the buffering analog input signal and the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement for good performance of the data acquisition system.

9.2.1.2 Detailed Design Procedure

The OPA365 is used to drive the 16-bit analog-to-digital converter (ADS8326). The RC filter at the output of the OPA365 is used to reduce the charge kick-back created by the opening and closing of the sampling switch inside the ADC. Design the RC filter such that the voltage at the sampling capacitor settles to 16-bit accuracy within the acquisition time of the ADC. Verify that the bandwidth of the driving amplifier is at least be four times the bandwidth of the RC filter.

The REF5040 is used to drive the REF pin of the ADS8326. Proper selection of voltage reference output capacitor is very important for this design. Very low equivalent series resistance (ESR) creates gain-peaking,

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which degrades SNR of the total system. If the ESR of the capacitor is not enough, then an additional resistor must be added in series with the output capacitor. A capacitance of 1µF can connect to the NR pin to reduce band-gap noise of the REF50xx.

Table 9-1 shows SNR measurements using different RC filters at the output of the OPA365, different values of output capacitor for the REF50xx and different values of capacitors at the TRIM/NR pin.

Table 9-1. Data Acquisition Measurement Results for Different Conditions

	TEST CONDITION 1	TEST CONDITION 2
OPA365 RC filter	124Ω, 1nF	124Ω, 1nF
REF5040 output capacitor	10µF	10µF + 47µF
TRIM/NR pin capacitor	0µF	1µF
SNR	86.7dB	92.8dB

9.2.1.3 Application Curve

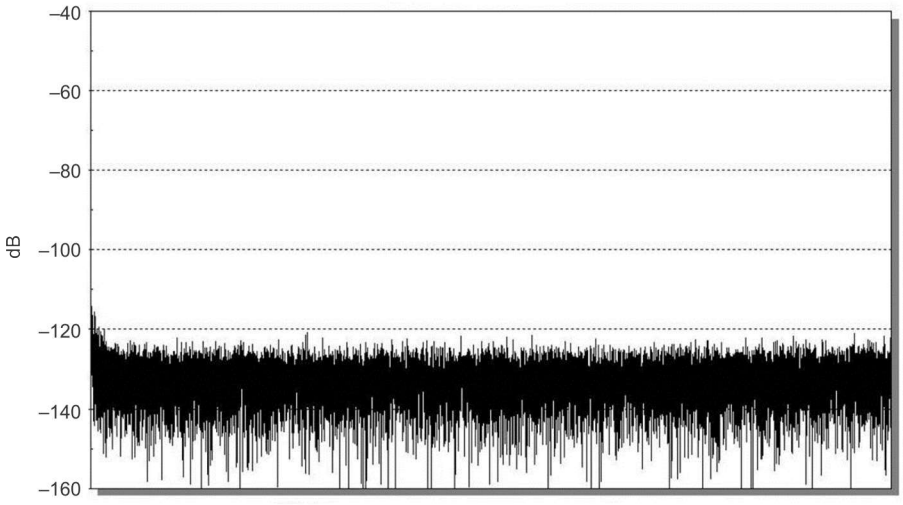


Figure 9-2. FFT Plot-Noise Floor of Data Acquisition System

9.3 Power Supply Recommendations

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V, the REF50xx family of voltage references operates with a supply of 200mV more than the output voltage in an unloaded condition. For loaded conditions, Figure 6-6 provides a typical dropout voltage versus load plot. TI recommends a supply bypass capacitor ranging from 1µF to 50µF for REF50xxI and REF50xxAI. TI recommends a supply bypass capacitor ranging from 1µF to 100µF for REF50xxEI.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 REF50xxI, REF50xxAI Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 1µF to 10µF. If necessary, add decoupling capacitance to compensate for noisy or high-impedance power supplies.
- Place a 1µF noise filtering capacitor between the NR pin and ground.
- Verify that the output decouples with a 1µF to 50µF capacitor. A resistor in series with the output capacitor is optional. For better noise performance, the recommended ESR on the output capacitor is from 1Ω to 1.5Ω.

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- Add a high-frequency, 1µF capacitor in parallel between the output and ground to filter noise and help with switching loads as data converters.

9.4.1.2 REF50xxEI Layout Guidelines

- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 0.1µF to 10µF. If necessary, add decoupling capacitance to compensate for noisy or high-impedance power supplies. Verify that the smallest capacitor is placed closest to the device.
- Place a 0.1µF to 1µF class 1 noise filtering capacitor between the NR pin and ground.
- Verify that the output decouples with a 1µF to 100µF low ESR (maximum 1Ω) capacitor.

9.4.2 Layout Example

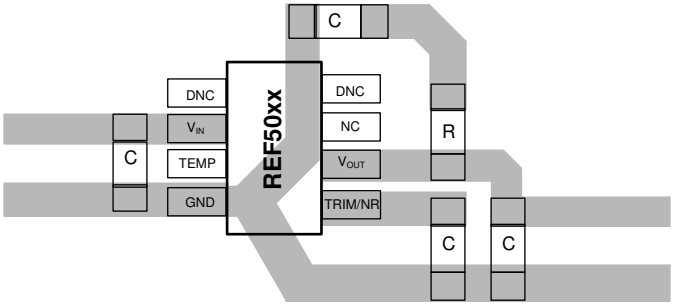


Figure 9-3. Layout Example for REF50xxI, REF50xxAI

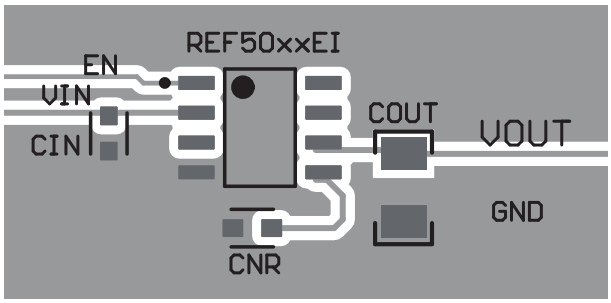


Figure 9-4. Layout Example for REF50xxEI

9.4.3 Power Dissipation

The REF50xx family is specified to deliver current loads of ±10mA over the specified input voltage range. The temperature of the device increases according to Equation 6:

$$T_J = T_A + P_D \times \theta_{JA} \quad (6)$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- P_D = power dissipated (W)
- θ_{JA} = junction-to-ambient thermal resistance (°C/W)

Establish that the REF50xx junction temperature does not exceed the absolute maximum rating of 150°C.

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *0.05µV/°C (Maximum), Single-Supply CMOS Zero-Drift Series Operational Amplifier* data sheet
- Texas Instruments, *REF5020 PSpice Model*
- Texas Instruments, *REF5020 TINA-TI Reference Design*
- Texas Instruments, *REF5020 TINA-TI Spice Model*
- Texas Instruments, *INA270 PSpice Model*
- Texas Instruments, *INA270 TINA-TI Reference Design*
- Texas Instruments, *INA270 TINA-TI Spice Model*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (March 2025) to Revision O (October 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Deleted paragraph describing REF50xxEI voltage range	1
• Updated Table 4-1 REF50xxE information	3
• Deleted Product Preview tag from REF5030EID, REF5040EID, and REF5045EID devices	3
• Added Table 4-2	3
• Updated pin information from: REF50xxA to: REF50xxAI	4
• Updated pin information from: REF50xxE to: REF50xxEI	4
• Updated title from: Electrical Characteristics REF50 to: Electrical Characteristics REF50xxA and REF50xxAI	7
• Changed from: Layout Guidelines to: REF50xxEI Layout Guidelines and REF50xxI, REF50xxAI Layout Guidelines	30

Changes from Revision M (December 2024) to Revision N (March 2025)	Page
• Update datasheet header folder link from REF50XX to REF50 and REF50E	1

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5010AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010
REF5010ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010
REF5010IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5020AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5020AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A
REF5020AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A
REF5020AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A
REF5020ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5020ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5020IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5020IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5025AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5025AIDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AIDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AIDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025EIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5025E
REF5025EIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5025E
REF5025ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5025ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5025IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5025IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5030AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5030AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030EIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5030E
REF5030ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5030ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5030IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5030IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5040AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5040AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKTG4.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040EIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5040E
REF5040ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040
REF5040ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040
REF5040IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040
REF5040IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5045AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5045ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5045IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5045IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5050AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50F

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5050AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050EIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5050E
REF5050EIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5050E
REF5050ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050
REF5050ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050
REF5050IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050
REF5050IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

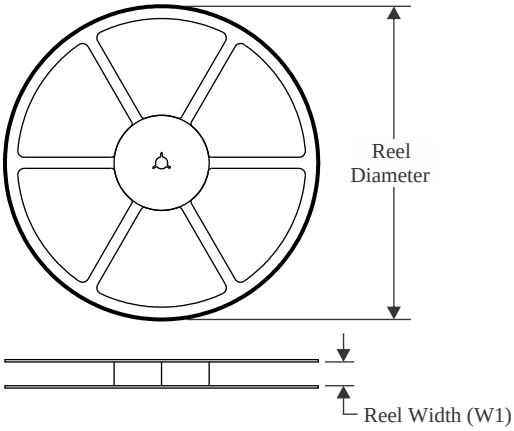
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

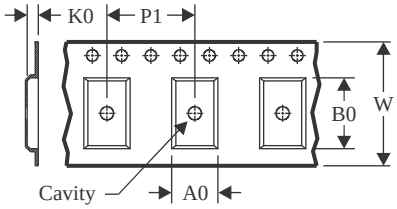
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

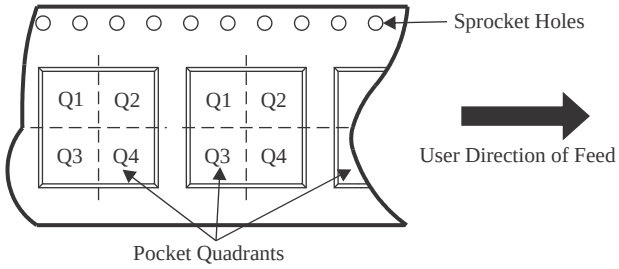


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

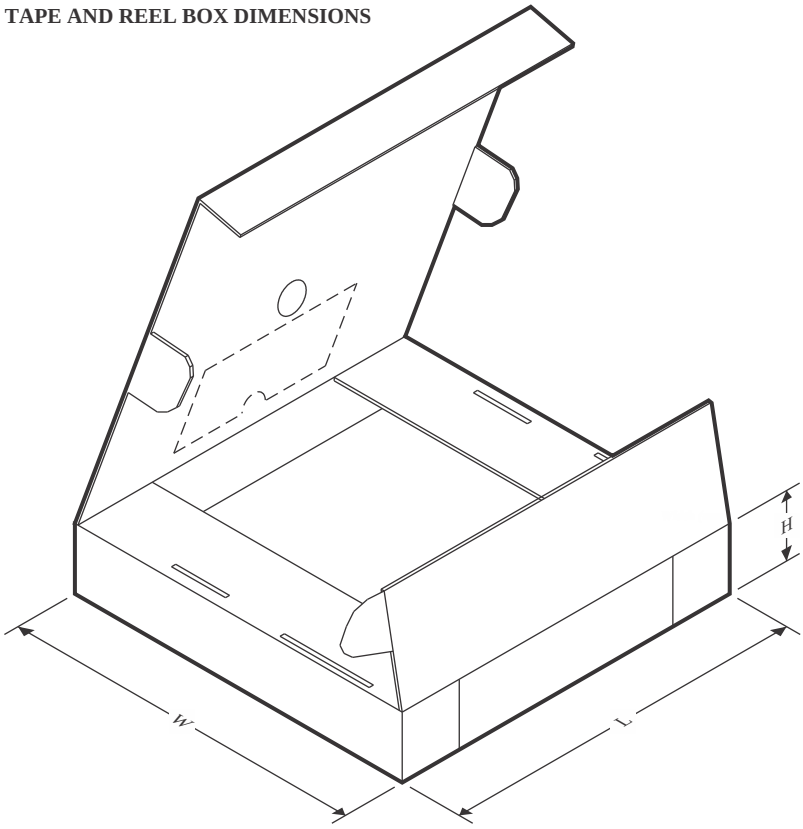


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5025AIDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKTG4	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

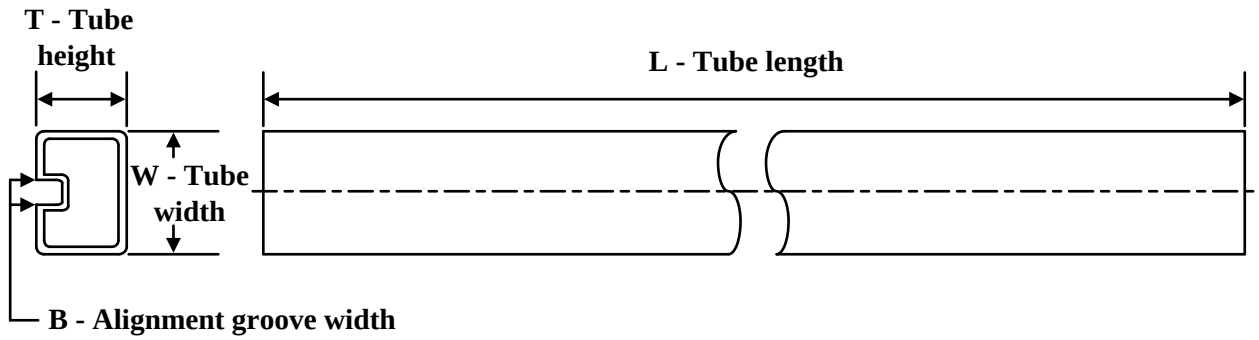


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5010AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5010AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5010AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
REF5010IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5010IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5020AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5020AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5020AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5020IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5020IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5020IDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5025AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5025AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5025AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5025AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5025AIDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
REF5025EIDR	SOIC	D	8	3000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5025IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5025IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5025IDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5030AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5030AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5030AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5030AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5030AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
REF5030EIDR	SOIC	D	8	3000	353.0	353.0	32.0
REF5030IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5030IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5030IDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5040AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5040AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5040AIDGKTG4	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5040AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5040AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
REF5040EIDR	SOIC	D	8	3000	353.0	353.0	32.0
REF5040IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5040IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5040IDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5045AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5045AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5045AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5045IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5045IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5045IDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5050AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5050AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5050AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5050AIDR	SOIC	D	8	2500	353.0	353.0	32.0
REF5050EIDR	SOIC	D	8	3000	353.0	353.0	32.0
REF5050IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
REF5050IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
REF5050IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

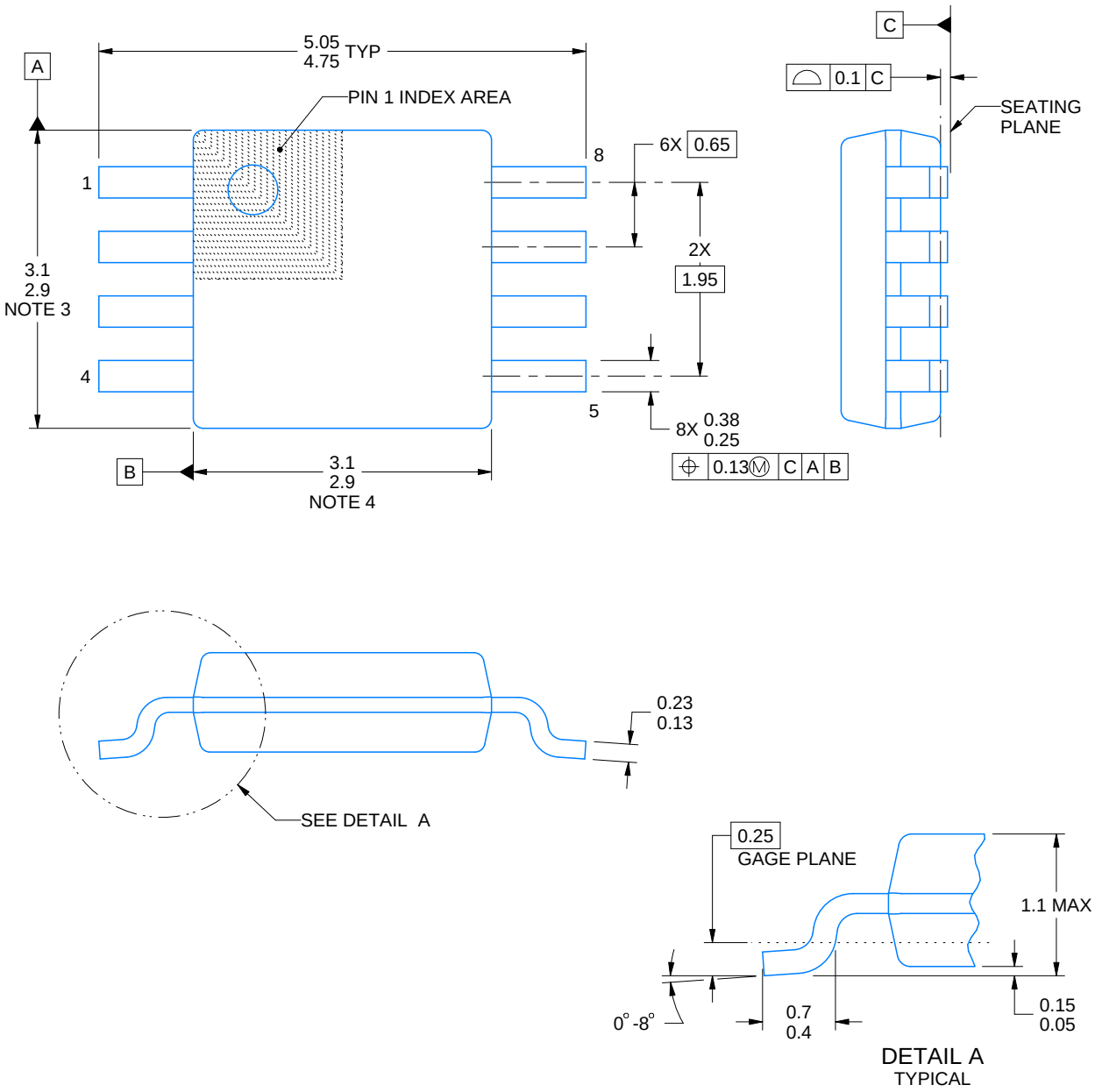
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
REF5010AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5010AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5010ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5010ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5020AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5020AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5020ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5020ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5025AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5025AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5025ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5025ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5030AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5030AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5030ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5030ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5040AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5040AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5040ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5040ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5045AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5045AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5045ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5045ID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5050AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5050AID.A	D	SOIC	8	75	506.6	8	3940	4.32
REF5050ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5050ID.A	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

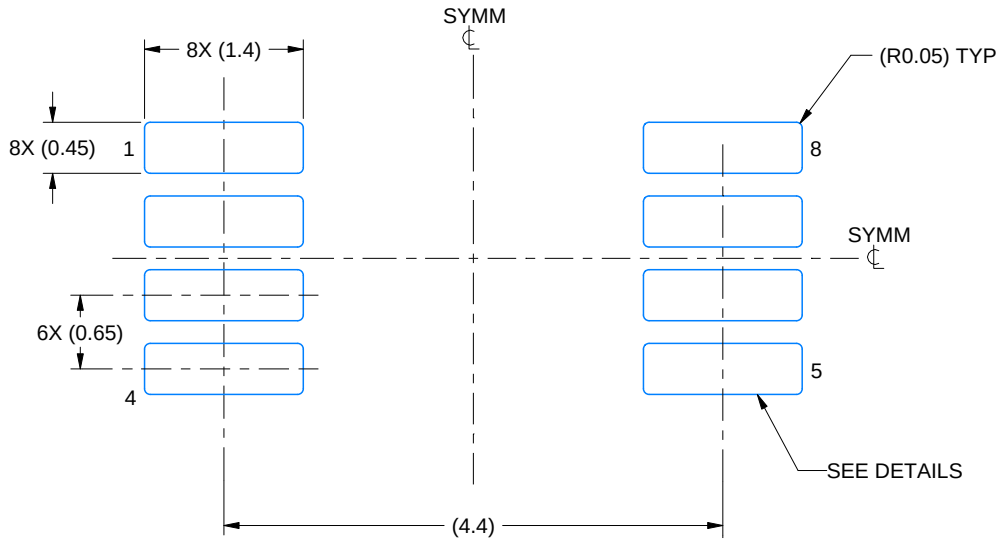
SMALL OUTLINE PACKAGE



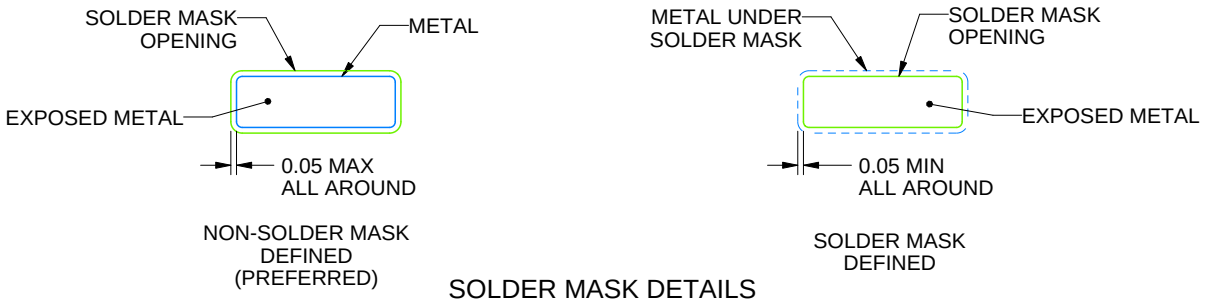
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

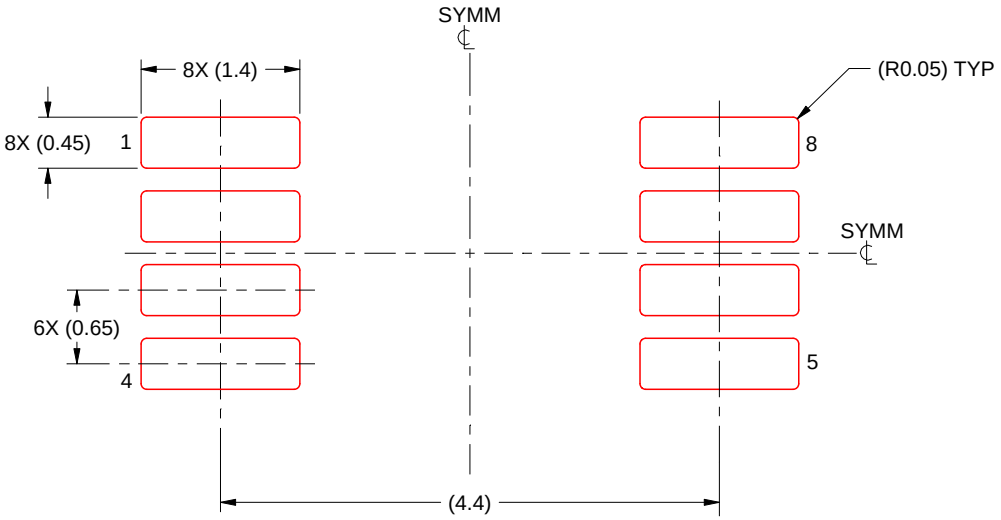


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

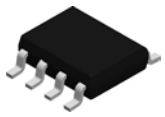


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

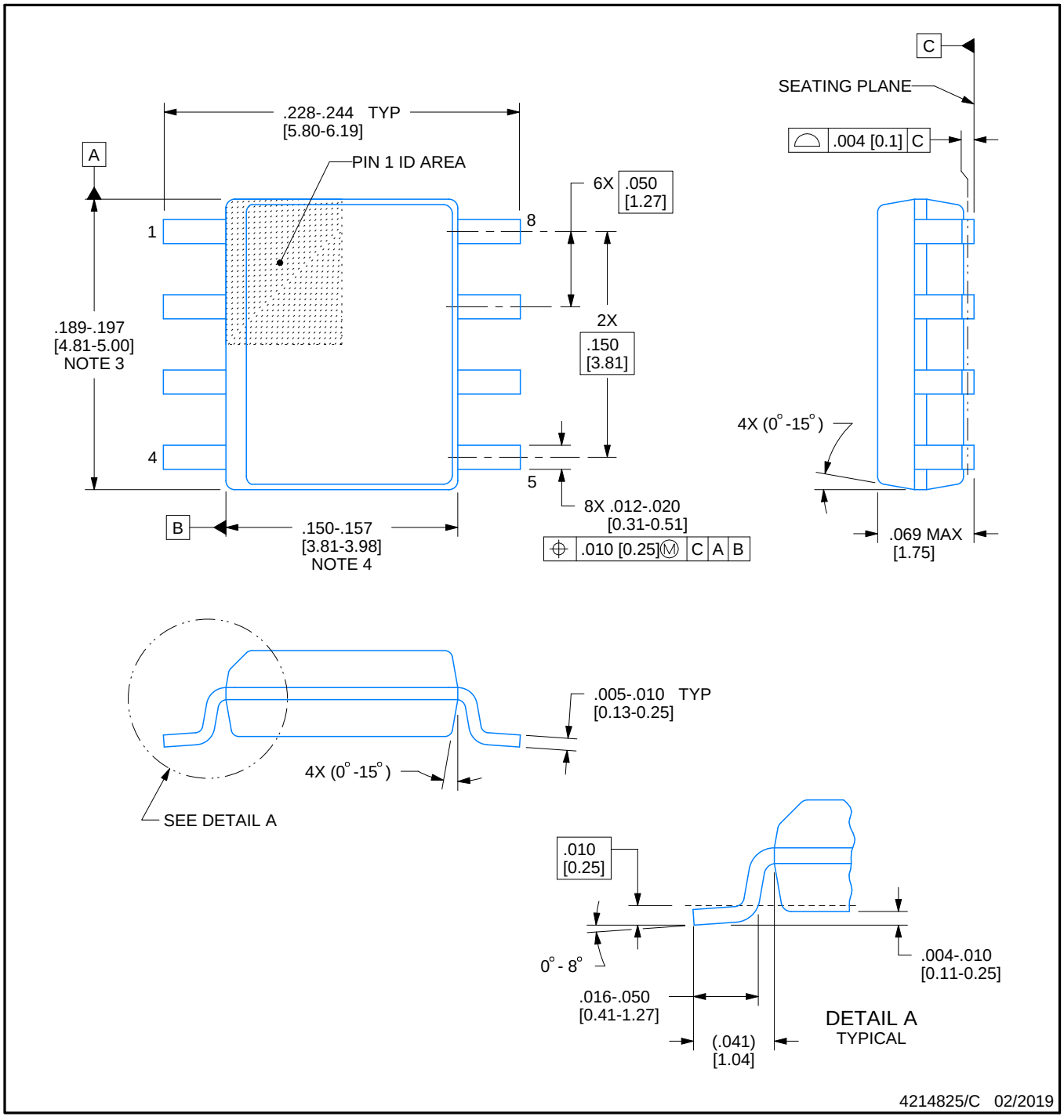


PACKAGE OUTLINE

D0008A

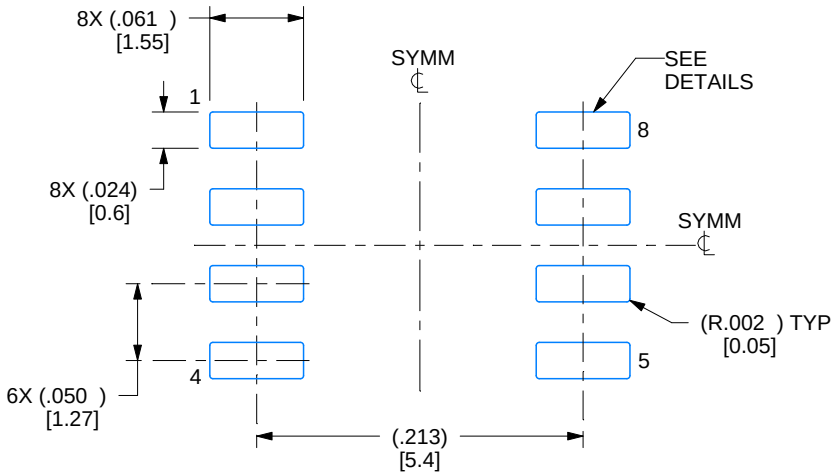
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

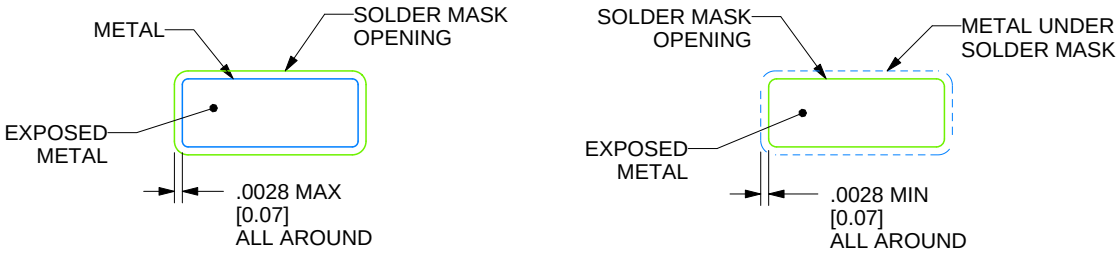


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

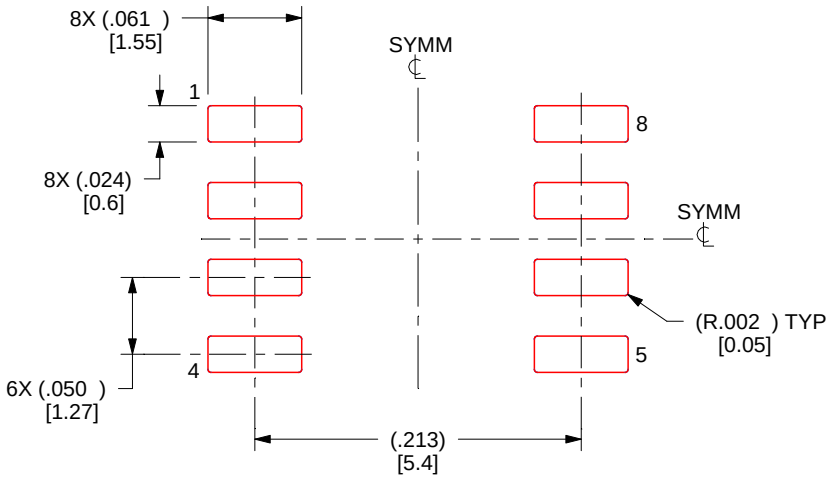
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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