UA78L 系列正电压线性稳压器

1 特性

- 输入电压范围 (V_I)：4.75 V 至 35 V
- 输出电压范围 (V_O)：
  - 2.6V 至 15V（适用于旧芯片）
  - 3.3V 至 15V（适用于新芯片）
- 输出电流：高达 100 mA
- 静态电流 I_Q：3.8 mA
- 内置短路电流限制和热保护
- 无需任何外部元件即可保持稳定
- 支持的温度范围：
  - 旧芯片 C 和 AC 版本：0°C 至 +125°C
  - 旧芯片 AI 版本：–40°C 至 +125°C
  - 新芯片：–40°C 至 +125°C
- 封装：
  - 8 引脚，4.9mm x 3.91mm SOIC
  - 3 引脚，4.3mm x 4.3mm TO-92
  - 3 引脚，4.5mm x 2.5mm SOT-89

2 应用

- 电机驱动器
- 电器
- 楼宇自动化
- 流量变送器
- 工厂自动化和控制

3 说明

UA78L 系列固定电压线性稳压器适用于各种应用。UA78L 系列可用于板级稳压，从而消除与单点稳压相关的噪声和分布问题。UA78L 也可与功率导通元件配合使用，用作高电流电压稳压器。UA78L 系列稳压器可提供高达 100mA 的输出电流。此外，UA78L 无需外部电容器即可在整个负载电流范围内稳定运行。这类稳压器的内部电流限制和热关断功能可避免器件发生过载。

对于旧芯片，UA78L00C 和 UA78L00AC 系列的额定结温范围为 0°C 至 +125°C，UA78L05AI 器件的额定工作结温范围为 -40°C 至 +125°C。

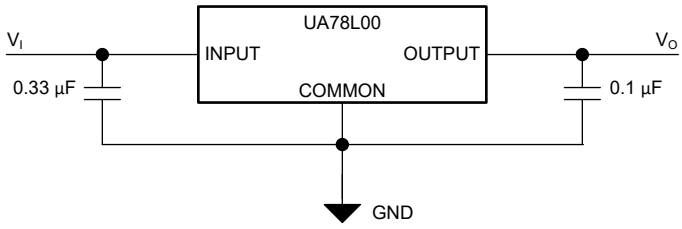
对于新芯片，UA78L 系列的额定结温范围为 -40°C 至 +125°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
UA78L	D（SOIC，8）	4.9 mm × 6 mm
	LP（TO-92，3）	5.2 mm x 3.68 mm
	PK（SOT-89，3）	4.5 mm × 4.095 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision W (April 2023) to Revision X (June 2023) **Page**

- 将 M3 器件状态从*预告信息*更改为*量产数据* ... 1

Changes from Revision V (November 2016) to Revision W (April 2023) **Page**

- 向文档添加了 M3 器件 ... 1
- 更改了*特性*、*应用*和*说明*部分 ... 1
- Changed *Description* column of *Pin Functions* table ... 3
- Added plots for new chip, reordered plots for legacy chip, and changed condition statement in *Typical Characteristics* section ... 13
- Changed *Overview* section ... 17
- Changed *Feature Description* section and added subsections ... 17
- Changed *Device Functional Modes* section: added *Device Functional Mode Comparison* table, deleted *Fixed-Output Mode* subsection, and added *Normal Operation* and *Dropout Operation* subsections ... 19
- Changed *Detailed Design Procedure* section and added subsections ... 20
- Added plots for new chip and changed condition statement in *Application Curves* section ... 24
- Added *Device Nomenclature* and *Evaluation Module* sections ... 27

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5 Pin Configuration and Functions

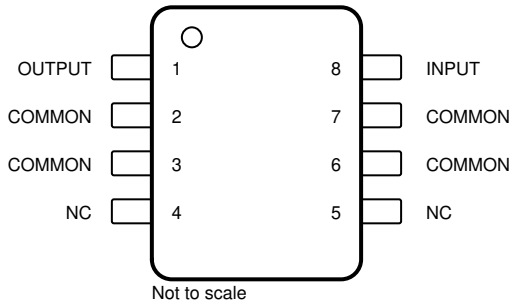


图 5-1. D Package, 8-Pin SOIC (Top View)

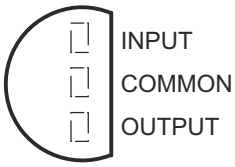


图 5-2. LP Package, 3-Pin TO-92 (Top View)

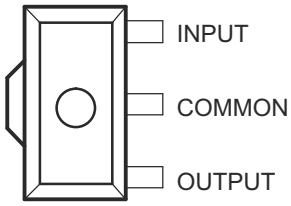


图 5-3. PK Package, 3-Pin SOT-89 (Top View)

PIN				TYPE	DESCRIPTION
NAME	SOIC	TO-92	SOT-89		
COMMON	2, 3, 6, 7	2	2	—	Ground
INPUT	8	3	3	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUTPUT	1	1	1	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
NC	4, 5	—	—	—	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_I (for legacy chip)	UA78L02AC, UA78L05C, UA78L09C, and UA78L10AC		30	V
	UA78L12C, UA78L12AC, UA78L15C, and UA78L15AC		35	
Input voltage, V_I (for new chip)	UA78L33AI, UA78L05AC, UA78L05AI, UA78L05C, UA78L12AC and UA78L15AC		45	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	TYP	MAX	UNIT
V_I	Input voltage	UA78L02AC (for legacy chip only)	4.75		20	V
		UA78L033AC (for new chip only)	4.75		20	
		UA78L05C and UA78L05AC (for both legacy and new chip)	7		20	
		UA78L06C and UA78L06AC (for legacy chip only)	8.5		20	
		UA78L08C and UA78L08AC (for legacy chip only)	10.5		23	
		UA78L09C and UA78L09AC (for legacy chip only)	11.5		24	
		UA78L10AC (for legacy chip only)	12.5		25	
		UA78L12C and UA78L12AC (for both legacy and new chip)	14.5		27	
		UA78L15C and UA78L15AC (for both legacy and new chip)	17.5		30	
I_O	Output current				100	mA
C_{IN} (2)	Input capacitor (3)			0.33		μF
C_{OUT} (2)	Output capacitor (4)			0.1		
T_J	Operating junction temperature	UA78L00C and UA78L00AC series (for legacy chip)	0		125	°C
		UA78L05AI (for legacy chip)	–40		125	
		UA78L00C , UA78L00AC, and UA78L05AI series (for new chip)	–40		125	

(1) All voltages are with respect to GND.
(2) UA78L regulator doesn't need any external capacitors for the the LDO stability.
(3) An input capacitor with value of 0.33 μF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.

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(4) An output capacitor with value of 0.1 μF is recommended to improve the load and line transient performance of the UA78L regulator.

6.4 Thermal Information

THERMAL METRIC[1]		UA78L00			UNIT
		D (SOIC)	LP (TO-92)	PK (SOT-89)	
		8 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	143.6	54.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	74.4	88.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	—	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.2	24.2	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	120.9	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: UA78L02 (Legacy Chip Only)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS[2]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 4.75 V to 20 V, and I_O = 1 mA to 40 mA	T_J = 25°C	2.5	2.6	2.7	V
		T_J = 0°C to 125°C	2.45		2.75	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		2.45		2.75	
Input voltage regulation	V_I = 4.75 V to 20 V, and T_J = 25°C			20	100	mV
	V_I = 5 V to 20 V, and T_J = 25°C			16	75	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz, and T_J = 25°C		43	51		dB
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C			12	50	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C			6	25	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C			30		μV
Dropout voltage	T_J = 25°C			1.7		V
Bias current	T_J = 25°C			3.6	6	mA
	T_J = 125°C				5.5	
Bias current change	V_I = 5 V to 20 V, and T_J = 0°C to 125°C				2.5	mA
	I_O = 1 mA to 40 mA, and T_J = 0°C to 125°C				0.1	

(1) Applies to UA78L02AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L02AC is T_J = 0°C to 125°C.

6.6 Electrical Characteristics: UA78L033 (New Chip Only)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 40 mA (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS [2]	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.5 V to 20 V, and I_O = 1 mA to 40 mA, T_J = 25°C	3.26	3.3	3.44	V
	V_I = 5.5 V to 20 V, and I_O = 1 mA to 40 mA, T_J = -40°C to 125°C	3.21		3.47	
	I_O = 1 mA to 70 mA, T_J = -40°C to 125°C	3.23		3.45	
Input voltage regulation	V_I = 5.5 V to 20 V, and T_J = 25°C		15	25	mV
	V_I = 6 V to 20 V, and T_J = 25°C		14	27	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz, and T_J = 25°C	49	57.5		dB
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C		13.5	28	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C		4.25	13	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C		85		μV

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6.6 Electrical Characteristics: UA78L033 (New Chip Only) (continued)

at specified junction temperature, V_I = 9 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
Dropout voltage	T_J = 25°C		1.7		V
Bias current	T_J = 25°C		3.53	4.1	mA
	T_J = 125°C			4.1	
Bias current change	V_I = 6 V to 20 V, and T_J = -40°C to 125°C			0.675	mA
	I_O = 1 mA to 40 mA, and T_J = -40°C to 125°C			0.01	

(1) Applies to UA78L033
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip)

at specified junction temperature, V_I = 10 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 7 V to 20 V, and I_O = 1 mA to 40 mA (for legacy chip)	T_J = 25°C	UA78L05C	4.6	5	5.4	V
			UA78L05AC and UA78L05AI	4.8	5	5.2	
		T_J = full range	UA78L05C	4.5		5.5	
			UA78L05AC and UA78L05AI	4.75		5.25	
	I_O = 1 mA to 70 mA, and T_J = full range (for legacy chip)	UA78L05C		4.5		5.5	
		UA78L05AC and UA78L05AI		4.75		5.25	
	V_I = 7 V to 20 V, and I_O = 1 mA to 40 mA (for new chip)	T_J = 25°C	UA78L05C	4.95	5	5.15	
			UA78L05AC and UA78L05AI	4.95	5	5.15	
		T_J = full range	UA78L05C	4.85		5.15	
			UA78L05AC and UA78L05AI	4.85		5.15	
	I_O = 1 mA to 70 mA, and T_J = full range (for new chip)	UA78L05C		4.80		5.14	
		UA78L05AC and UA78L05AI		4.80		5.14	
Input voltage regulation	V_I = 7 V to 20 V, and T_J = 25°C (for legacy chip)	UA78L05C			32	200	mV
		UA78L05AC and UA78L05AI			32	150	
	V_I = 8 V to 20 V, and T_J = 25°C (for legacy chip)	UA78L05C			26	150	
		UA78L05AC and UA78L05AI			26	100	
	V_I = 7 V to 20 V, and T_J = 25°C (for new chip)	UA78L05C			32	33	
		UA78L05AC and UA78L05AI			32	33	
	V_I = 8 V to 20 V, and T_J = 25°C (for new chip)	UA78L05C			26	28	
		UA78L05AC and UA78L05AI			26	28	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz, and T_J = 25°C (for legacy chip)	UA78L05C		40	49		dB
		UA78L05AC and UA78L05AI		41	49		
	V_I = 8 V to 18 V, f = 120 Hz, and T_J = 25°C (for new chip)	UA78L05C		48	55		
		UA78L05AC and UA78L05AI		48	55		
Output voltage regulation	for legacy chip	I_O = 1 mA to 100 mA, and T_J = 25°C			15	60	mV
		I_O = 1 mA to 40 mA, and T_J = 25°C			8	30	
	for new chip	I_O = 1 mA to 100 mA, and T_J = 25°C			15	35	
		I_O = 1 mA to 40 mA, and T_J = 25°C			8	15	
Output noise voltage	for legacy chip	f = 10 Hz to 100 kHz, and T_J = 25°C			42		µV
	for new chip	f = 10 Hz to 100 kHz, and T_J = 25°C			125		
Dropout voltage	for legacy chip	T_J = 25°C			1.7		V
	for new chip				1.7		V

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6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 10 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Bias current	for legacy chip	T_J = 25°C		3.8	6	mA
		T_J = 125°C			5.5	mA
	for new chip	T_J = 25°C		3.53	3.95	mA
		T_J = 125°C			4.0	
Bias current change	V_I = 8 V to 20 V, and T_J = full range (for new legacy chip)				1.5	mA
	I_O = 1 mA to 40 mA, and T_J = full range (for legacy chip)	UA78L05C			1.5	mA
		UA78L05AC and UA78L05AI			1.5	mA
	V_I = 8 V to 20 V, and T_J = full range (for new chip)				0.485	mA
	I_O = 1 mA to 40 mA, and T_J = full range (for new chip)	UA78L05C			0.01	
		UA78L05AC and UA78L05AI			0.01	

(1) Applies to UA78L05C, UA78L05AC and UA78L05AI.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L05C, UA78L05AC is T_J = 0°C to 125°C, and for the UA78L05AI is T_J = –40°C to 125°C. For new chip, temperature range for the UA78L05C, UA78L05AC and UA78L05AI is T_J = –40°C to 125°C.

6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip)

at specified junction temperature, V_I = 19 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 14 V to 27 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L12C (legacy chip)	11.1	12	12.9	V
			UA78L12AC (legacy chip)	11.5	12	12.5	
		T_J = 0°C to 125°C	UA78L12C (legacy chip)	10.8		13.2	
			UA78L12AC (legacy chip)	11.4		12.6	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L12C (legacy chip)	10.8		13.2	
			UA78L12AC (legacy chip)	11.4		12.6	
	V_I = 14 V to 27 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L12C (new chip)	11.83	12	12.31	
			UA78L12AC (new chip)				
		T_J = -40°C to 125°C	UA78L12C (new chip)	11.65		12.35	
			UA78L12AC (new chip)				
	T_J = -40°C to 125°C, and I_O = 1 mA to 70 mA		UA78L12C (new chip)	11.47		12.35	
			UA78L12AC (new chip)				
Input voltage regulation	T_J = 25°C	V_I = 14.5 V to 27 V	for legacy chip		55	250	mV
		V_I = 16 V to 27 V			49	200	
		V_I = 14.0 V to 27 V	for new chip		55	80	
		V_I = 16 V to 27 V			49	65	

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6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 19 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Ripple rejection	T_J = 25°C	V_I = 15 V to 25 V, and f = 120 Hz	UA78L12C (legacy chip)	36	42		dB
			UA78L12AC (legacy chip)	37	42		
			UA78L12C (new chip)	40	50		
			UA78L12AC (new chip)				
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA	for legacy chip		22	100	mV
		I_O = 1 mA to 40 mA			13	50	
		I_O = 1 mA to 100 mA	for new chip		22	70	
		I_O = 1 mA to 40 mA			13	30	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz	for legacy chip			70		µV
		for new chip			290		µV
Dropout voltage	T_J = 25°C	for legacy chip			1.7		V
		for new chip			1.7		
Bias current	T_J = 25°C	for legacy chip			4.3	6.5	mA
	T_J = 125°C					6	
	T_J = 25°C	for new chip			3.84	4.350	mA
	T_J = 125°C					4.355	
Bias current change	T_J = 0°C to 125°C	V_I = 16 V to 27 V (legacy chip)				1.5	mA
		I_O = 1 mA to 40 mA	UA78L12C (legacy chip)			0.2	
			UA78L12AC (legacy chip)			0.1	
	T_J = –40°C to 125°C	V_I = 16 V to 27 V (new chip)				0.450	
		I_O = 1 mA to 40 mA	UA78L12C (new chip)			0.01	
			UA78L12AC (new chip)				

(1) Applies to UA78L12C and UA78L12AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L12C, UA78L12AC is T_J = 0°C to 125°C. For new chip, temperature range for the UA78L12C and UA78L12AC is T_J = –40°C to 125°C.

6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only)

at specified junction temperature, V_I = 12 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L06C	5.7	6.2	6.7	V
			UA78L06AC	5.95	6.2	6.45	
		T_J = 0°C to 125°C	UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
Input voltage regulation	T_J = 25°C	V_I = 8.5 V to 20 V	UA78L06C		35	200	mV
			UA78L06AC		35	175	
		V_I = 9 V to 20 V	UA78L06C		29	150	
			UA78L06AC		29	125	
Ripple rejection	T_J = 25°C, V_I = 10 V to 20 V, and f = 120 Hz		UA78L06C	39	48		dB
			UA78L06AC	40	48		

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6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only) (continued)

at specified junction temperature, V_I = 12 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS[2]			MIN	TYP	MAX	UNIT
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			16	80	mV
		I_O = 1 mA to 40 mA			9	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz				46		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				3.9	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 9 V to 20 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L06C			0.2	
			UA78L06AC			0.1	

(1) Applies to UA78L06C and UA78L06AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L06C and UA78L06AC is T_J = 0°C to 125°C.

6.10 Electrical Characteristics: UA78L08 (Legacy Chip Only)

at specified junction temperature, V_I = 14 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS[2]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L08C	7.36	8	8.64	V
			UA78L08AC	7.7	8	8.3	
		T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
	I_O = 1 mA to 70 mA	T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
Input voltage regulation	T_J = 25°C	V_I = 10.5 V to 23 V	UA78L08C		42	200	mV
			UA78L08AC		42	175	
		V_I = 11 V to 23 V	UA78L08C		36	150	
			UA78L08AC		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz, and T_J = 25°C		UA78L08C	36	46		dB
			UA78L08AC	37	46		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			18	80	mV
		I_O = 1 mA to 40 mA			10	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				54		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 11 V to 23 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L08C			0.2	
			UA78L08AC			0.1	

(1) Applies to UA78L08C and UA78L08AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L08C and UA78L08AC is T_J = 0°C to 125°C.

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6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only)

at specified junction temperature, V_I = 16 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L09C	8.3	9	9.7	V
			UA78L09AC	8.6	9	9.4	
		T_J = 0°C to 125°C	UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
Input voltage regulation	T_J = 25°C	V_I = 12 V to 24 V	UA78L09C		45	225	mV
			UA78L09AC		45	175	
		V_I = 13 V to 24 V	UA78L09C		40	175	
			UA78L09AC		40	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz, and T_J = 25°C		UA78L09C	36	45		dB
			UA78L09AC	38	45		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			19	90	mV
		I_O = 1 mA to 40 mA			11	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				58		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4.1	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 13 V to 24 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L09C			0.2	
			UA78L09AC			0.1	

(1) Applies to UA78L09C ad UA78L09AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L09C and UA78L09AC is T_J = 0°C to 125°C.

6.12 Electrical Characteristics: UA78L10 (Legacy Chip Only)

at specified junction temperature, V_I = 14 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 25 V, and I_O = 1 mA to 40 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		9.5		10.5	
Input voltage regulation	T_J = 25°C	V_I = 13 V to 25 V		51	175	mV
		V_I = 14 V to 25 V		42	125	
Ripple rejection	T_J = 25°C, V_I = 15 V to 25 V, and f = 120 Hz		37	44		dB
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA		20	90	mV
		I_O = 1 mA to 40 mA		11	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz			62		µV
Dropout voltage	T_J = 25°C			1.7		V
Bias current	T_J = 25°C			4.2	6	mA
	T_J = 125°C				5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 14 V to 25 V			1.5	mA
		I_O = 1 mA to 40 mA			0.1	

(1) Applies to UA78L10AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L10AC is T_J = 0°C to 125°C.

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6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip)

at specified junction temperature, V_I = 23 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS (2)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 17.5 V to 30 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L15C (legacy chip)	13.8	15	16.2	V
			UA78L15AC (legacy chip)	14.4	15	15.6	V
		T_J = 0°C to 125°C	UA78L15C (legacy chip)	13.5		16.5	V
			UA78L15AC (legacy chip)	14.25		15.75	V
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L15C (legacy chip)	13.5		16.5	V
			UA78L15AC (legacy chip)	14.25		15.75	V
	V_I = 17.5 V to 30 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L15C (new chip)	14.750	15	15.425	V
			UA78L15AC (new chip)	14.750	15	15.425	
		T_J = -40°C to 125°C	UA78L15C (new chip)	14.575		15.450	
			UA78L15AC (new chip)	14.575		15.450	
	T_J = -40°C to 125°C, and I_O = 1 mA to 70 mA		UA78L15C (new chip)	14.35		15.45	
			UA78L15AC (new chip)	14.35		15.45	
Input voltage regulation	T_J = 25°C	V_I = 17.5 V to 30 V	for legacy chip		65	300	mV
		V_I = 20 V to 30 V			58	250	
		V_I = 17.5 V to 30 V	for new chip		65	82	
		V_I = 20 V to 30 V			58	60	
Ripple rejection	T_J = 25°C	V_I = 18.5 V to 28.5 V, and f = 120 Hz	UA78L15C (legacy chip)	33	39		dB
			UA78L15AC (legacy chip)	34	39		
		V_I = 18.5 V to 28.5 V, and f = 120 Hz	UA78L15C (new chip)	40	45		
			UA78L15AC (new chip)	40	45		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA	for legacy chip		25	150	mV
		I_O = 1 mA to 40 mA			15	75	
		I_O = 1 mA to 100 mA	for new chip		25	27	
		I_O = 1 mA to 40 mA			15	60	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz	for legacy chip			82		µV
		for new chip			388		
Dropout voltage	T_J = 25°C	for legacy chip			1.7		V
		for new chip			1.7		
Bias current	T_J = 25°C	for legacy chip			4.6	6.5	mA
	T_J = 125°C					6	
	T_J = 25°C	for new chip			4.1	4.670	
	T_J = 125°C					4.675	

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6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip) (continued)

at specified junction temperature, V_I = 23 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF and I_O = 40 mA (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS (2)			MIN	TYP	MAX	UNIT
Bias current change	T_J = 0°C to 125°C	V_I = 10 V to 30 V	legacy chip			1.5	mA
		I_O = 1 mA to 40 mA	UA78L15C (legacy chip)			0.2	
			UA78L15AC (legacy chip)			0.1	
	T_J = -40°C to 125°C	V_I = 20 V to 30 V	new chip			0.425	
		I_O = 1 mA to 40 mA	UA78L15C (new chip)			0.01	
			UA78L15AC (new chip)			0.02	

(1) Applies to UA78L15C and UA78L15AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L15C, UA78L15AC is T_J = 0°C to 125°C. For new chip, temperature range for the UA78L15C and UA78L15AC is T_J = –40°C to 125°C.

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6.14 Typical Characteristics

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

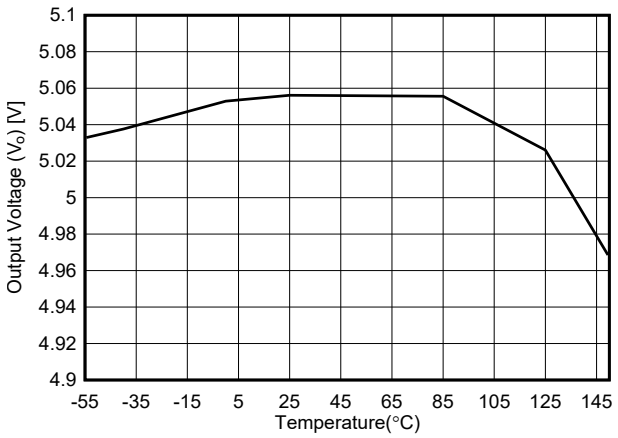


图 6-1. V_O vs Temperature for New Chip

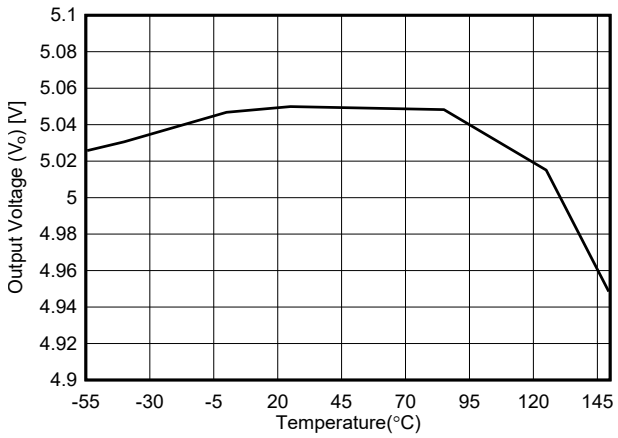


图 6-2. V_O vs Temperature for New Chip

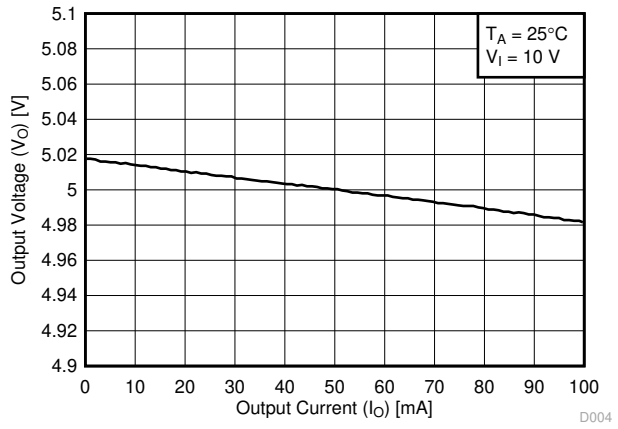


图 6-3. Load Regulation for Legacy Chip

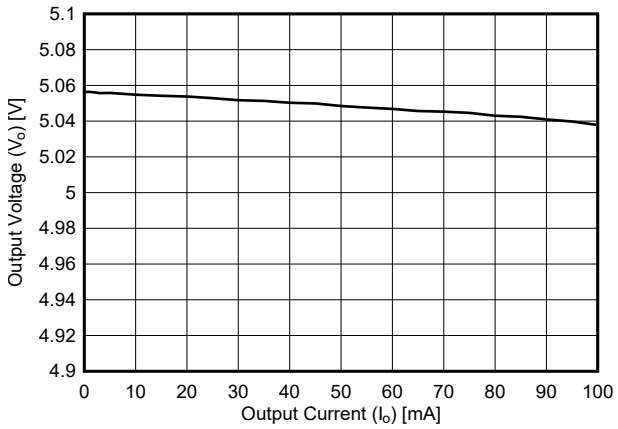


图 6-4. Load Regulation for New Chip at T_J = 25°C

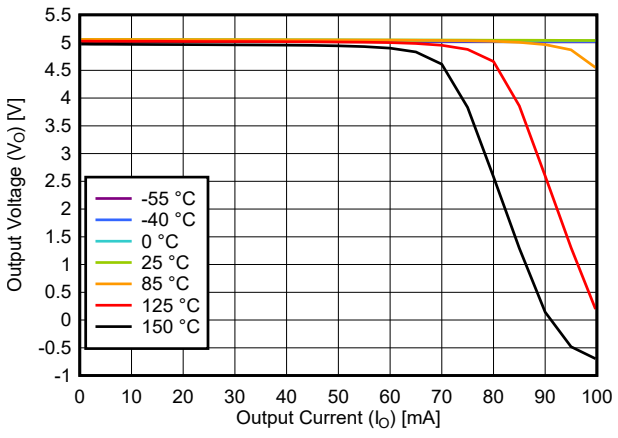
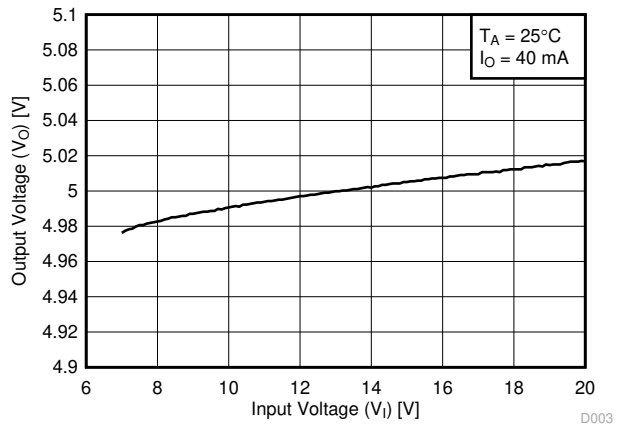


图 6-5. Load Regulation for New Chip



I_O = 40 mA

图 6-6. Line Regulation at I_O = 40 mA for Legacy Chip

6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

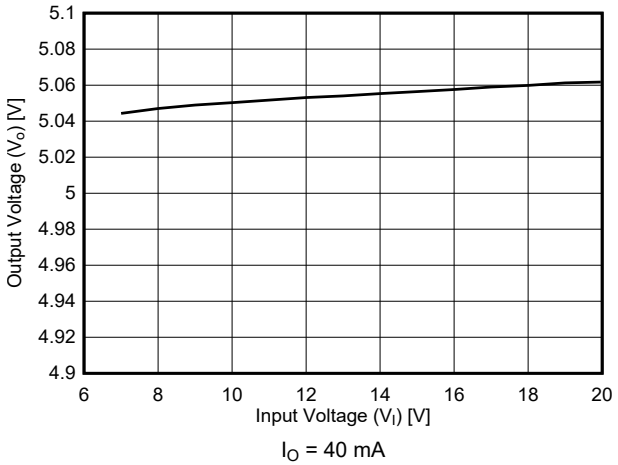


图 6-7. Line Regulation at I_O = 40 mA for New Chip at T_J = 25°C

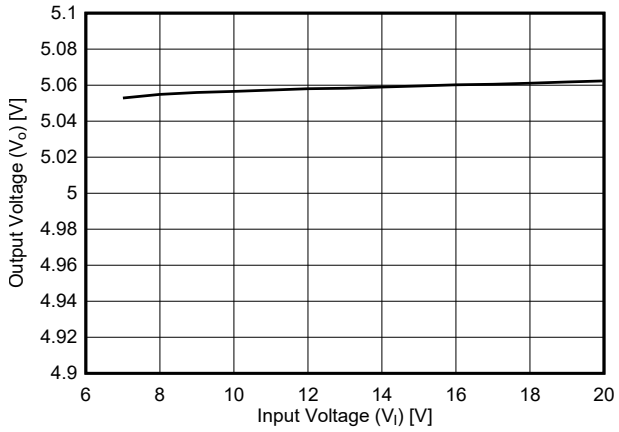


图 6-8. Line Regulation at I_O = 1 mA for New Chip at T_J = 25°C

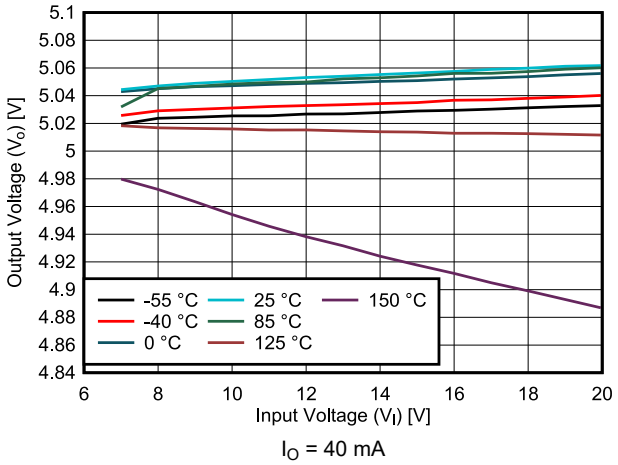


图 6-9. Line Regulation at I_O = 40 mA for New Chip

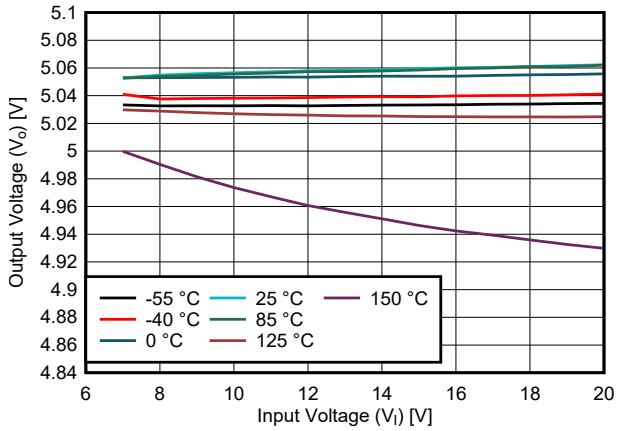


图 6-10. Line Regulation at I_O = 1 mA for New Chip

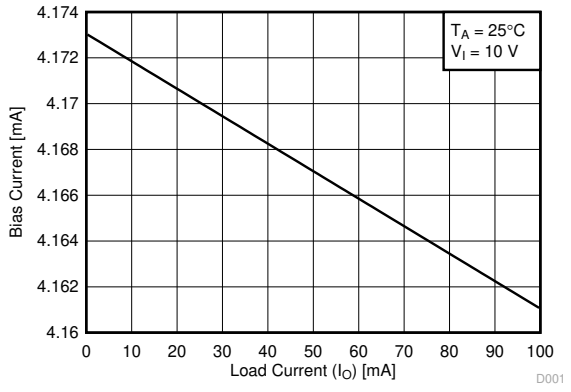


图 6-11. Bias Current vs Load Current for Legacy Chip

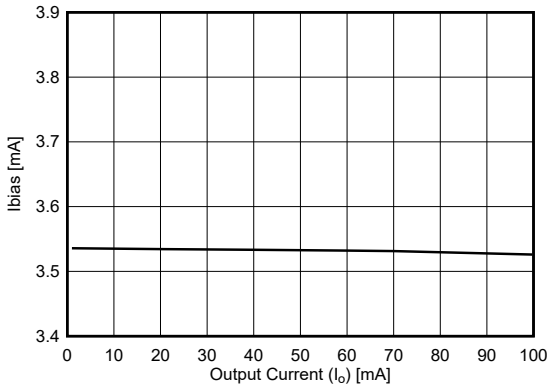


图 6-12. Bias Current vs Load Current for New Chip at T_J = 25°C

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6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)

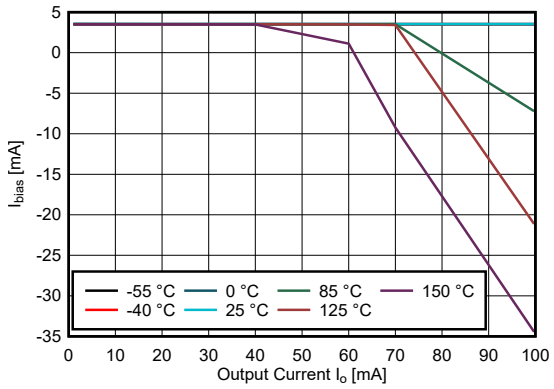
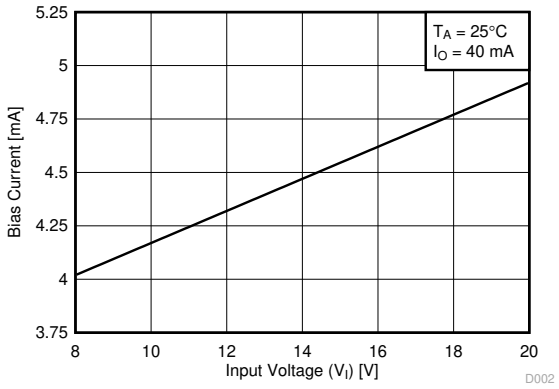
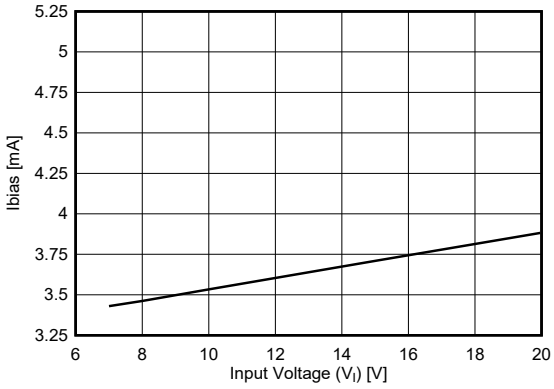


图 6-13. Bias Current vs Load Current for New Chip



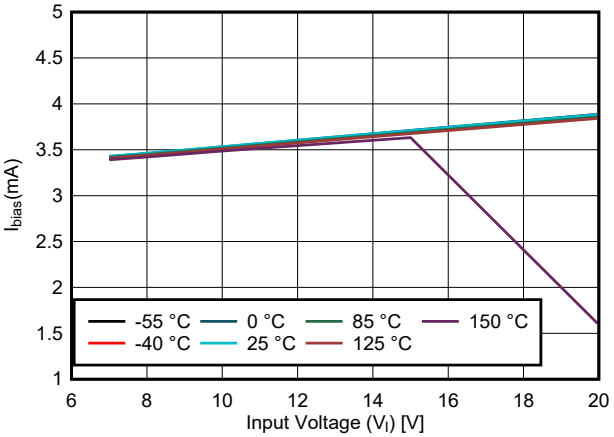
I_O = 40 mA

图 6-14. Bias Current vs Input Voltage for Legacy Chip



I_O = 40 mA

图 6-15. Bias Current vs Input Voltage for New Chip at T_J = 25°C



I_O = 40 mA

图 6-16. Bias Current vs Input Voltage for New Chip

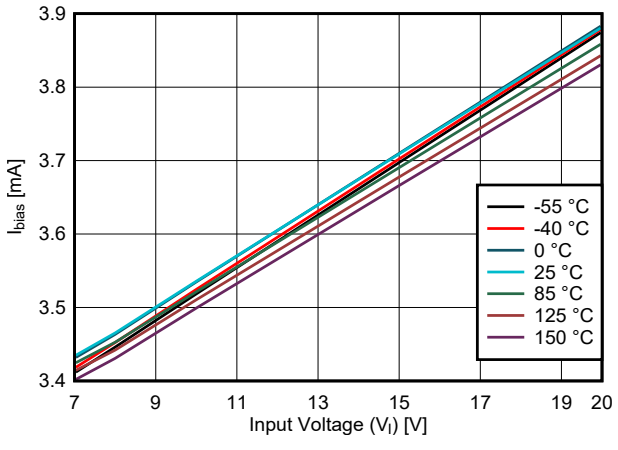
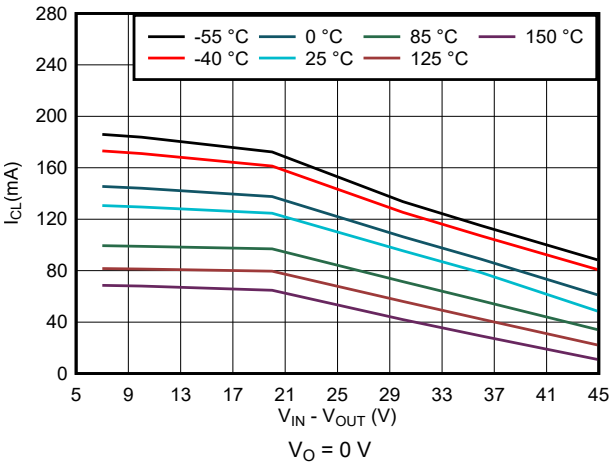


图 6-17. Bias Current vs Input Voltage at I_O = 1 mA for New Chip



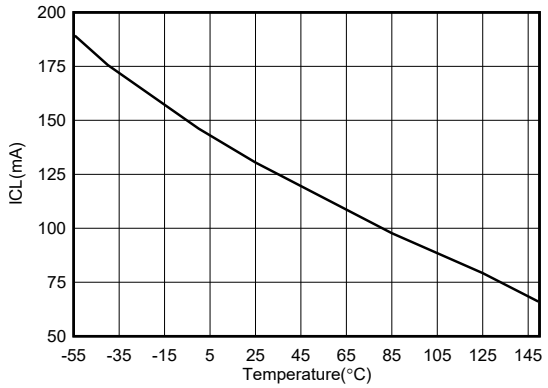
V_O = 0 V

图 6-18. I_{SC} vs V_I for New Chip

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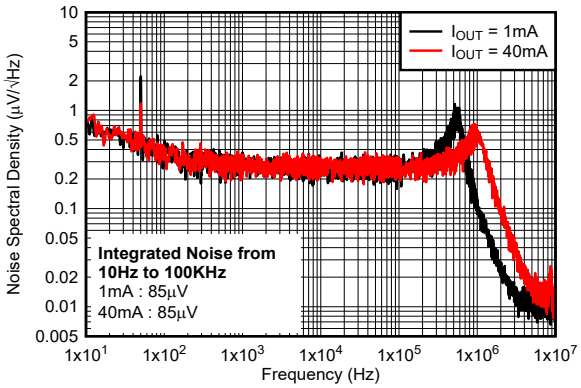
6.14 Typical Characteristics (continued)

at specified junction temperature T_J = 25 °C, V_I = 10 V, V_O = 5 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 1 mA (unless otherwise noted)



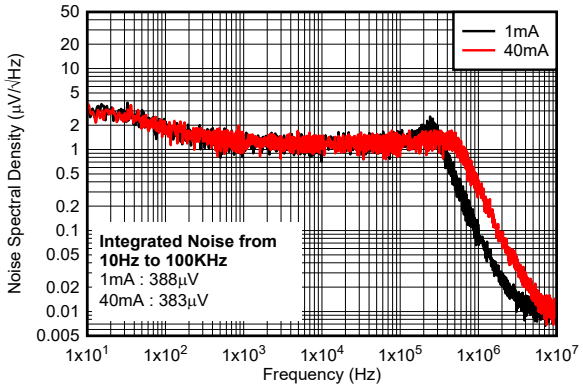
V_O = 90% of V_O (typ)

图 6-19. I_{CL} vs Temperature for New Chip



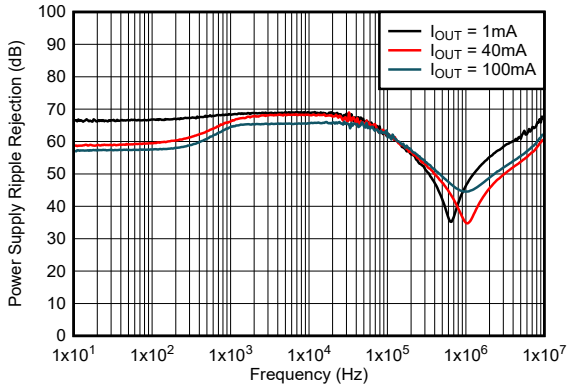
V_I = 9 V, V_O = 3.3 V

图 6-20. Noise Spectral Density vs Frequency and I_O for New Chip



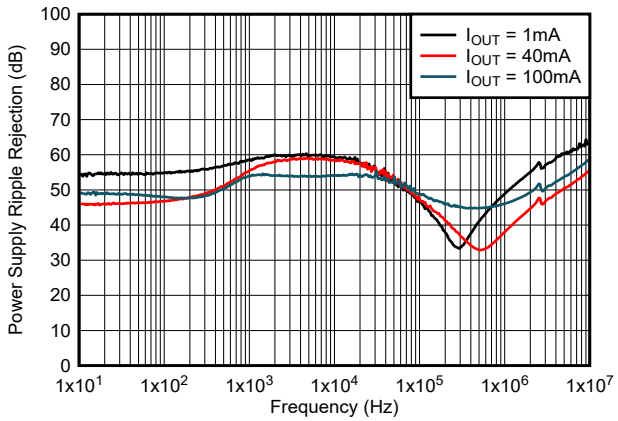
V_I = 23 V, V_O = 15 V

图 6-21. Noise Spectral Density vs Frequency and I_O for New Chip



V_I = 9 V, V_O = 3.3 V

图 6-22. PSRR vs Frequency and I_O for New Chip



V_I = 23 V, V_O = 15 V

图 6-23. PSRR vs Frequency and I_O for New Chip

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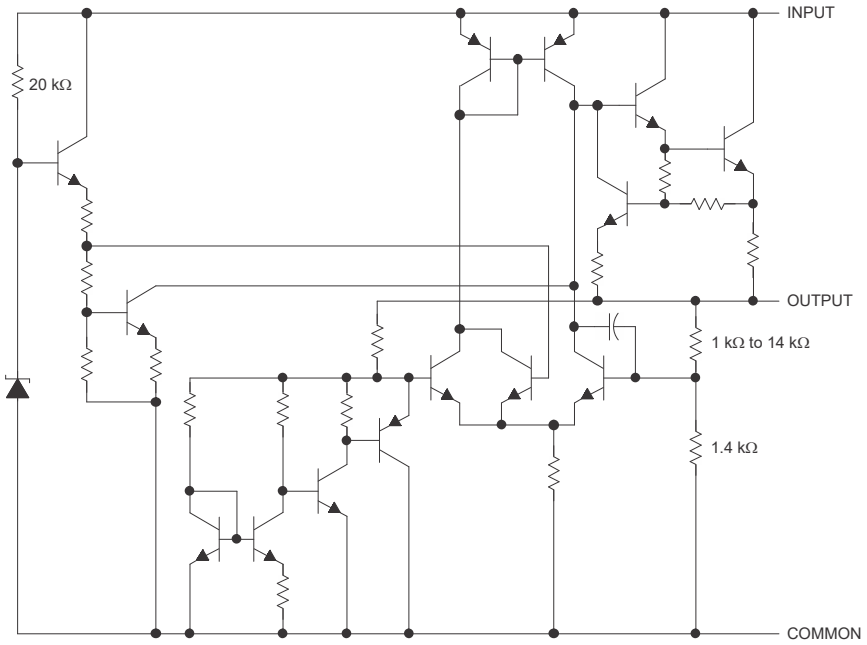
7 Detailed Description

7.1 Overview

The UA78L series of fixed-voltage, integrated-circuit voltage regulators is designed for a wide range of applications. The UA78L series supports a wide range of input voltages and can deliver 100 mA of load current.

This device features internal current-limiting and thermal shutdown mechanisms. To provide reliable operation across wide V_I ranges, the current-limiting mechanism modulates the load current capacity both by monitoring the V_O level and the difference between the V_I and V_O voltage levels. The operating ambient temperature range of the device is –40°C to +125°C for all variants of the new chip.

7.2 Functional Block Diagram



NOTE: Resistor values shown are nominal.

7.3 Feature Description

7.3.1 Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. In a high-load current fault, the current limit scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [$(V_I - V_O) \times I_{CL}$]. For more information on current limits, see the *Know Your Limits* application note.

To achieve a safe operation across a wide range of Input voltage, the UA78L series also has a built-in protection mechanism with current limit. The protection mechanism decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage limits defined in the *Recommended Operating Conditions* table. 图 7-1 shows the behavior of the current limit variation.

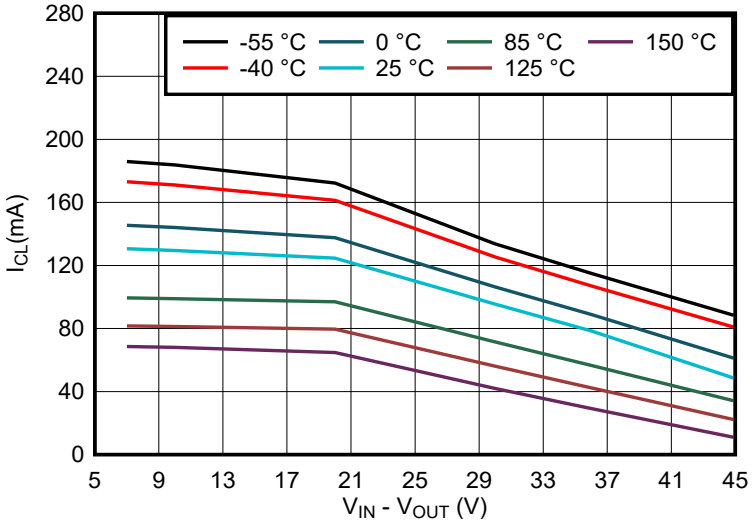


图 7-1. Current-Limit vs $V_{Head-room}$ Behavior for New Chip Only

7.3.2 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_I – V_O voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_I – V_O) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_O listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

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7.4 Device Functional Modes

表 7-1 provides a quick comparison between the normal and dropout modes of operation.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_I	I_O
Normal	$V_I > V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$
Dropout	$V_I < V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_O < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_I < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

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8 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The UA78L series is designed for use as a linear regulator with only a few external components needed. The UA78L can also be used to clean power-supply noise by attenuating ripple on the input signal.

8.2 Typical Application

The UA78L series is typically used as a fixed-output linear regulator, sourcing current up to 100 mA into a load.

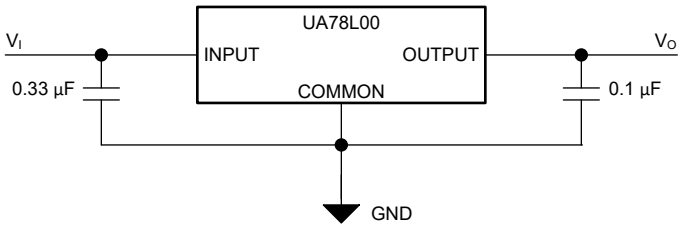


图 8-1. Fixed-Output Regulator

8.2.1 Design Requirements

The COMMON pin must be tied to ground to set the OUTPUT pin to the desired fixed output voltage.

Although not required, a 0.33-µF bypass capacitor is recommended on the input, and a 0.1-µF bypass capacitor is recommend on the output.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although both input and output capacitor are not required for stability, good analog design practice is to connect a capacitor from IN to COMMON and from OUT to COMMON. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.2.2.2 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_I - V_O) \times I_O \quad (1)$$

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备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

8.2.2.3 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (3)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

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$$T_J = T_B + \psi_{JB} \times P_D \quad (4)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2.2.4 External Capacitor Requirements

The UA78L is designed to be stable without any external component. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.2.2.5 Overload Recovery

As the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur where removing an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so the behavior is not unique to the UA78L.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after removing a short circuit or when the shutdown pin is pulled high after the input voltage is already turned on. The load line for such a load has the possibility to intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply can possibly need to be cycled down to zero and brought up again to make the output recover to the desired voltage operating point.

8.2.2.6 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_O \leqslant V_I + 7$ V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

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图 8-2 shows one approach for protecting the device.

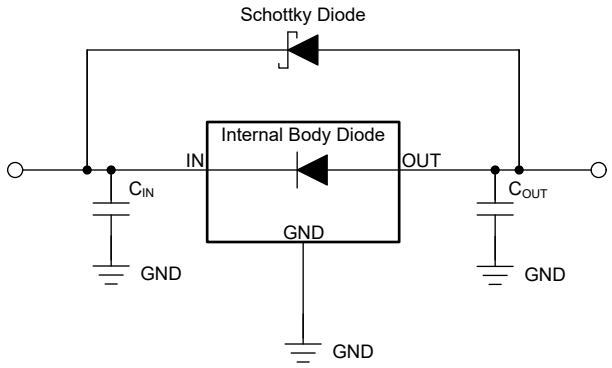


图 8-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.2.2.7 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection can lead to polarity reversal of the regulator output and can damage the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

图 8-3 shows one approach for protecting the device.

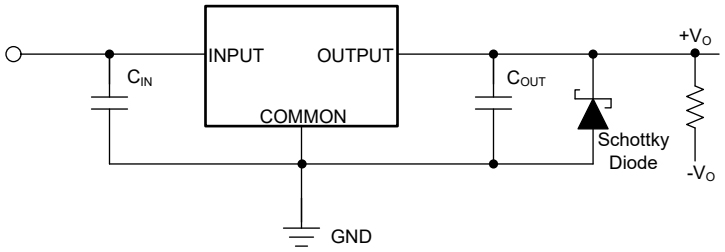


图 8-3. Example Circuit for Polarity Reversal Protection Using a Schottky Diode

8.2.3 Application Curves

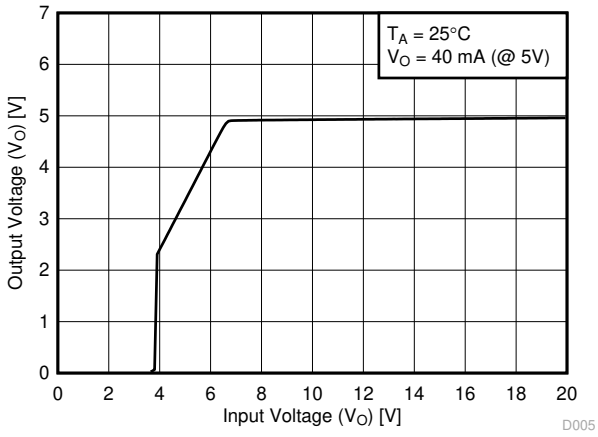


图 8-4. Output Voltage vs Input Voltage for Legacy Chip

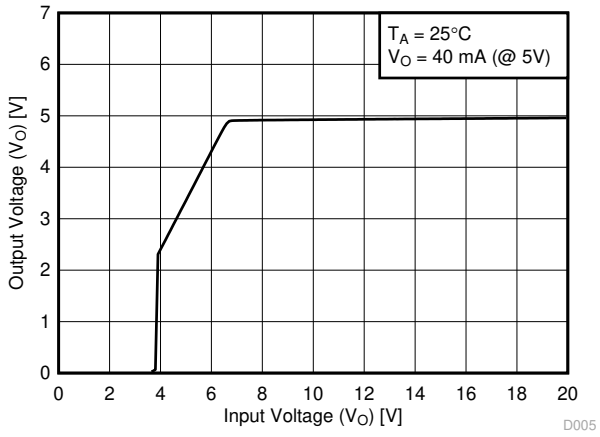
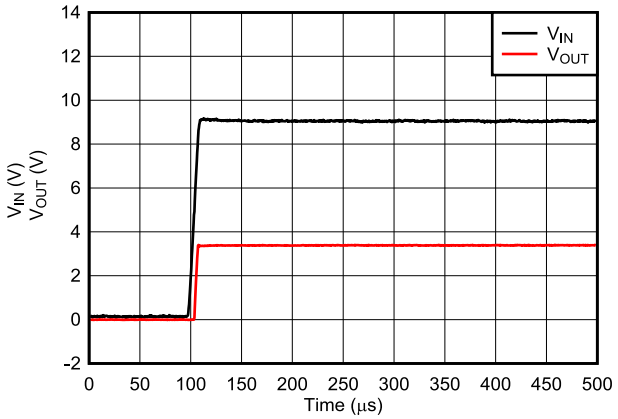
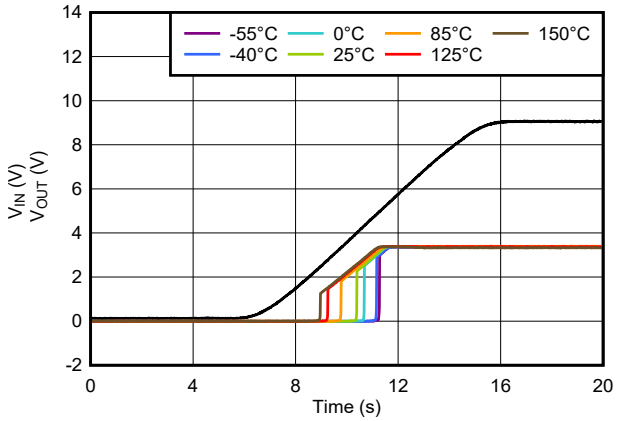


图 8-5. Output Voltage vs Input Voltage for New Chip



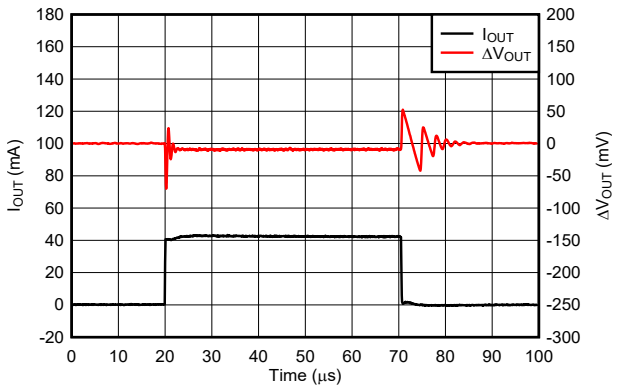
V_O = 3.3 V

图 8-6. Start-Up With Fast V_I Ramp for New Chip



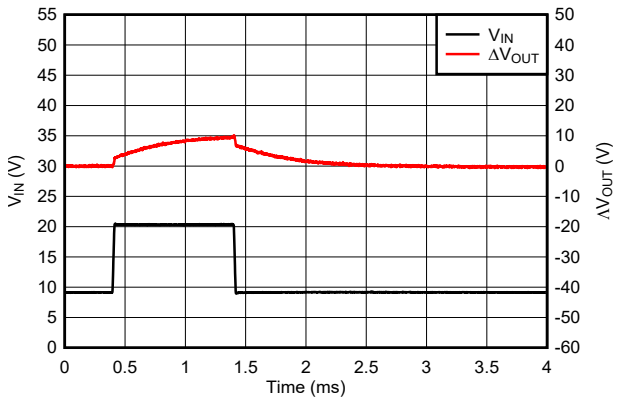
V_O = 3.3 V

图 8-7. Start-Up With Slow V_I Ramp Across Temperature for New Chip



V_O = 3.3 V, dI_O/dt = 1 A/ µ s

图 8-8. Load Transient Behavior for New Chip



V_O = 3.3 V, dV_{IN}/dt = 1 V/ µ s

图 8-9. Line Transient Behavior for New Chip

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8.3 System Examples

8.3.1 Positive Regulator in Negative Configuration

图 8-10 shows the UA78L as a positive regulator used in a negative configuration.

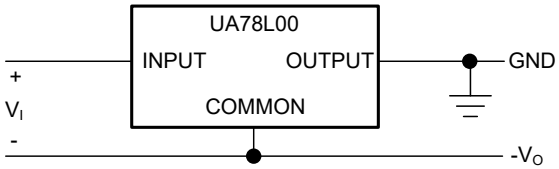


图 8-10. Positive Regulator in Negative Configuration (V_I Must Float)

8.3.2 Current Limiter Circuit

图 8-11 shows an example of using the UA78L as a current limiter. The output current limit is set by 方程式 5.

$$I_O = \left(\frac{V_O}{R1}\right) + I_O \text{ Bias Current} \quad (5)$$

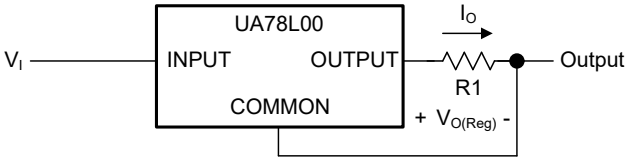


图 8-11. Current Limiter Example

8.4 Power Supply Recommendations

See the *Recommended Operating Conditions* table for the recommended power-supply voltages for each variation of the UA78L. Each device variant can have a different recommended maximum operating voltage.

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8.5 Layout

8.5.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output pins. Place bypass capacitors as close to the UA78L as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

8.5.2 Layout Example

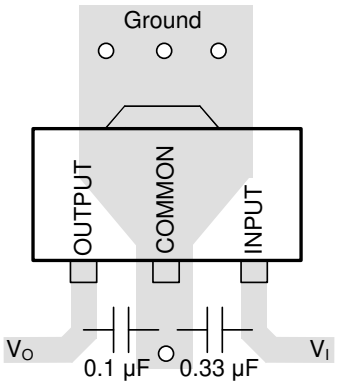


图 8-12. Example Layout for the PK Package

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the UA78L. The UA78LEVM-075 (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.2 Device Nomenclature

表 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
UA78L**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example, 05 = 5.0 V, 15 = 15.0 V). **yyy** is the package designator. **z** is the package quantity.
UA78L**xxyyyz M3** New chip	**xx** is the nominal output voltage (for example, 05 = 5.0 V, 15 = 15.0 V). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUA78L033AIPK	Active	Preproduction	SOT-89 (PK) | 3	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUA78L033AIPK.A	Active	Preproduction	SOT-89 (PK) | 3	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUA78L05ACPKM3	Active	Preproduction	SOT-89 (PK) | 3	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUA78L05ACPKM3.A	Active	Preproduction	SOT-89 (PK) | 3	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UA78L02ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A
UA78L02ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A
UA78L02ACDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A
UA78L02ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L02AC
UA78L02ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L02AC
UA78L02ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L02AC
UA78L033AIPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	O7
UA78L033AIPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	O7
UA78L033AIPKR2	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	O7
UA78L033AIPKR2.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	O7
UA78L05ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDE4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A
UA78L05ACDRM3	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05A
UA78L05ACDRM3.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05A
UA78L05ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPM	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78L05ACLPM.A	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPME3	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L05AC
UA78L05ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F5
UA78L05ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F5
UA78L05ACPKE6	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	0 to 125	F5
UA78L05ACPKE6.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	0 to 125	F5
UA78L05ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F5
UA78L05ACPKM3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	F5
UA78L05ACPKM3.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	F5
UA78L05AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI
UA78L05AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI
UA78L05AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI
UA78L05AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI
UA78L05AIDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI
UA78L05AILP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AILP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AILPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AILPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AILPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AILPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	78L05AI
UA78L05AIPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	J5
UA78L05AIPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	J5
UA78L05AIPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	J5
UA78L05CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C
UA78L05CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C
UA78L05CDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C
UA78L05CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C
UA78L05CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78L05CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C
UA78L05CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05C
UA78L05CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05C
UA78L05CLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L05C
UA78L05CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L05C
UA78L05CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L05C
UA78L05CPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	B5
UA78L05CPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	B5
UA78L05CPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	B5
UA78L06ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L06AC
UA78L06ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L06AC
UA78L06ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L06AC
UA78L06ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L06AC
UA78L06ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L06AC
UA78L06ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F6
UA78L06ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F6
UA78L06ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F6
UA78L08ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A
UA78L08ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L08AC
UA78L08ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F8
UA78L08ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F8

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78L08ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F8
UA78L09ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A
UA78L09ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A
UA78L09ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A
UA78L09ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A
UA78L09ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A
UA78L09ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L09AC
UA78L09ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F9
UA78L09ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F9
UA78L09ACPKE6	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	0 to 125	F9
UA78L09ACPKE6.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	0 to 125	F9
UA78L09ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	F9
UA78L10ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A
UA78L10ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A
UA78L10ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A
UA78L10ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A
UA78L10ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A
UA78L10ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L10AC
UA78L10ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FA
UA78L10ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FA
UA78L10ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78L12ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A
UA78L12ACDRM3	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L12A
UA78L12ACDRM3.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L12A
UA78L12ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLPM	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLPM.A	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L12AC
UA78L12ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FC
UA78L12ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FC
UA78L12ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FC
UA78L15ACD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A
UA78L15ACD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A
UA78L15ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A
UA78L15ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A
UA78L15ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A
UA78L15ACDRM3	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L15A
UA78L15ACDRM3.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L15A
UA78L15ACLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC
UA78L15ACLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC
UA78L15ACLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC
UA78L15ACLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78L15ACLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC
UA78L15ACLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	78L15AC
UA78L15ACPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FF
UA78L15ACPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FF
UA78L15ACPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	FF
UA78L15ACPKM3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	FF
UA78L15ACPKM3.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	FF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

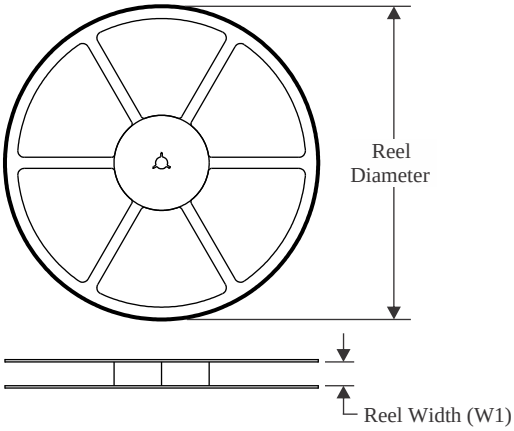
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

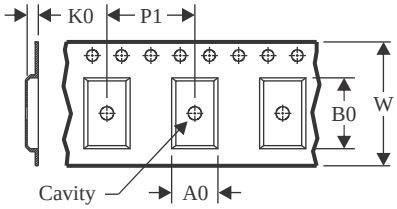
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

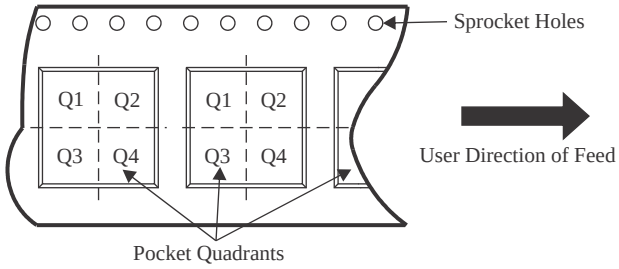


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

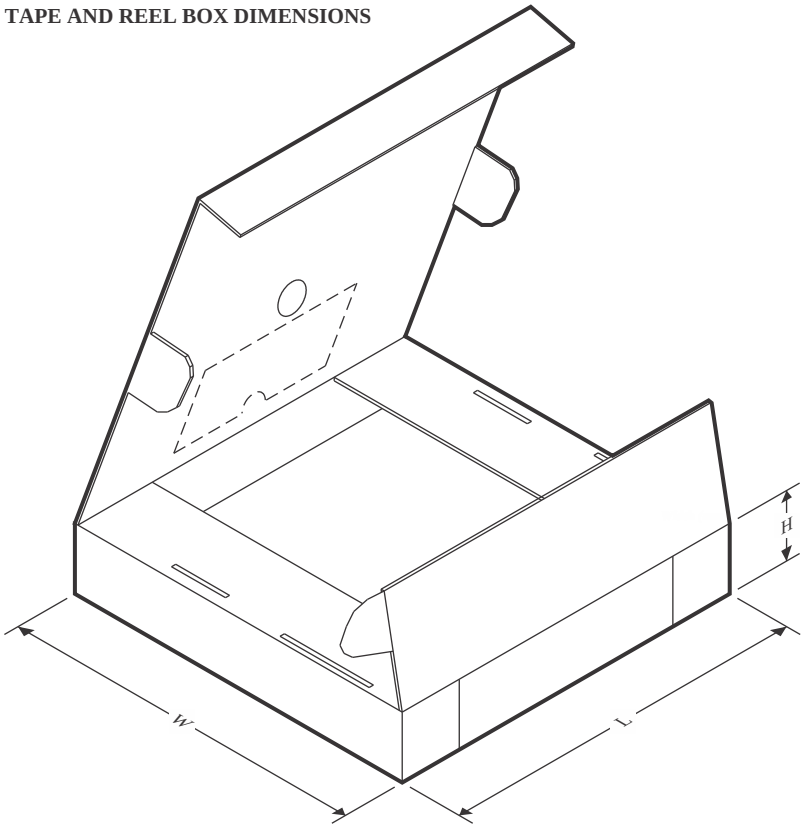


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L033AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDRM3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPKM3	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L06ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L08ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L08ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L09ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L10ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L10ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDRM3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L12ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACDRM3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACPKM3	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

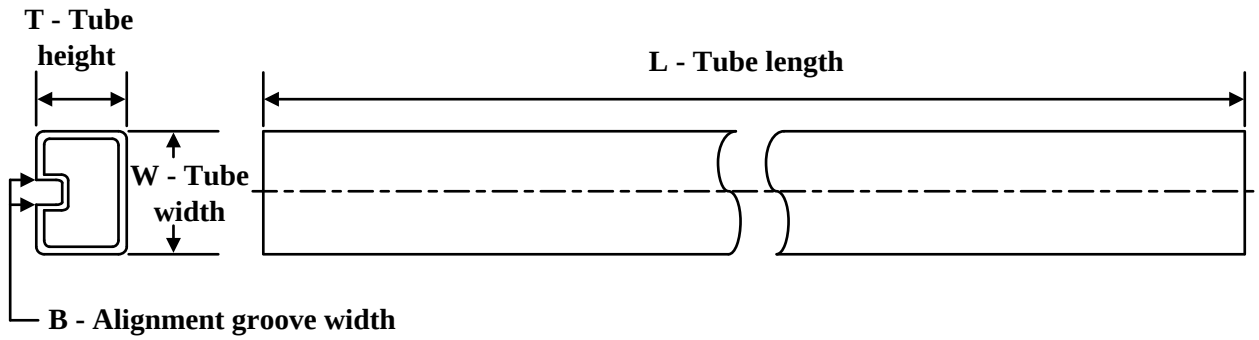


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L033AIPK	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L05ACDRG4	SOIC	D	8	2500	353.0	353.0	32.0
UA78L05ACDRG4	SOIC	D	8	2500	533.4	186.0	36.0
UA78L05ACDRM3	SOIC	D	8	2500	353.0	353.0	32.0
UA78L05ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L05ACPKM3	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L05AIDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L05AIDR	SOIC	D	8	2500	533.4	186.0	36.0
UA78L05AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05CDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L05CPK	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L05CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L06ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L08ACDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L08ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L08ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L09ACDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L09ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L10ACDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L10ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L12ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L12ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACDRM3	SOIC	D	8	2500	353.0	353.0	32.0
UA78L12ACPK	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L12ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACDR	SOIC	D	8	2500	353.0	353.0	32.0
UA78L15ACDRM3	SOIC	D	8	2500	353.0	353.0	32.0
UA78L15ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACPK	SOT-89	PK	3	1000	190.0	190.0	30.0
UA78L15ACPKM3	SOT-89	PK	3	1000	190.0	190.0	30.0

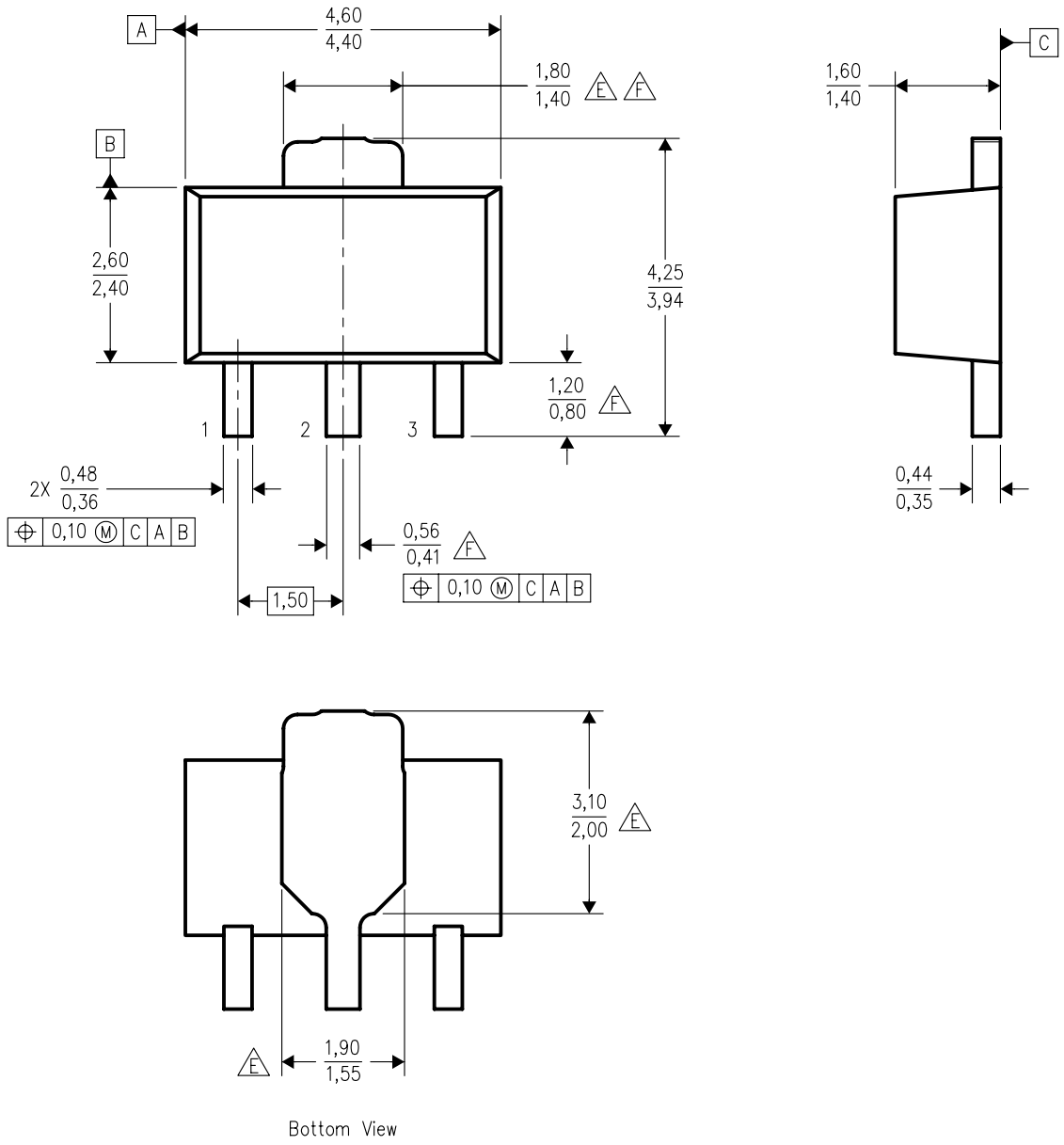
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA78L02ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L02ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L02ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDE4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05AID	D	SOIC	8	75	507	8	3940	4.32
UA78L05AID.A	D	SOIC	8	75	507	8	3940	4.32
UA78L05CD	D	SOIC	8	75	507	8	3940	4.32
UA78L05CD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L05CDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L08ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L08ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L09ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L09ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L10ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L10ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L15ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L15ACD.A	D	SOIC	8	75	507	8	3940	4.32

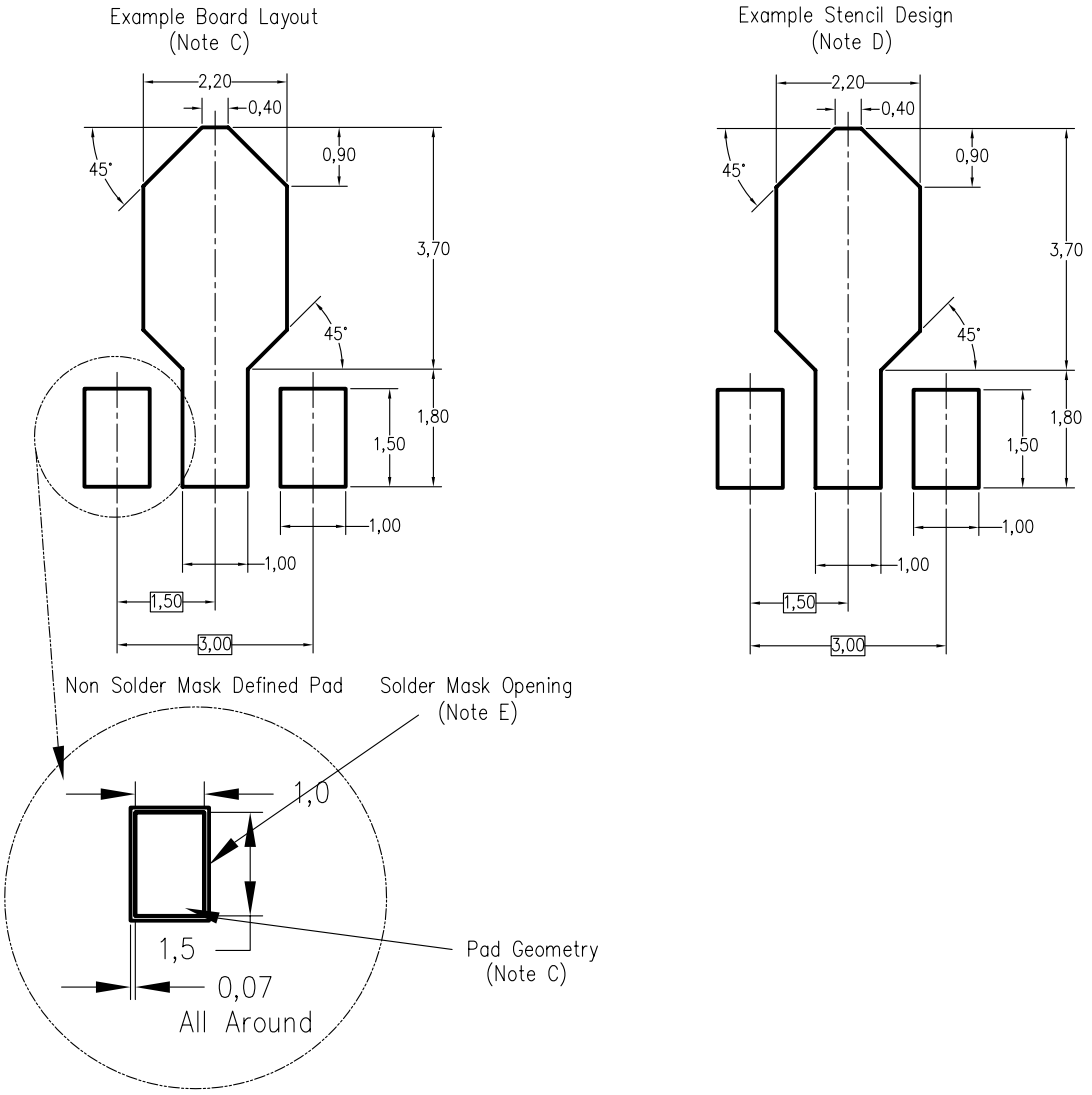
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

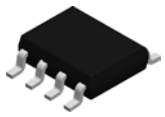
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



4208221/A 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

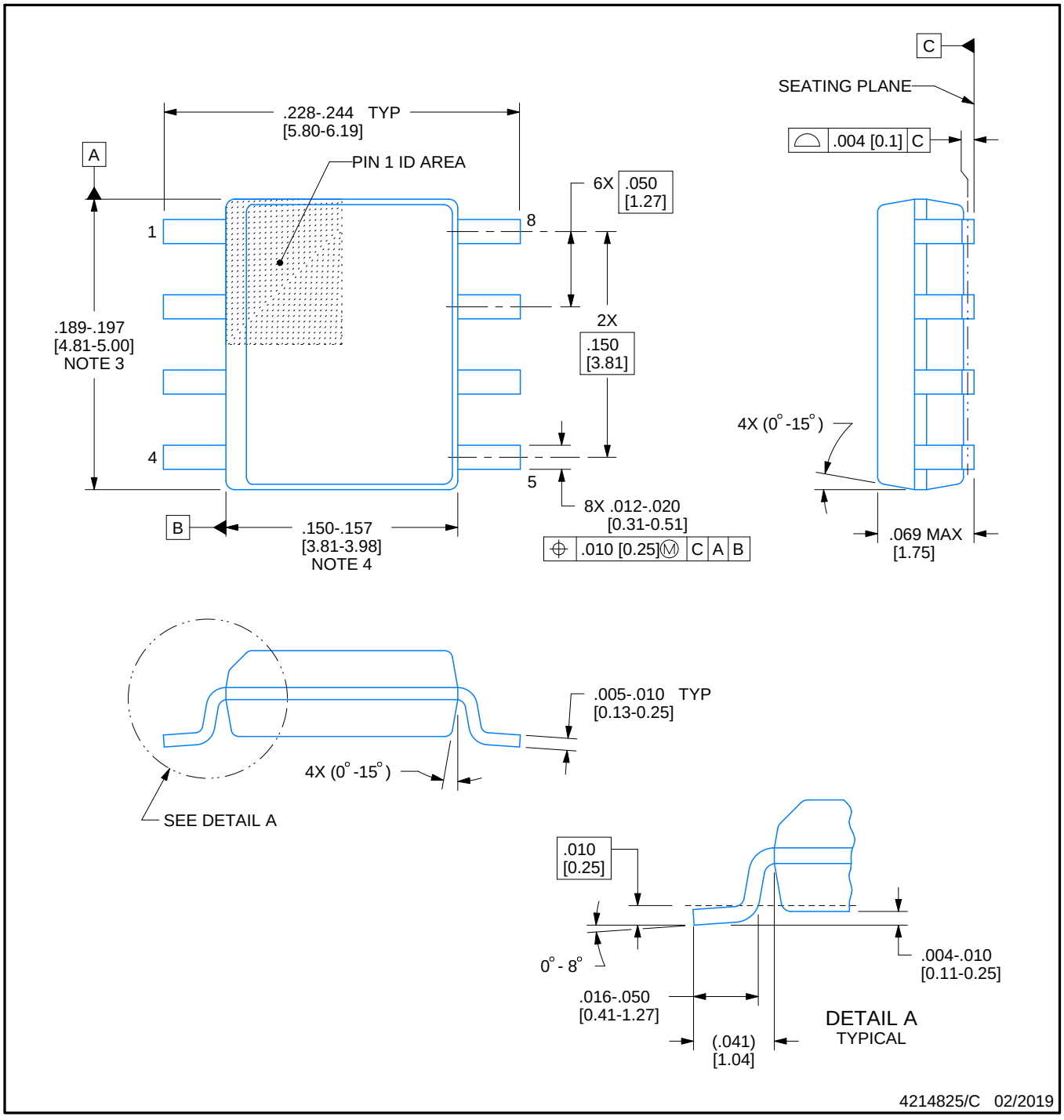


PACKAGE OUTLINE

D0008A

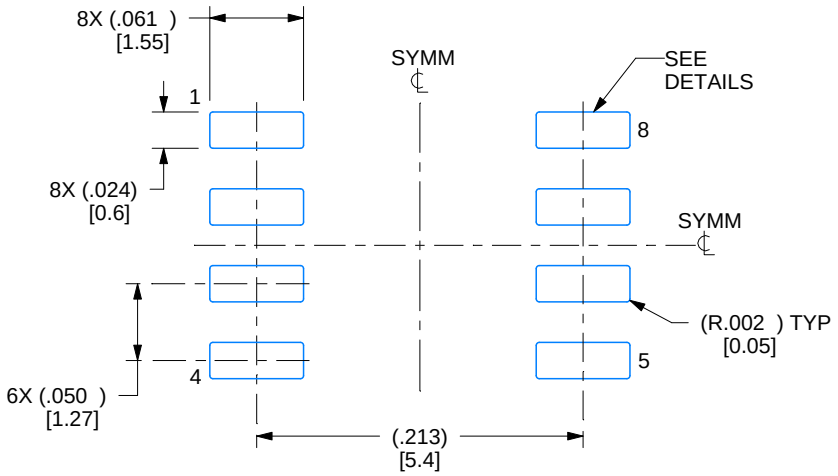
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

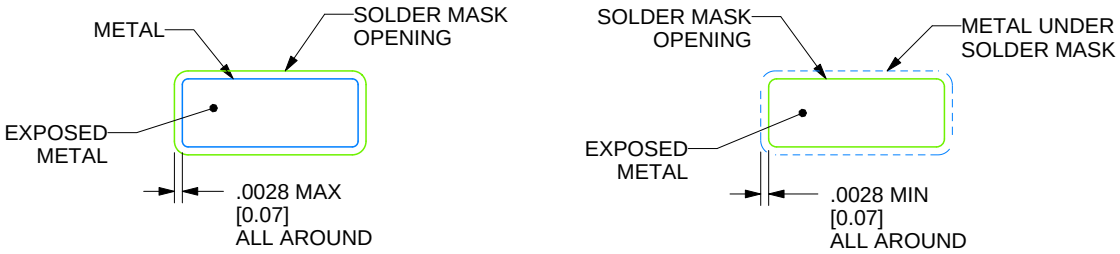


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

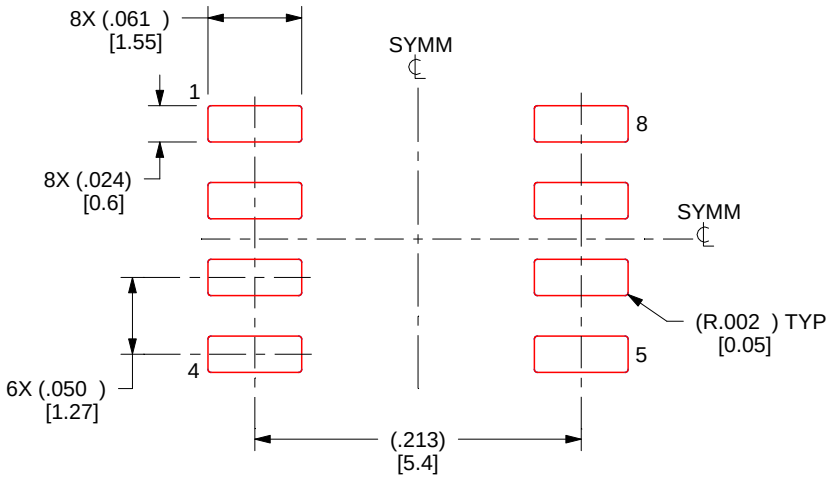
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

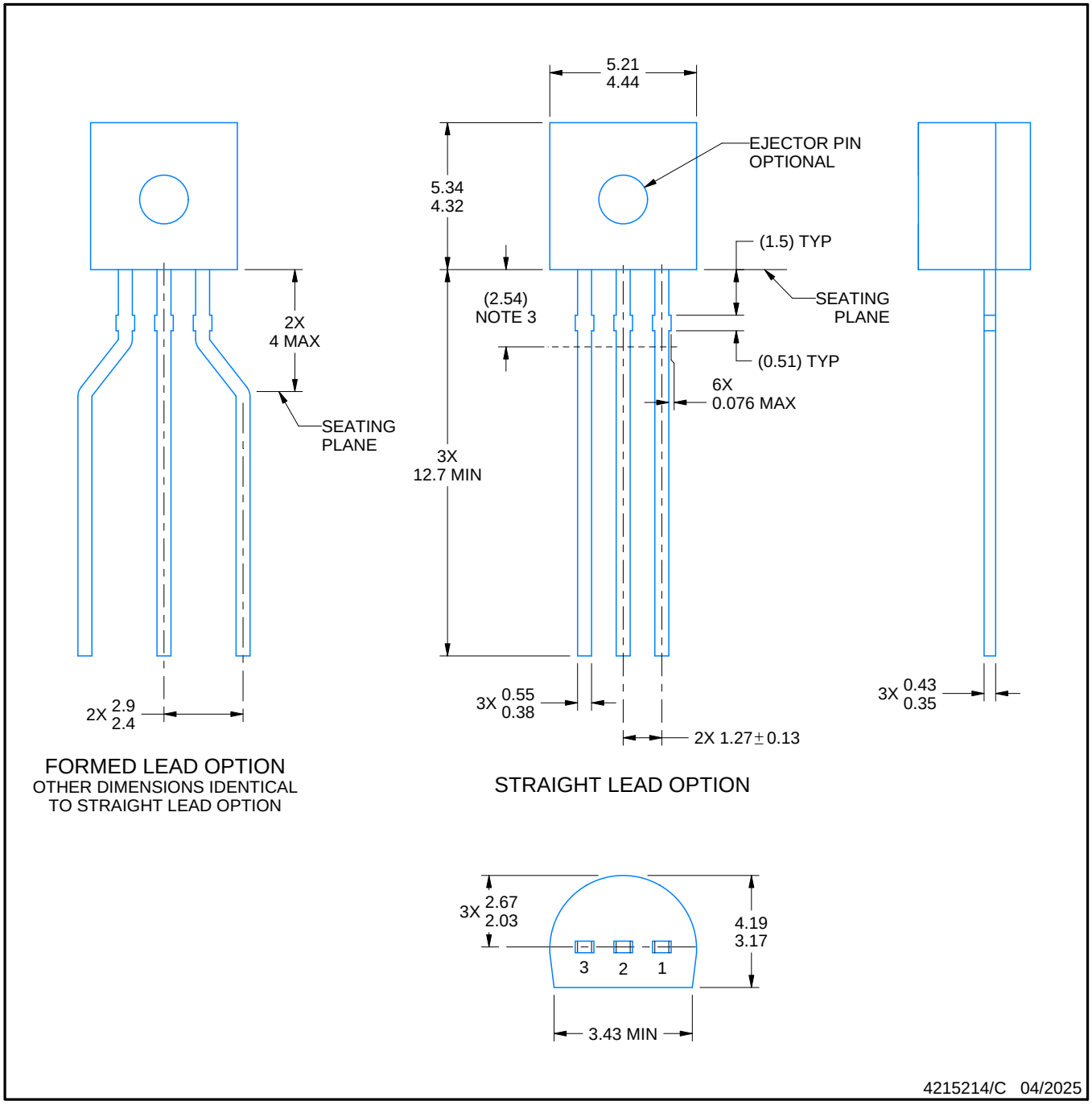
LP0003A



PACKAGE OUTLINE

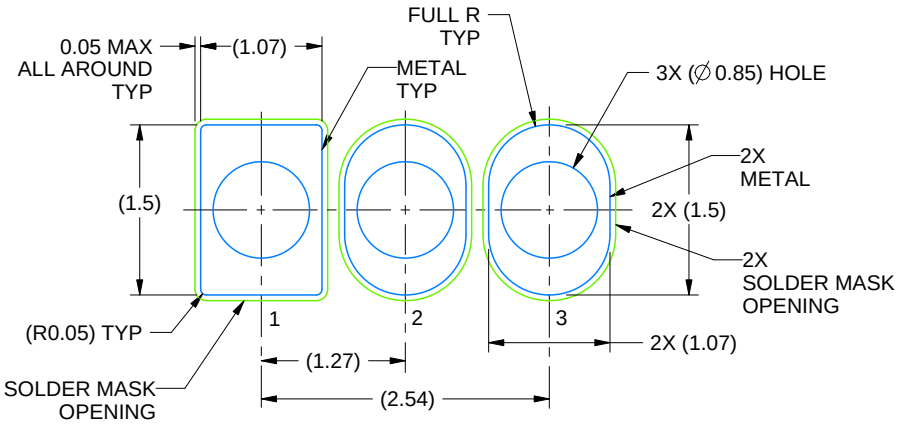
TO-92 - 5.34 mm max height

TO-92

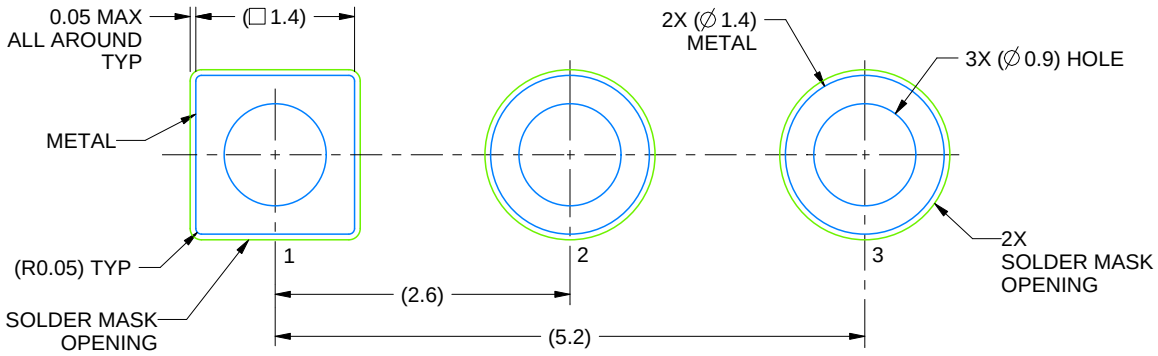


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



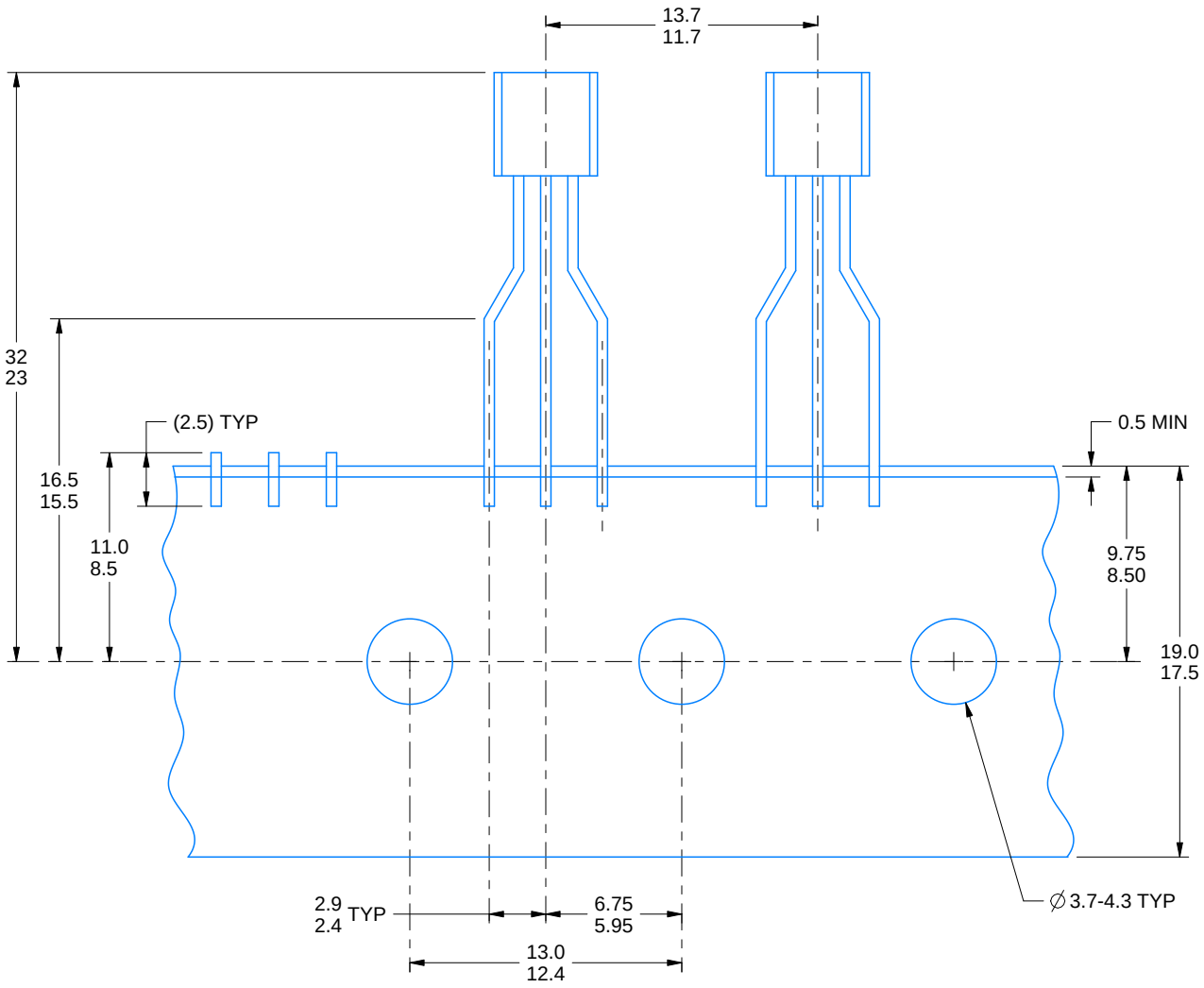
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025

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