

## FCB20N60

### N-Channel SuperFET® MOSFET

600 V, 20 A, 190 mΩ

October 2013



#### Features

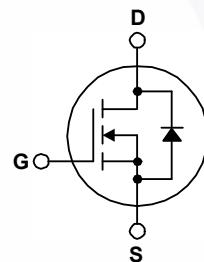
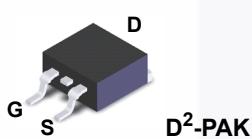
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 150 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 75 \text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss,\text{eff}} = 165 \text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

#### Application

- Lighting
- AC-DC Power Supply
- Solar Inverter

#### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter		FCB20N60TM	Unit
$V_{DSS}$	Drain to Source Voltage		600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	20	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	12.5	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	60.0	A
$V_{GSS}$	Gate to Source Voltage		$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		690	mJ
$I_{AR}$	Avalanche Current (Note 1)		20	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		20.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)		4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )		208	W
		- Derate above $25^\circ\text{C}$	1.67	$W/\text{^\circ C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FCB20N60TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.6	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	$^\circ\text{C/W}$
	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB20N60	FCB20N60TM	D <sup>2</sup> -PAK	330mm	24m	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	$^\circ\text{C}$
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 20 \text{ A}$	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.15	0.19	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 10 \text{ A}$	-	17	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$	-	2370	3080	pF
$C_{oss}$	Output Capacitance		-	1280	1665	pF
$C_{rss}$	Reverse Transfer Capacitance		-	95	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	-	65	85	pF
$C_{osseff.}$	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$	-	165	-	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300 \text{ V}, I_D = 20 \text{ A}$ $R_G = 25 \Omega$	-	62	135	ns
$t_r$	Turn-On Rise Time		-	140	290	ns
$t_{d(off)}$	Turn-Off Delay Time		-	230	470	ns
$t_f$	Turn-Off Fall Time		(Note 4)	65	140	ns
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 480 \text{ V}, I_D = 20 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	75	98	nC
$Q_{gs}$	Gate to Source Gate Charge		-	13.5	18	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	36	-	nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	20	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 20 \text{ A}$	-	-	$1.4 \text{ V}$
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 20 \text{ A}$	-	530	-
$Q_{rr}$	Reverse Recovery Charge	$dl_f/dt = 100 \text{ A}/\mu\text{s}$	-	10.5	$\mu\text{C}$

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 10 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 20 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

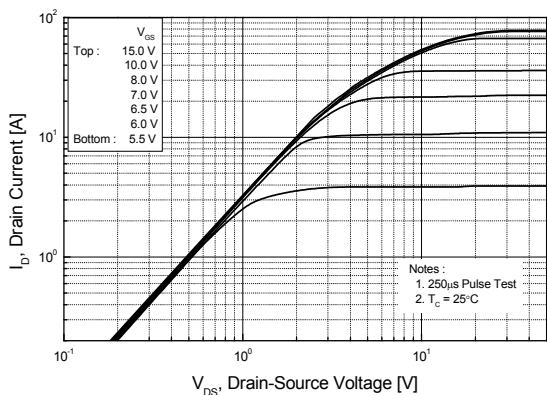


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

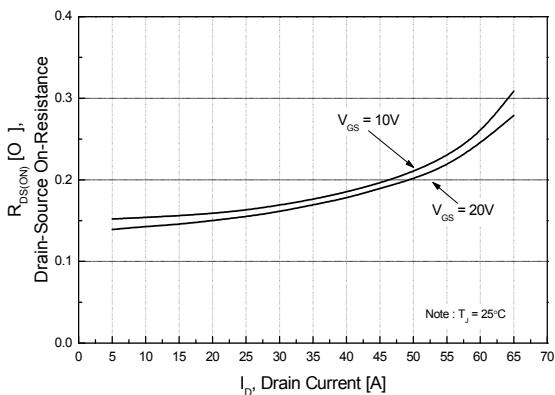


Figure 2. Transfer Characteristics

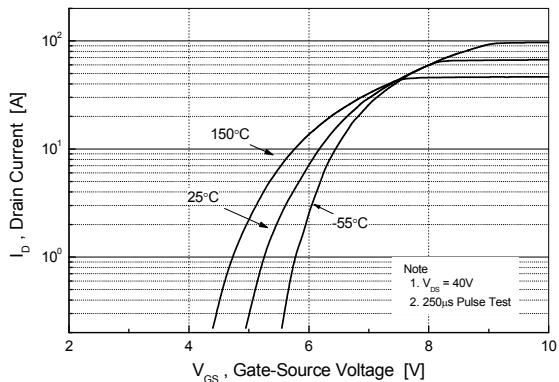


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

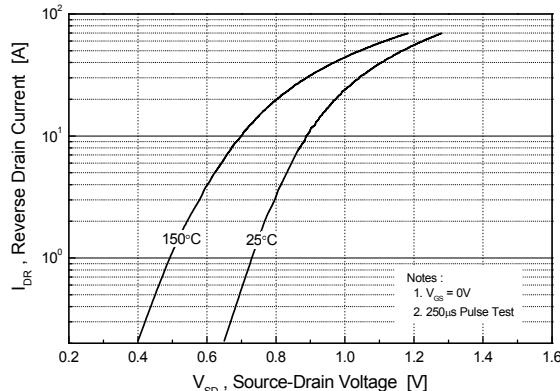


Figure 5. Capacitance Characteristics

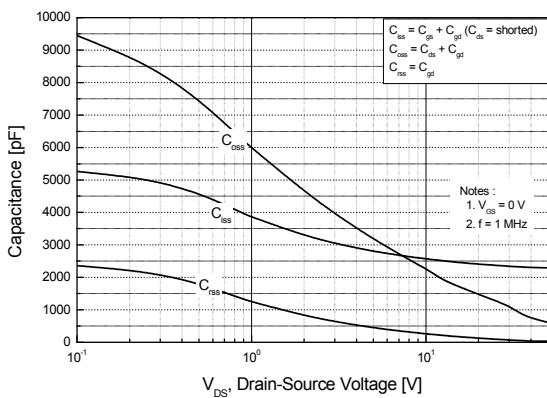
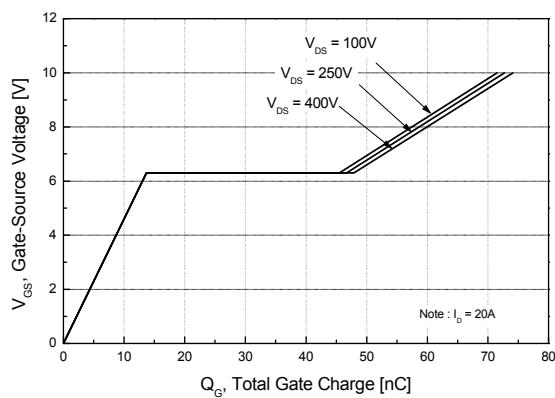
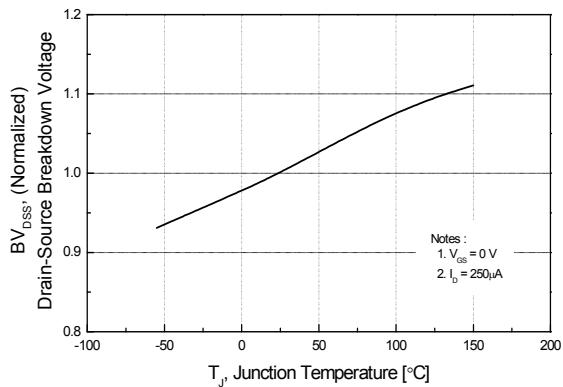


Figure 6. Gate Charge Characteristics

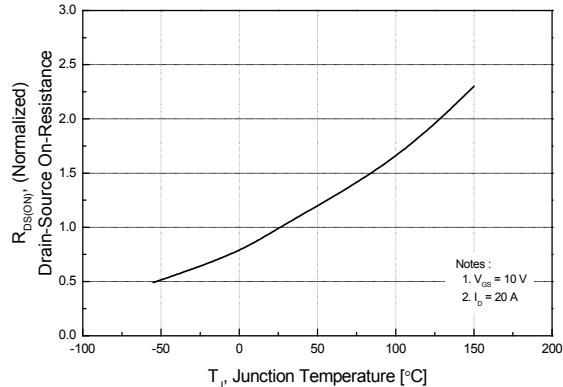


## Typical Performance Characteristics (Continued)

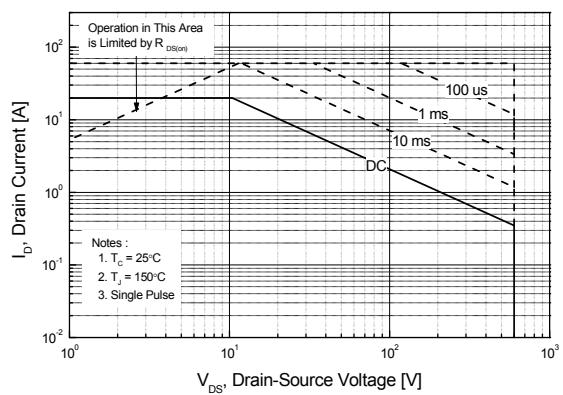
**Figure 7. Breakdown Voltage Variation vs. Temperature**



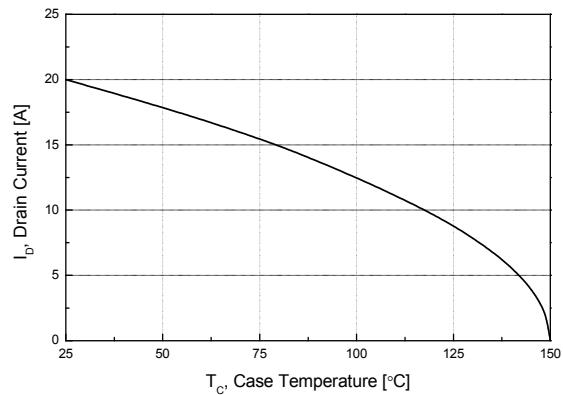
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

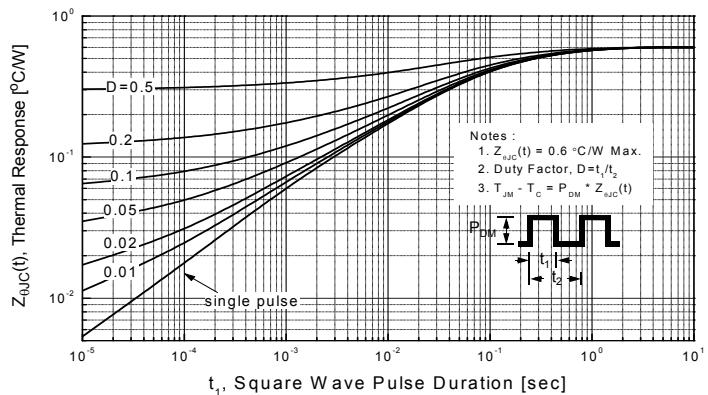


Figure 12. Gate Charge Test Circuit & Waveform

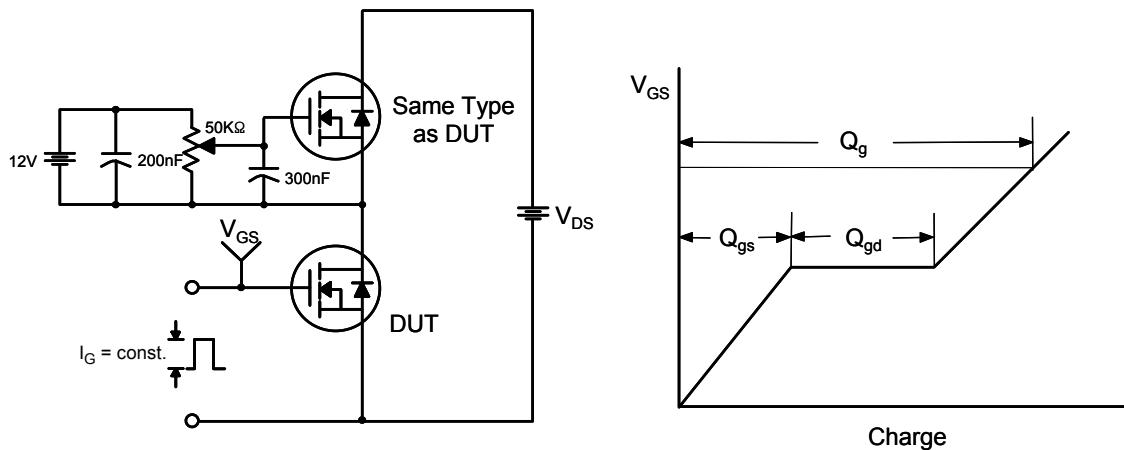


Figure 13. Resistive Switching Test Circuit & Waveforms

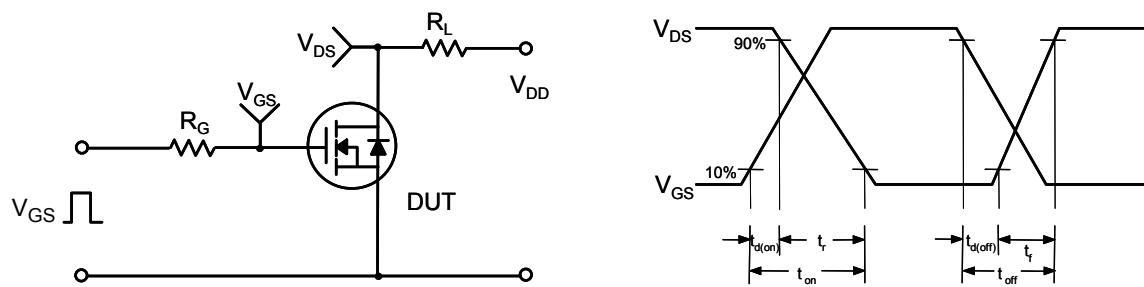


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

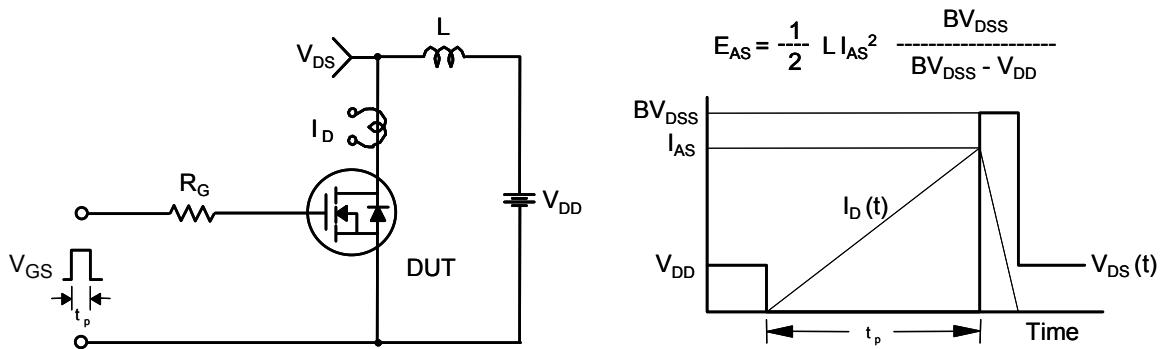
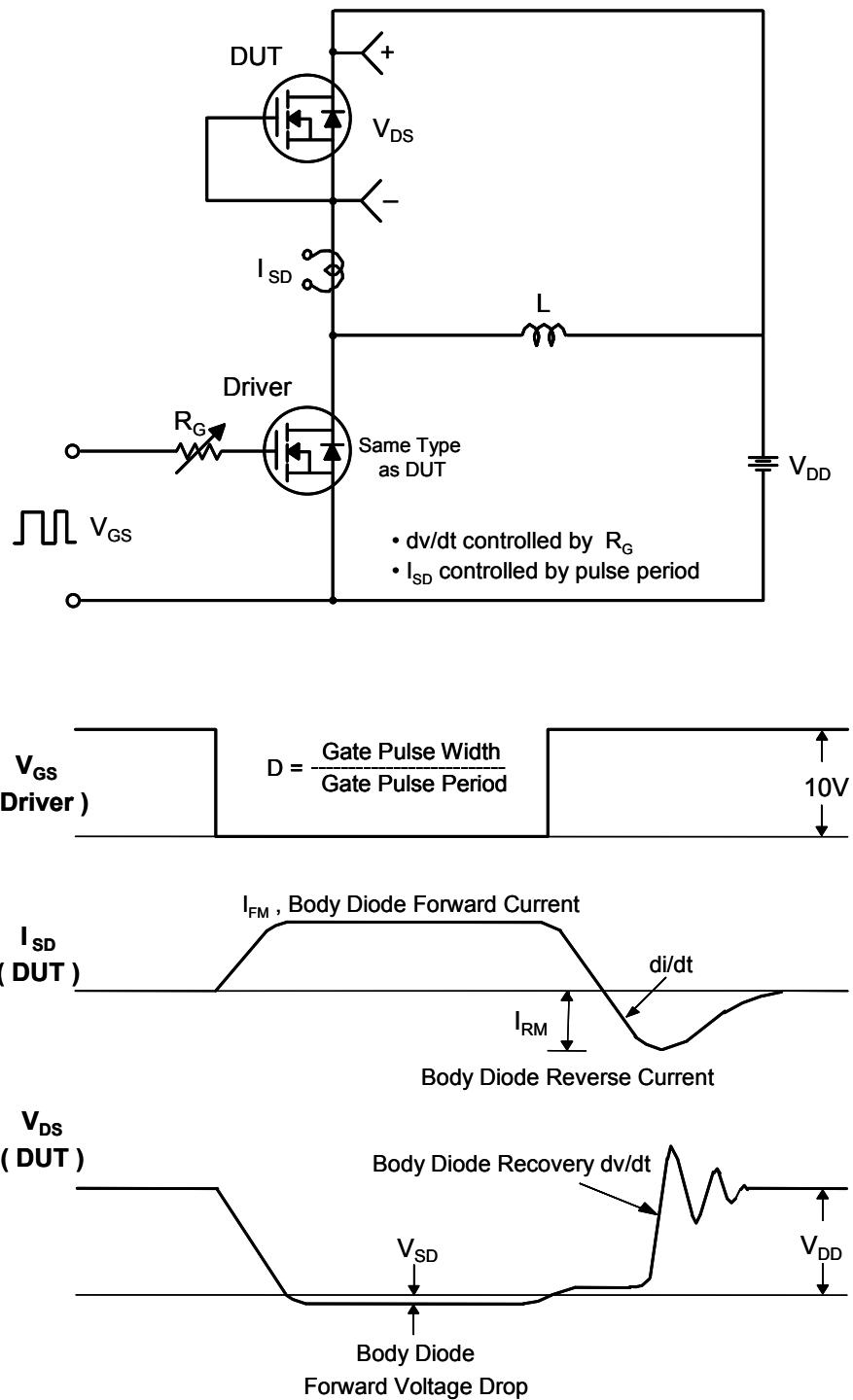


Figure 15. Peak Diode Recovery dv/dt Test Circuit &amp; Waveforms



## Mechanical Dimensions

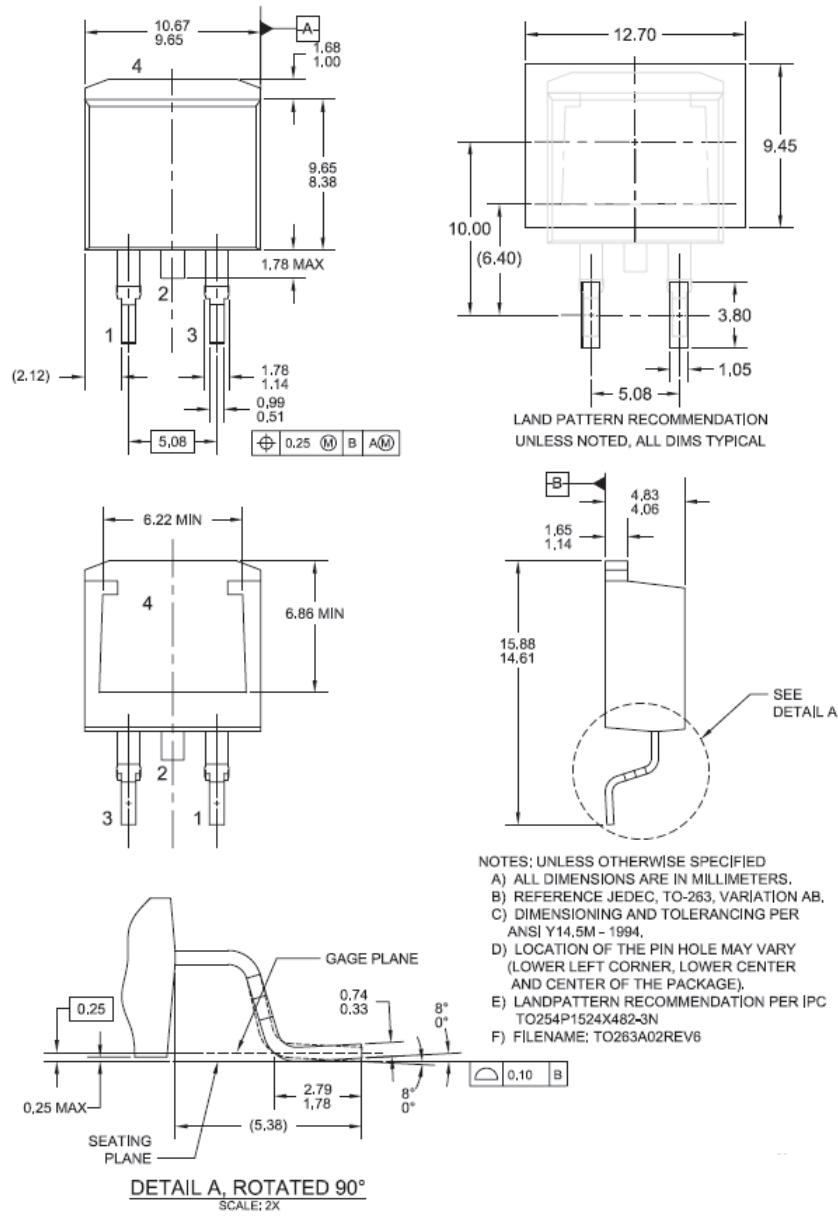
TO-263 2L (D<sup>2</sup>PAK)

Figure 16. 2LD, TO263, Surface Mount

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Dimension in Millimeters



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