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FCH104N60F

N-Channel SuperFET® II FRFET® MOSFET

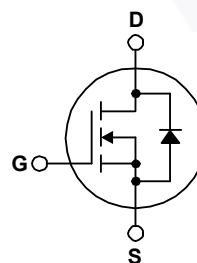
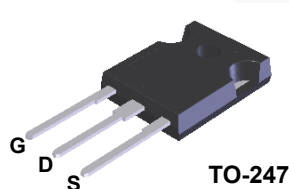
600 V, 37 A, 104 mΩ

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 98\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 107\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 109\text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH104N60F	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC (f > 1 Hz)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	37
		- Continuous ($T_C = 100^\circ\text{C}$)	24
I_{DM}	Drain Current	- Pulsed (Note 1)	111
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	809
I_{AR}	Avalanche Current	(Note 1)	6.8
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.57
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	357
		- Derate Above 25°C	2.85
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCH104N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH104N60F	FCH104N60F	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 25^\circ\text{C}$	600	-	-	V
		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.67	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	16	-	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18.5\text{ A}$	-	98	104	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 18.5\text{ A}$	-	47	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	4475	5950	pF
C_{oss}	Output Capacitance		-	135	180	pF
C_{rss}	Reverse Transfer Capacitance		-	1.5	2.5	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	75	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	109	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	107	139	nC
Q_{gs}	Gate to Source Gate Charge		-	25	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	44	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.87	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$ (Note 4)	-	34	78	ns
t_r	Turn-On Rise Time		-	24	58	ns
$t_{d(off)}$	Turn-Off Delay Time		-	98	206	ns
t_f	Turn-Off Fall Time		-	5	20	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	37	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	111	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 18.5 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 18.5 A,	-	144	-	ns
Q _{rr}	Reverse Recovery Charge	di _F /dt = 100 A/μs	-	0.91	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 6.8\text{ A}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 18.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

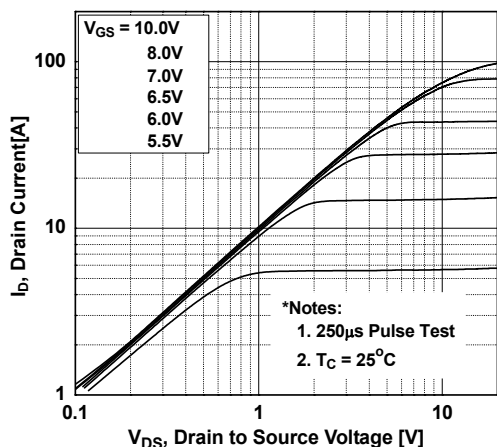


Figure 2. Transfer Characteristics

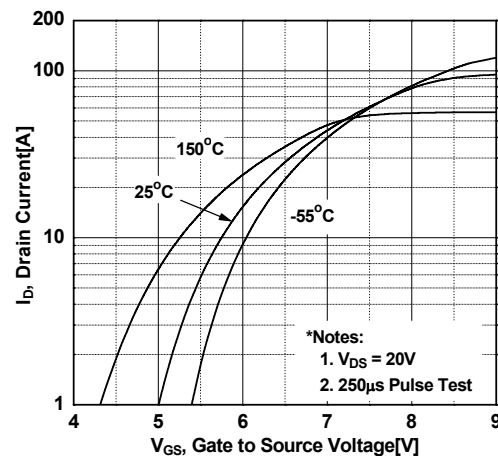


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

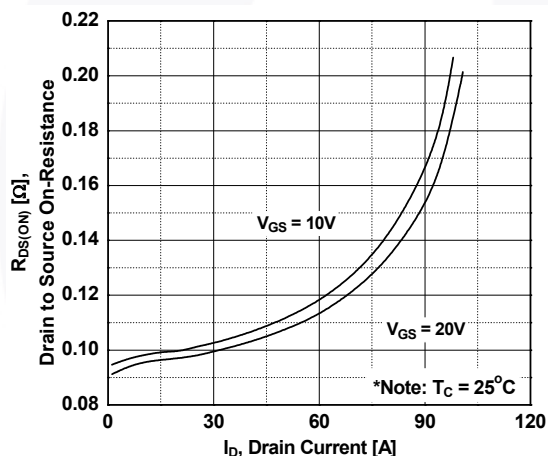


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

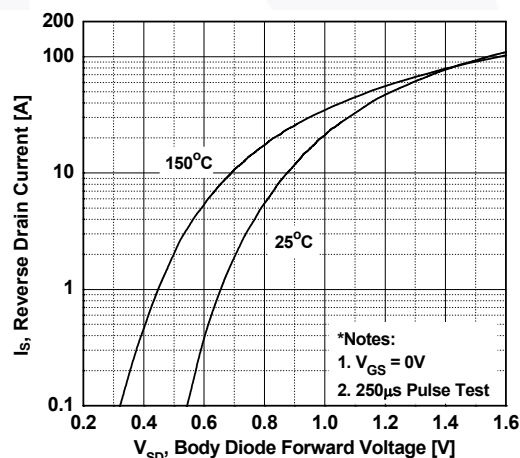


Figure 5. Capacitance Characteristics

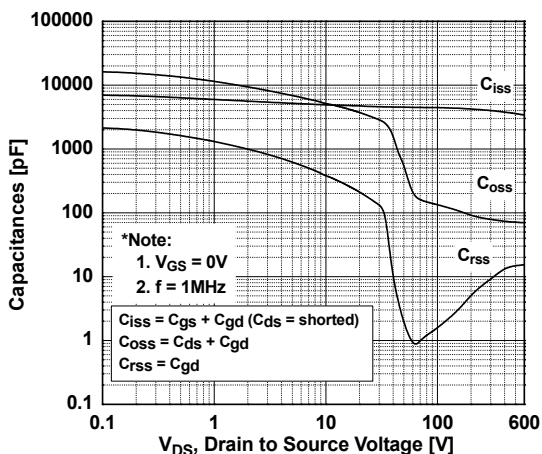
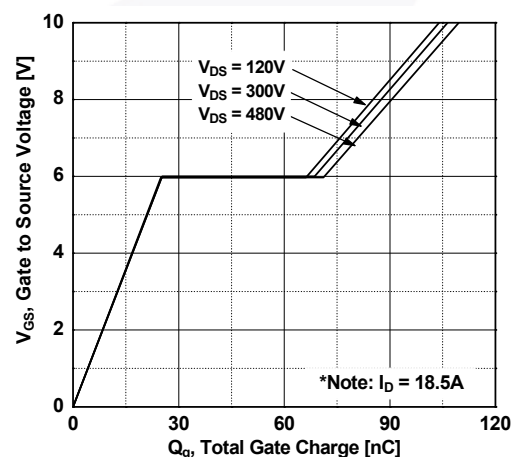


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

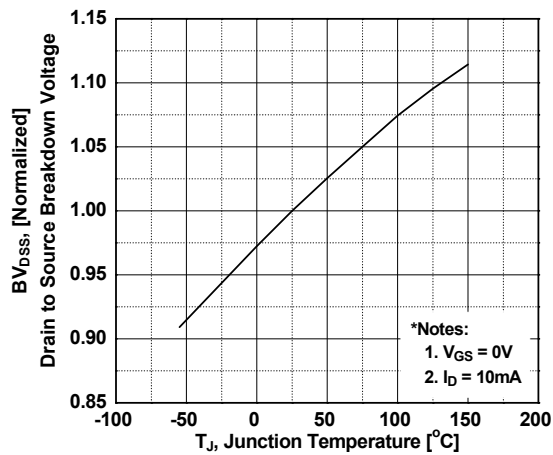


Figure 8. On-Resistance Variation vs. Temperature

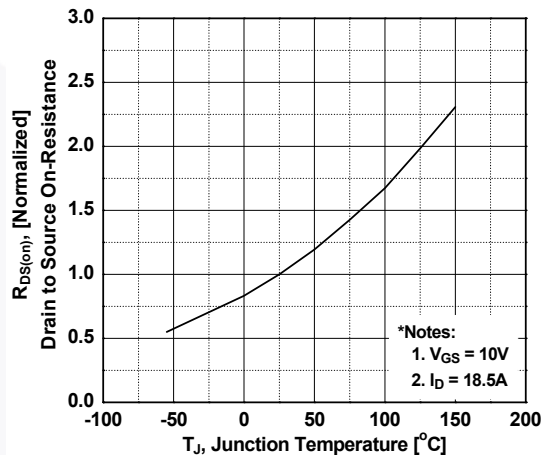


Figure 9. Maximum Safe Operating Area

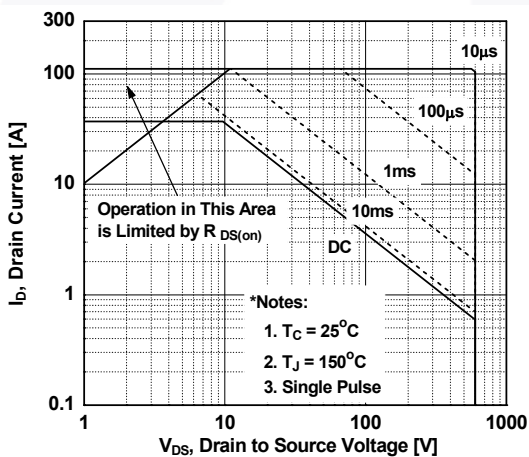


Figure 10. Maximum Drain Current vs. Case Temperature

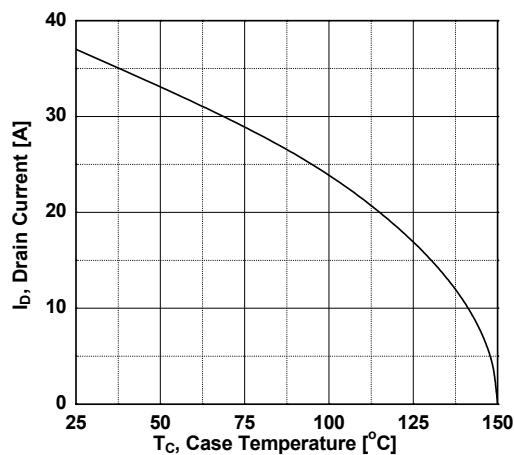
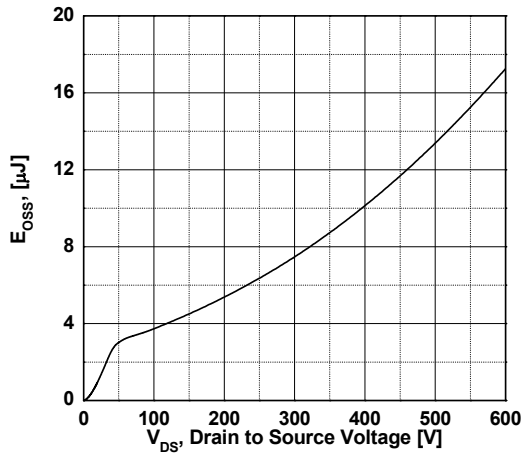
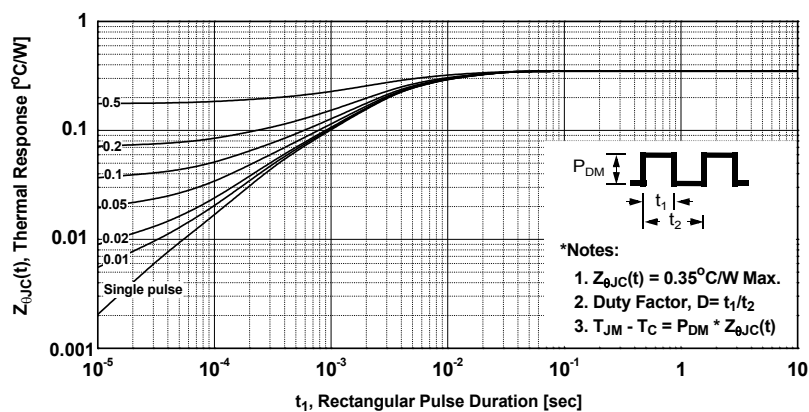


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



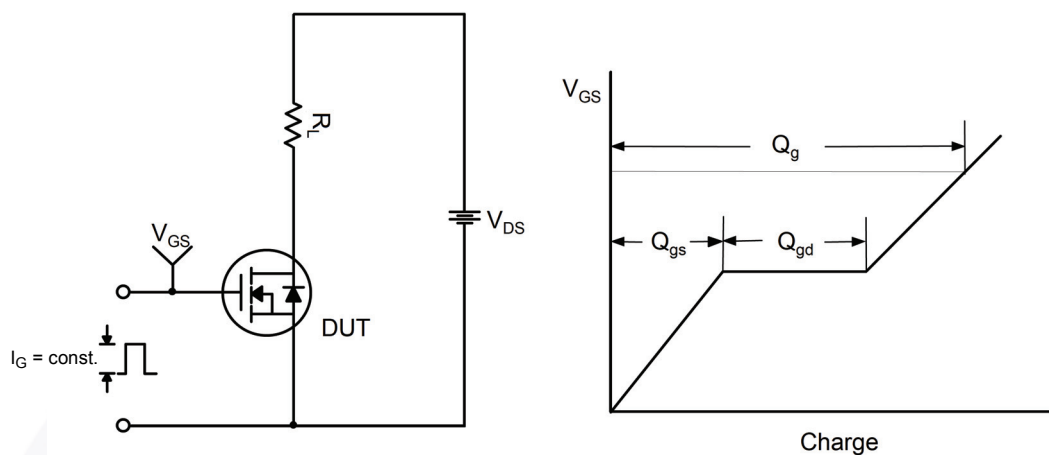


Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

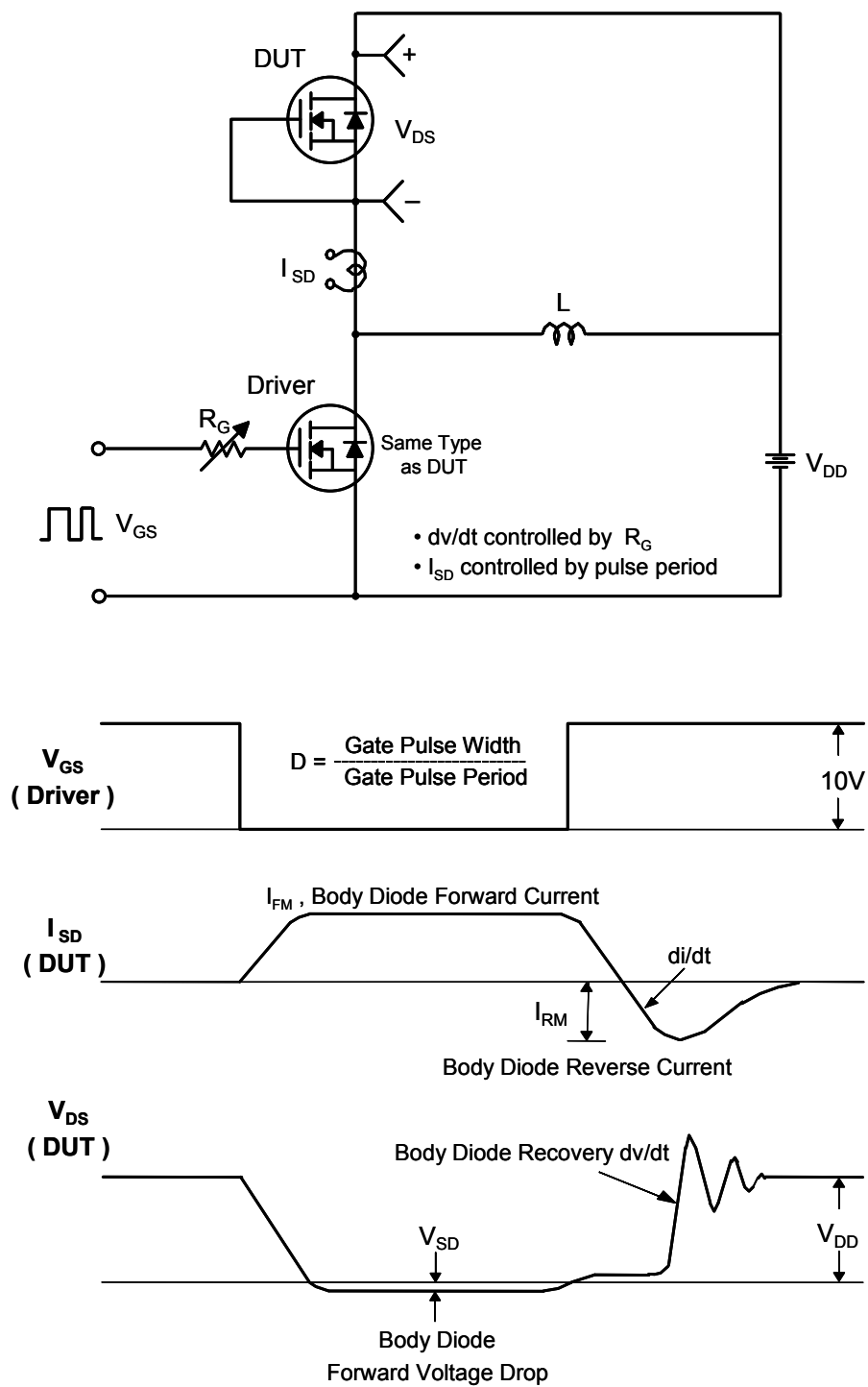
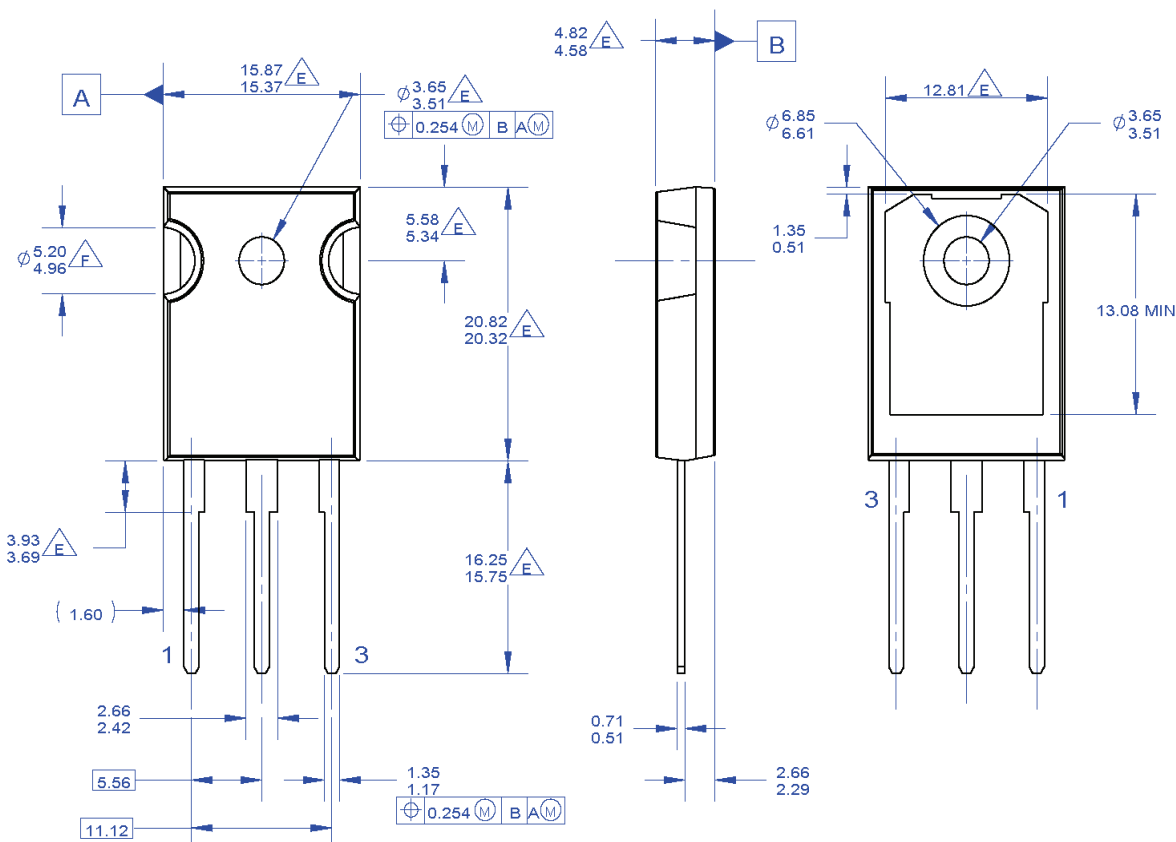


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



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- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$ DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$ NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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