

MOSFET – POWERTRENCH® N-Channel

100 V, 240 A, 4.1 mΩ

FDBL86066-F085

Features

- Typical $R_{DS(on)}$ = 3.3 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 47 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

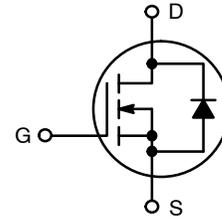
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous, ($V_{GS} = 10$ V) $T_C = 25^\circ\text{C}$ (Note 1)	185	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	(See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	93.6	mJ
P_D	Power Dissipation	300	W
	Derate Above 25°C	2	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

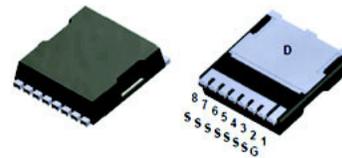
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting $T_J = 25^\circ\text{C}$, $L = 30 \mu\text{H}$, $I_{AS} = -79$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	4.1 mΩ @ 10 V	240 A

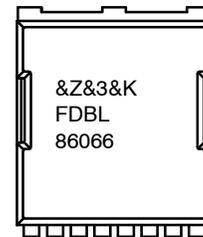


N-CHANNEL MOSFET



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDBL86066 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	43	

3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$ (Note 4)	–	–	1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2	2.9	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}$ $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$ (Note 4)	–	3.3	4.1	m Ω
			–	7.3	8.8	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	3240	–	pF
C_{oss}	Output Capacitance		–	1950	–	pF
C_{rss}	Reverse Transfer Capacitance		–	26	–	pF
R_g	Gate Resistance	$V_{GS} = 0.5 \text{ V}, f = 1 \text{ MHz}$	–	0.5	–	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 80 \text{ A}$	–	47	69	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ V to } 2 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 80 \text{ A}$	–	6	–	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 50 \text{ V}, I_D = 80 \text{ A}$	–	15	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	$V_{DD} = 50 \text{ V}, I_D = 80 \text{ A}$	–	10	–	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 50 \text{ V}, I_D = 80 \text{ A}, V_{GS} = 10 \text{ V},$ $R_{GEN} = 6 \Omega$	–	–	35	ns
$t_{d(on)}$	Turn-On Delay		–	18	–	ns
t_r	Rise Time		–	9	–	ns
$t_{d(off)}$	Turn-Off Delay		–	36	–	ns
t_f	Fall Time		–	13	–	ns
t_{off}	Turn-Off Time		–	–	68	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$I_{SD} = 80 \text{ A}, V_{GS} = 0 \text{ V}$	–	0.9	1.25	V
		$I_{SD} = 40 \text{ A}, V_{GS} = 0 \text{ V}$	–	0.85	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 80 \text{ A}, di_{SD}/dt = 300 \text{ A}/\mu\text{s}$	–	36	54	ns
Q_{rr}	Reverse Recovery Charge		–	84	126	nC
t_{rr}	Reverse Recovery Time	$I_F = 80 \text{ A}, di_{SD}/dt = 1000 \text{ A}/\mu\text{s}$	–	32	48	ns
Q_{rr}	Reverse Recovery Charge		–	243	365	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

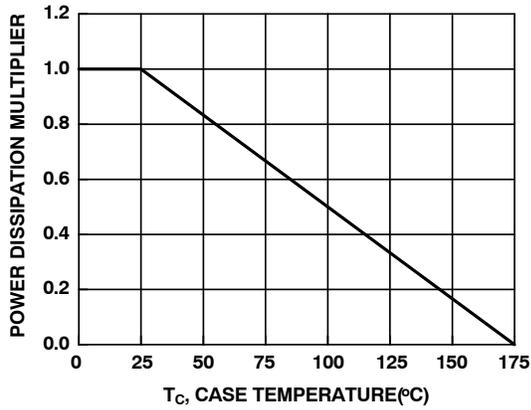


Figure 1. Normalized Power Dissipation vs. Case Temperature

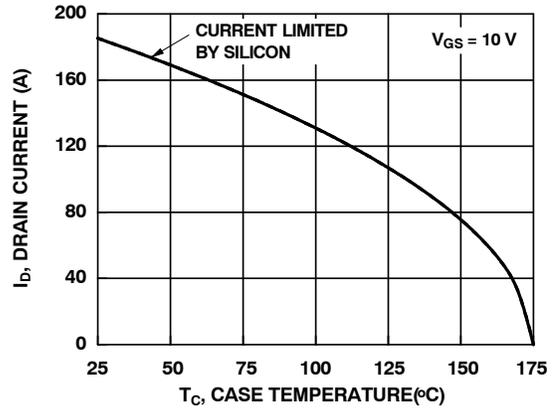


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

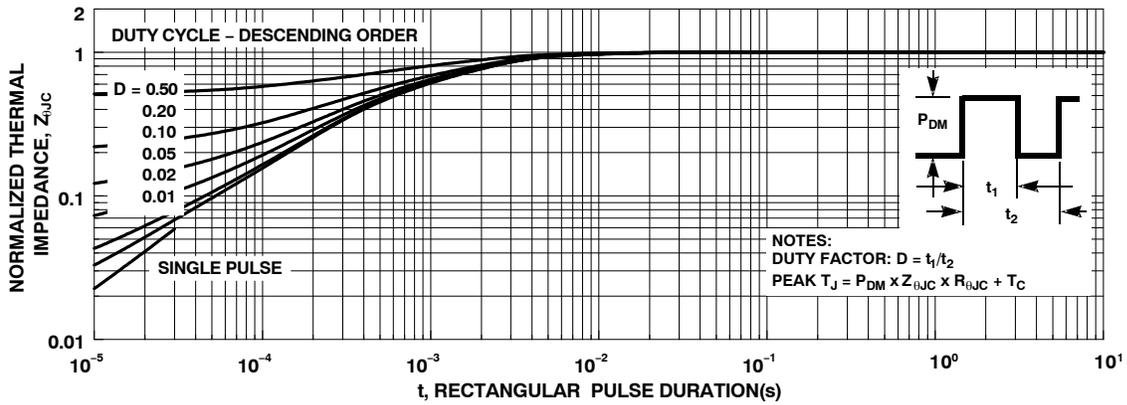


Figure 3. Normalized Maximum Transient Thermal Impedance

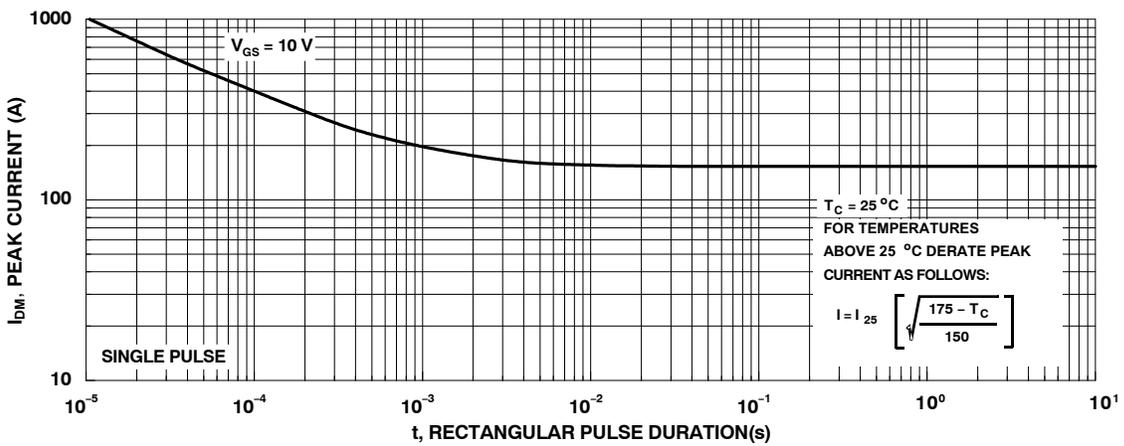


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

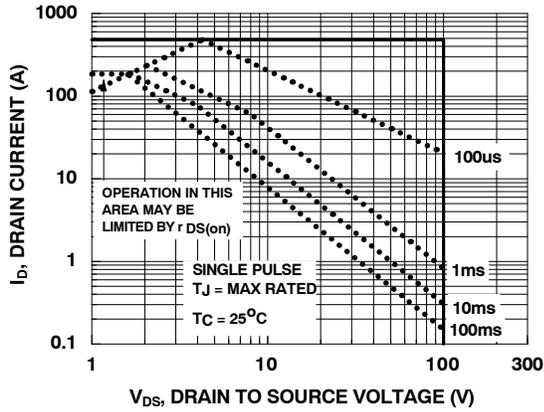


Figure 5. Forward Bias Safe Operating Area

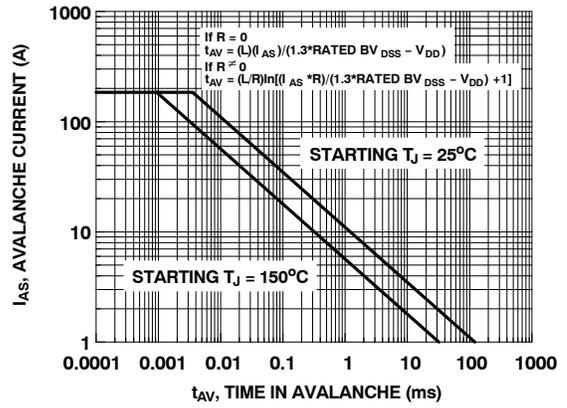


Figure 6. Unclamped Inductive Switching Capability

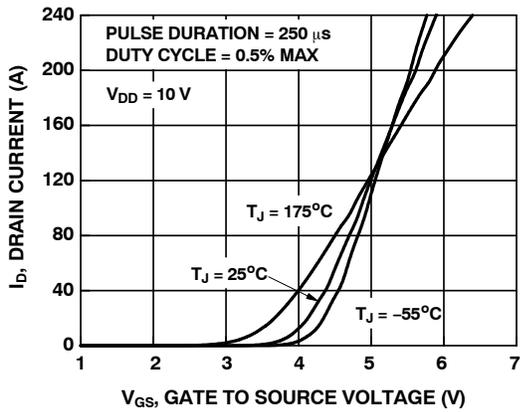


Figure 7. Transfer Characteristics

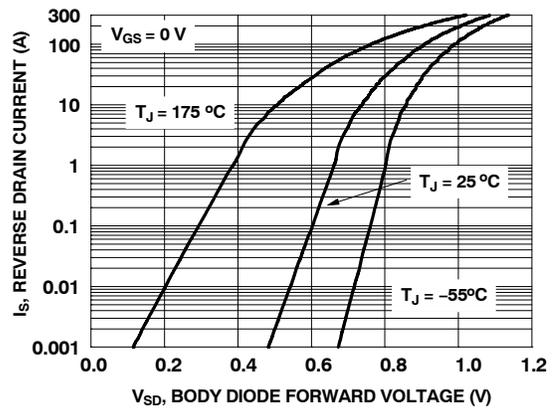


Figure 8. Forward Diode Characteristics

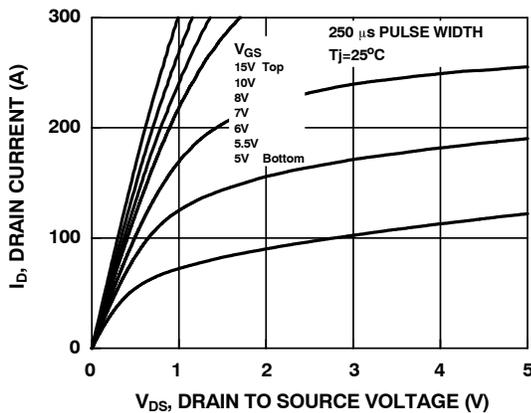


Figure 9. Saturation Characteristics

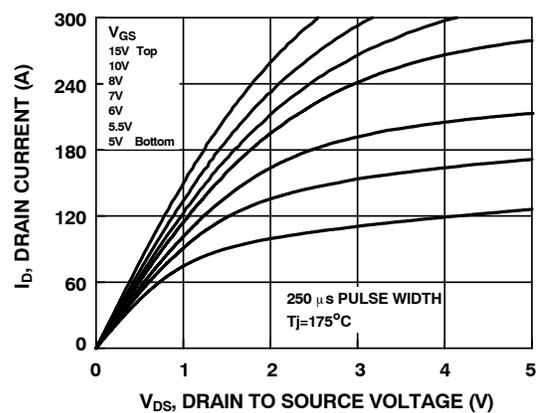


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

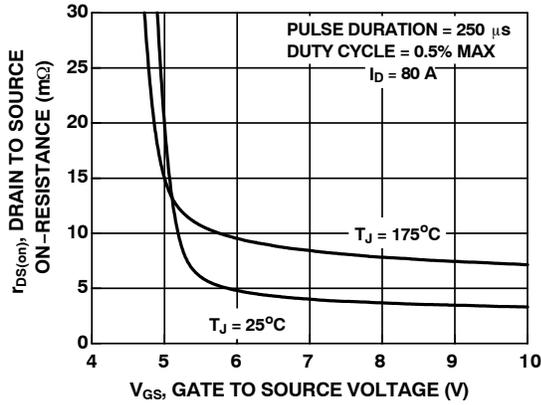


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

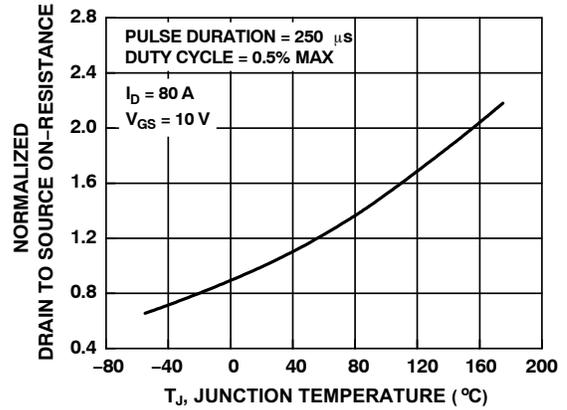


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

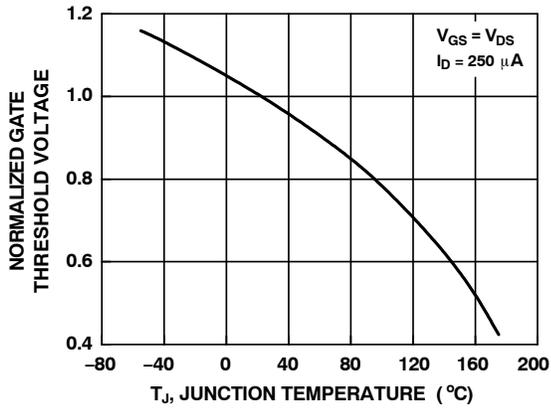


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

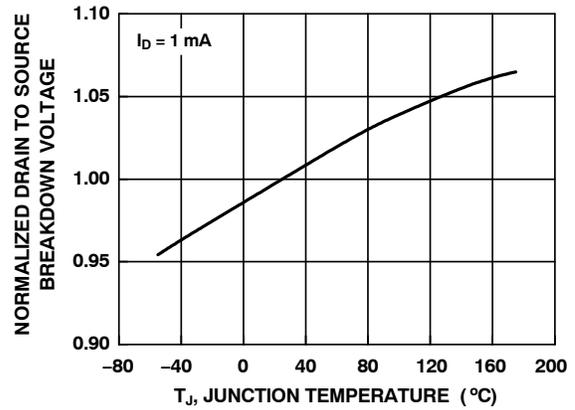


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

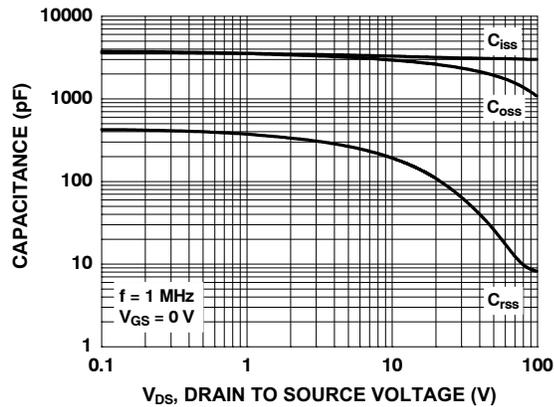


Figure 15. Capacitance vs. Drain to Source Voltage

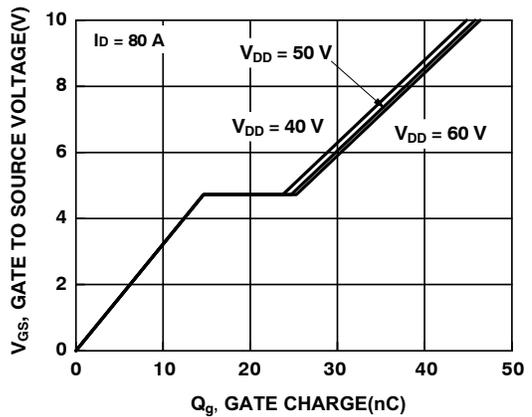


Figure 16. Gate Charge vs. Gate to Source Voltage

FDBL86066–F085

PACKAGE MARKING AND ORDERING INFORMATION

Device	Marking	Package	Shipping†
FDBL86066–F085	FDBL86066	H–PSOF8L (Pb-Free / Halogen Free)	2000 Units / Tape & Reel

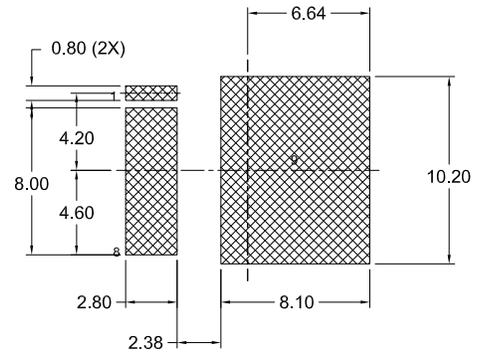
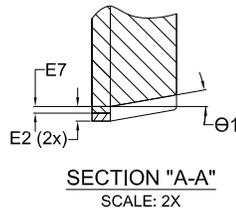
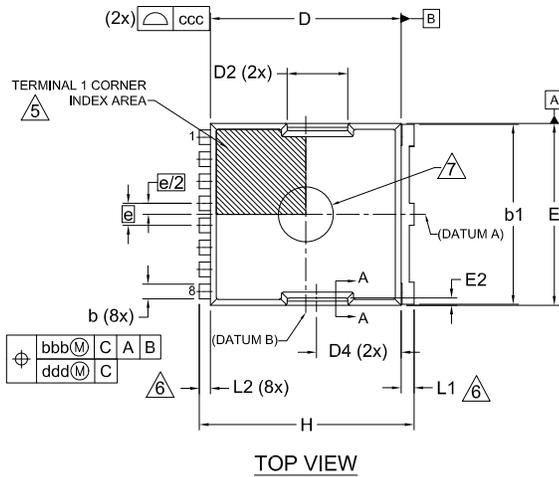
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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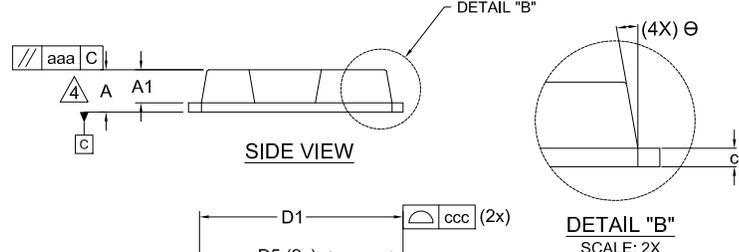


H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

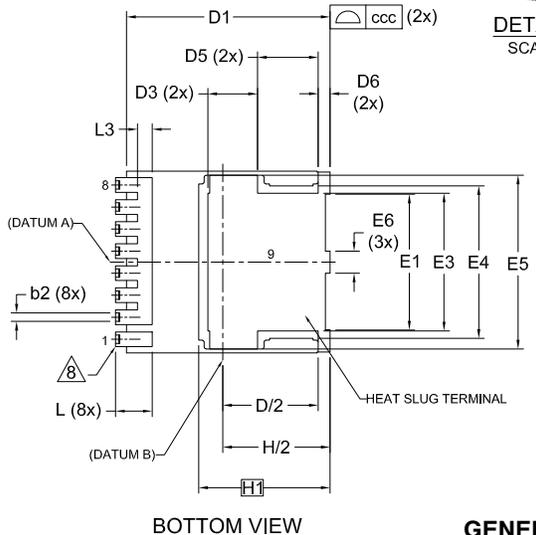
DATE 30 JUL 2024



LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 3. "e" REPRESENTS THE TERMINAL PITCH.
 4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
 5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
 6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
 7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
 8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

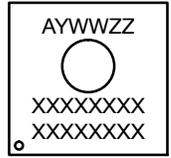


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	10° REF		
theta 1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*

- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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