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September 2015



# FL73282

## Half-Bridge Gate Driver

### Features

- Floating Channel for Bootstrap Operation to +900 V
- Typically 350 mA / 650 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative  $V_S$  Swing to -9.8 V for Signal Propagation at  $V_{CC}=V_{BS}=15$  V
- $V_{CC}$  &  $V_{BS}$  Supply Range from 10 V to 20 V
- UVLO Functions for Both Channels
- Matched Propagation Delay Below 50 ns
- Built-in 170 ns Dead-Time
- Output in Phase with Input Signal

### Applications

- Fluorescent Lamp Ballast
- HID Ballast
- SMPS
- Motor Driver
- General Purpose Half Bridge Topology

### Description

The FL73282, a monolithic half bridge gate-drive IC, can drive MOSFETs and IGBTs that operate up to +900 V. Fairchild's high-voltage process and common mode noise canceling technique provides stable operation of the high-side driver under high-d $V_S$ /dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to  $V_S=-9.8$  V (typical) for  $V_{BS}=15$  V. The UVLO circuits for both channels prevent malfunction when  $V_{CC}$  or  $V_{BS}$  is lower than the specified threshold voltage. Output drivers typically source/sink 350 mA / 650 mA, respectively, which is suitable for all kinds of half- and full-bridge inverters.



Figure 1. SOP 8

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FL73282MX <sup>(1)</sup>	-40°C to +125°C	8-Lead, Small Outline Integrated Circuit, (SOIC)	Tape & Reel

#### Note:

1. These devices passed wave-soldering test by JESD22A-111.

## Typical Application Diagram

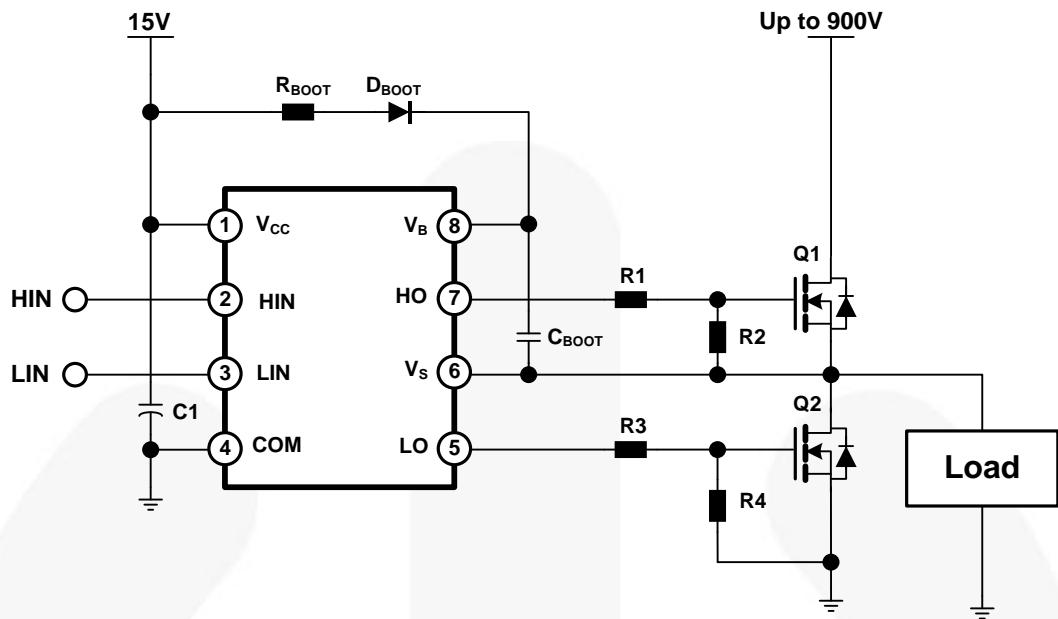


Figure 2. Application Circuit for Half Bridge Topology

## Internal Block Diagram

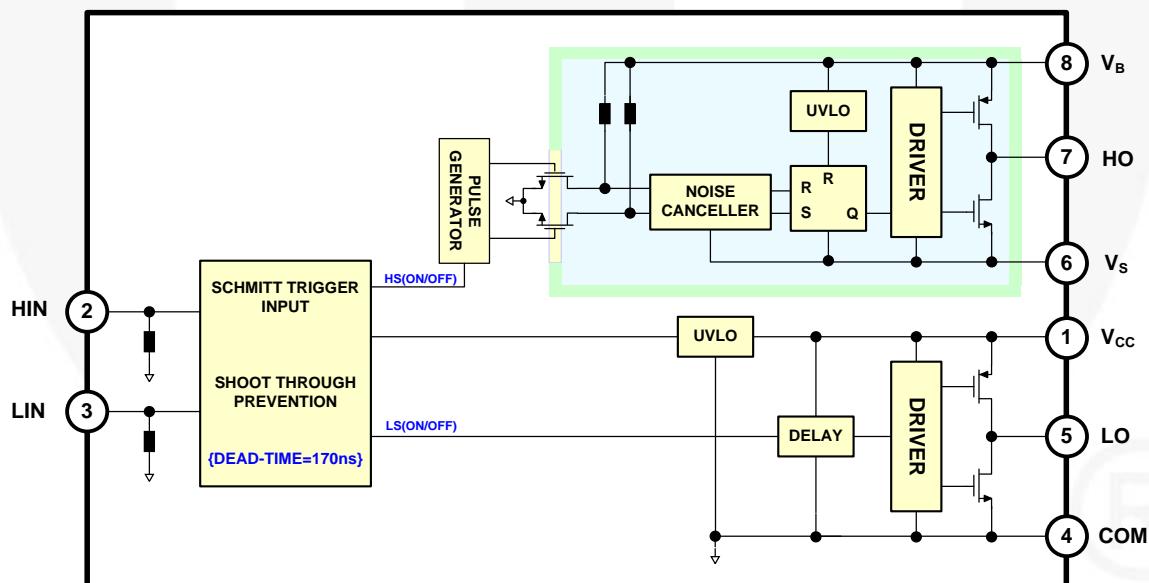


Figure 3. Functional Block Diagram

## Pin Configuration

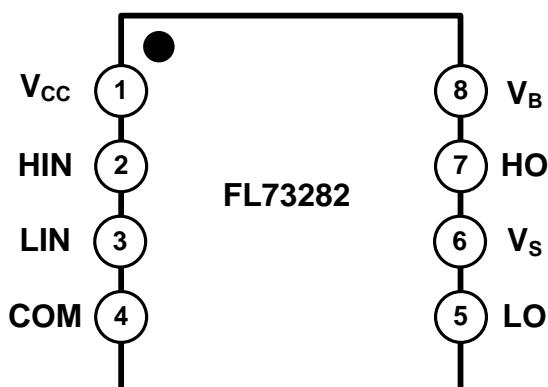


Figure 4. Pin Assignments (Top View)

## Pin Definitions

Pin	Name	I/O	Description
1	V <sub>CC</sub>	I	Low-Side Supply Voltage
2	HIN	I	Logic Input for High-Side Gate Driver Output
3	LIN	I	Logic Input for Low-Side Gate Driver Output
4	COM		Logic Ground and Low-Side Driver Return
5	LO	O	Low-Side Driver Output
6	V <sub>S</sub>	I	High-Voltage Floating Supply Return
7	HO	O	High-Side Driver Output
8	V <sub>B</sub>	I	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_S$	High-Side Floating Offset Voltage	$V_B-24$	$V_B+0.3$	V
$V_B$	High-Side Floating Supply Voltage	-0.3	924.0	V
$V_{CC}$	Low-Side and Logic-Fixed Supply Voltage	-0.3	24	V
$V_{HO}$	High-Side Floating Output Voltage $V_{HO}$	$V_S-0.3$	$V_B+0.3$	V
$V_{LO}$	Low-Side Floating Output Voltage $V_{LO}$	-0.3	$V_{CC}+0.3$	V
$V_{IN}$	Logic Input Voltage (HIN, LIN)	-0.3	$V_{CC}+0.3$	V
COM	Logic Ground	$V_{CC}-24$	$V_{CC}+0.3$	V
$dV_S/dt$	Allowable Offset Voltage Slew Rate		$\pm 50$	V/ns
$P_D^{(3)(4)(5)}$	Power Dissipation		0.625	W
$\theta_{JA}$	Thermal Resistance		200	°C/W
$T_J$	Junction Temperature		150	°C
$T_{STG}$	Storage Temperature	-55	150	°C

### Notes:

2. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
3. Refer to the following standards:  
*JESD51-2: Integral circuit's thermal test method environmental conditions, natural convection;*  
*JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.*
4. Do not exceed maximum power dissipation ( $P_D$ ) under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S+10$	$V_S+20$	V
$V_S$	High-Side Floating Supply Offset Voltage	$6-V_{CC}$	900	V
$V_{HO}$	High-Side (HO) Output Voltage	$V_S$	$V_B$	V
$V_{LO}$	Low-Side (LO) Output Voltage	COM	$V_{CC}$	V
$V_{IN}$	Logic Input Voltage (HIN, LIN)	COM	$V_{CC}$	V
$V_{CC}$	Low-Side Supply Voltage	10	20	V
$T_A$	Ambient Temperature	-40	+125	°C

## Static Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}) = 15.0$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S$  and COM and are applicable to the respective outputs HO and LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Power Supply Section</b>						
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	$V_{IN}=0$ V or 5 V		80	180	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN}=0$ V or 5 V		50	120	$\mu\text{A}$
$I_{PCC}$	Operating $V_{CC}$ Supply Current	$f_{IN}=20$ kHz, rms value			550	$\mu\text{A}$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$f_{IN}=20$ kHz, rms value			600	$\mu\text{A}$
$I_{LK}$	Offset Supply Leakage Current	$V_B=V_S=900$ V			10	$\mu\text{A}$
<b>Bootstrapped Supply Section</b>						
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ & $V_{BS}$ Supply Under-Voltage Positive going Threshold		8.2	9.2	10.0	V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ & $V_{BS}$ Supply Under-Voltage Negative going Threshold		7.6	8.7	9.6	V
$V_{CCUVH}$ $V_{BSUVH}$	$V_{CC}$ Supply Under-Voltage Lockout Hysteresis			0.5		V
<b>Input Section</b>						
$V_{IH}$	Logic "1" Input Voltage		2.5			V
$V_{IL}$	Logic "0" Input Voltage				0.8	V
$I_{IN+}$	Logic "1" Input Bias Current	$V_{IN}=5$ V		20	50	$\mu\text{A}$
$I_{IN-}$	Logic "0" Input Bias Current	$V_{IN}=0$ V		1.0	2.0	$\mu\text{A}$
$R_{IN}$	Logic Input Pull-Down Resistance		100	250		$\text{k}\Omega$
<b>Gate Driver Output Section</b>						
$V_{OH}$	High-Level Output Voltage, $V_{BIAS}-V_O$	$I_O=0$ A			85	mV
$V_{OL}$	Low-Level Output Voltage, $V_O$	$I_O=0$ A			85	mV
$I_{O+}$	Output HIGH Short-Circuit Pulsed Current	$V_O=0$ V, $V_{IN}=5$ V with $PW \leq 10$ $\mu\text{s}$	250	350		mA
$I_{O-}$	Output LOW Short-Circuit Pulsed Current	$V_O=15$ V, $V_{IN}=0$ V with $PW \leq 10$ $\mu\text{s}$	500	650		mA
$V_S$	Allowable Negative $V_S$ Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V

## Dynamic Electrical Characteristics

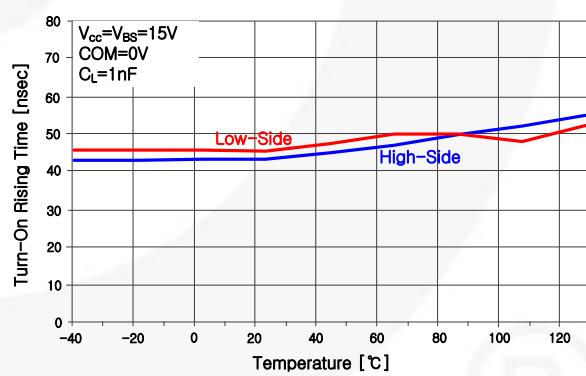
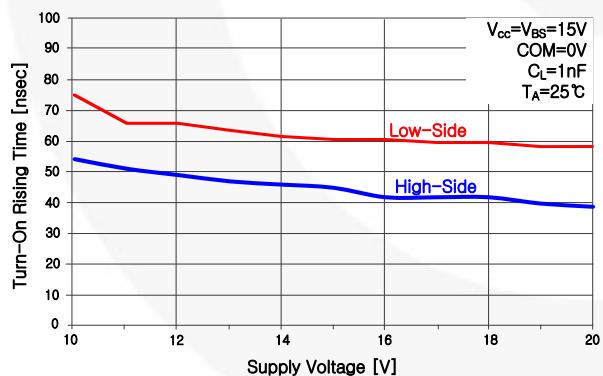
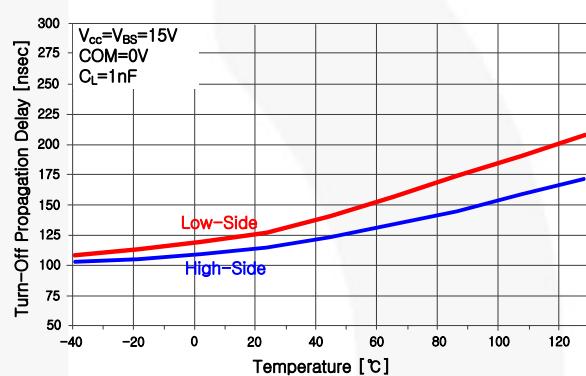
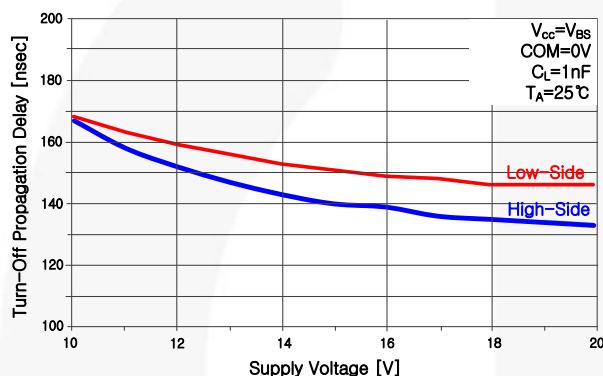
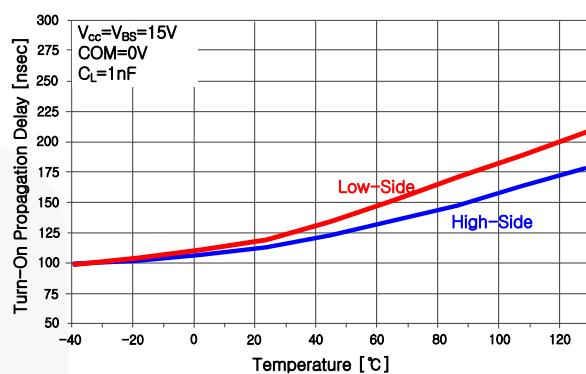
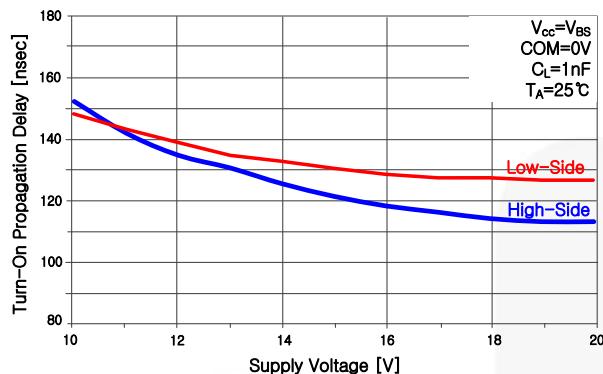
$V_{BIAS}(V_{CC}, V_{BS}) = 15.0$  V,  $V_S = \text{COM}$ ,  $C_L = 1000$  pF and  $T_A = 25^\circ\text{C}$ , unless otherwise specified..

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{ON}$	Turn-On Propagation Delay	$V_S=0$ V	80	150	220	ns
$t_{OFF}$	Turn-Off Propagation Delay	$V_S=0$ V or $900$ V <sup>(5)</sup>	80	150	220	ns
$t_R$	Turn-On Rise Time	$V_{LIN}=V_{HIN}=5$ V		60	140	ns
$t_F$	Turn-Off Fall Time	$V_{LIN}=V_{HIN}=0$ V		30	80	ns
DT	Dead Time		70	170	270	ns
MT	Delay Matching, HS & LS Turn-on/off				50	ns
$t_{PW}$	Minimum Input Pulse Width that changes the Output <sup>(5)(6)</sup>				220	ns

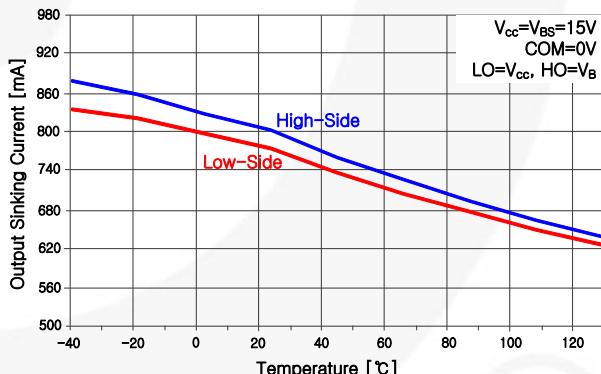
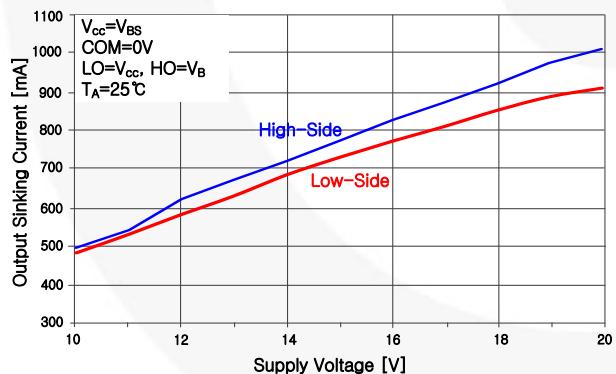
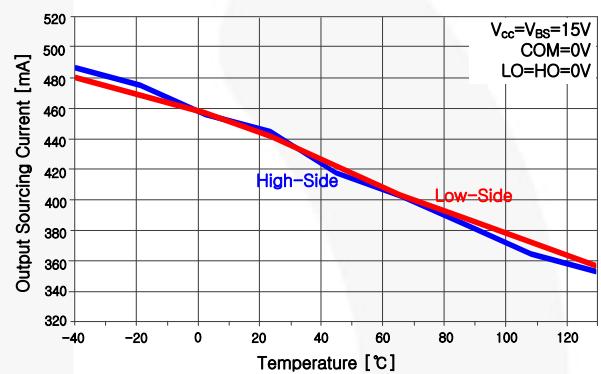
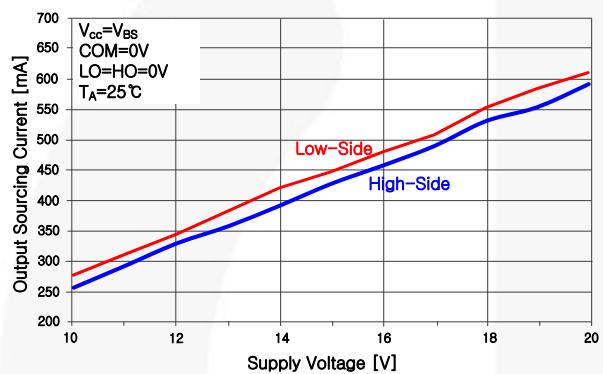
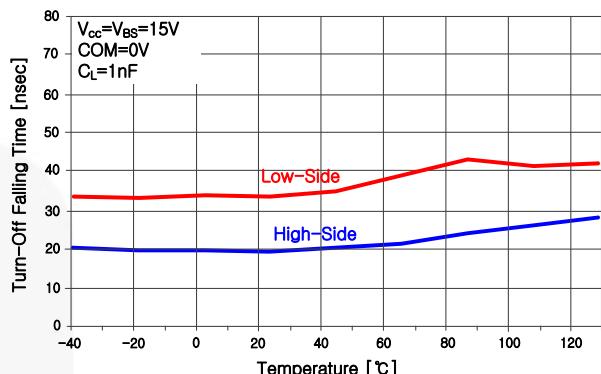
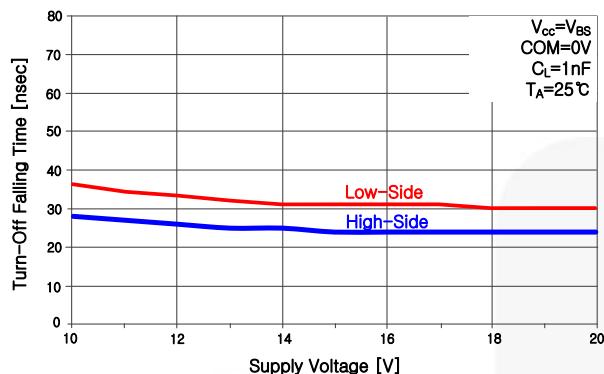
**Notes:**

5. These parameters are guaranteed by design.
6. The minimum input pulse width time included dead time

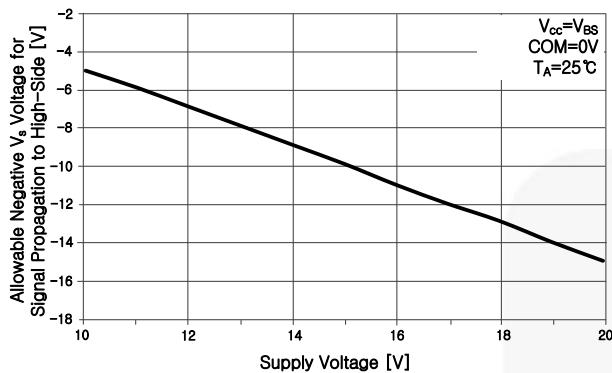
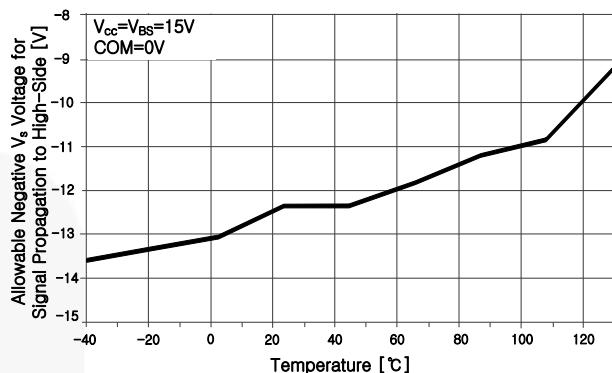
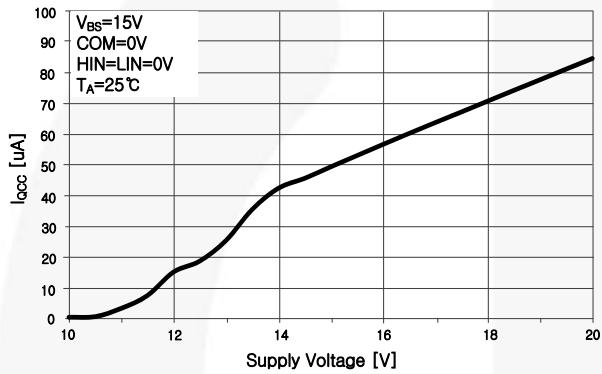
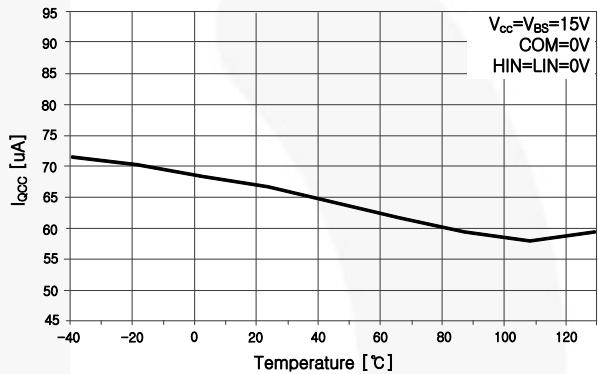
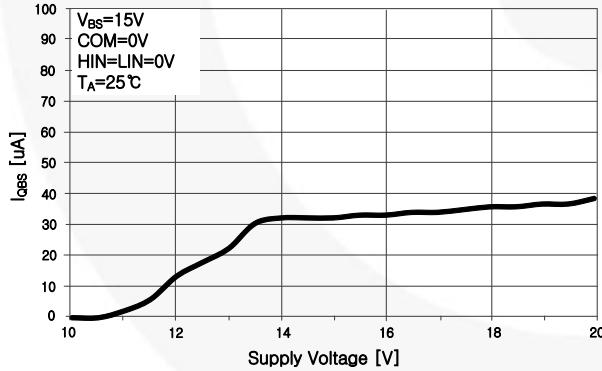
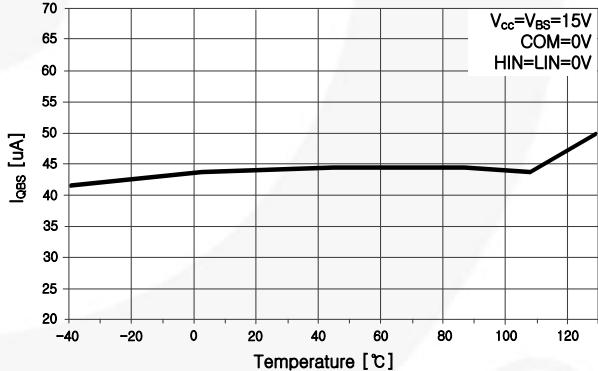
## Typical Characteristics



## Typical Characteristics (Continued)



## Typical Characteristics (Continued)

Figure 17. Allowable Negative  $V_s$  Voltage for Signal Propagation to High Side vs. Supply VoltageFigure 18. Allowable Negative  $V_s$  Voltage for Signal Propagation to High Side vs. TemperatureFigure 19.  $I_{QCC}$  vs. Supply VoltageFigure 20.  $I_{QCC}$  vs. TemperatureFigure 21.  $I_{QBS}$  vs. Supply VoltageFigure 22.  $I_{QBS}$  vs. Temperature

## Typical Characteristics (Continued)

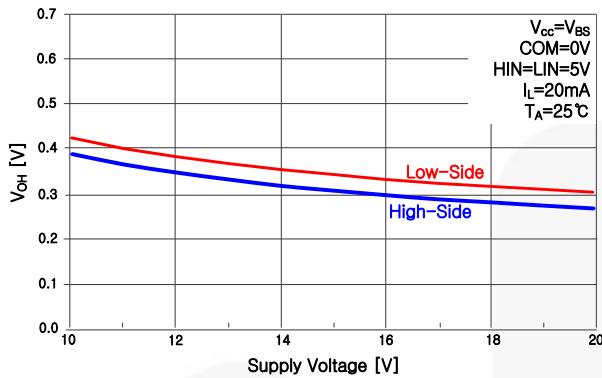


Figure 23. High-Level Output Voltage vs. Supply Voltage

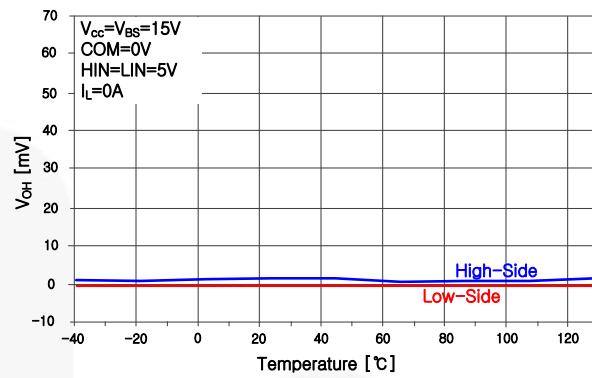


Figure 24. High-Level Output Voltage vs. Temperature

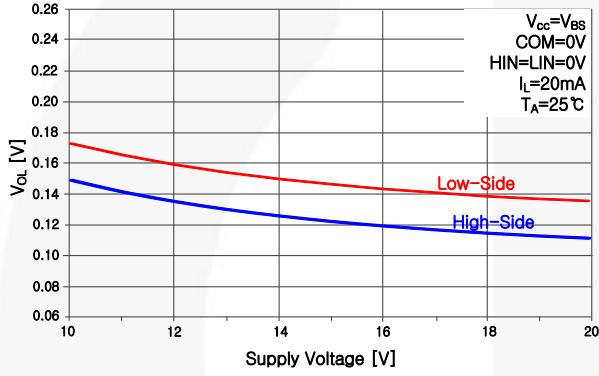


Figure 25. Low-Level Output Voltage vs. Supply Voltage

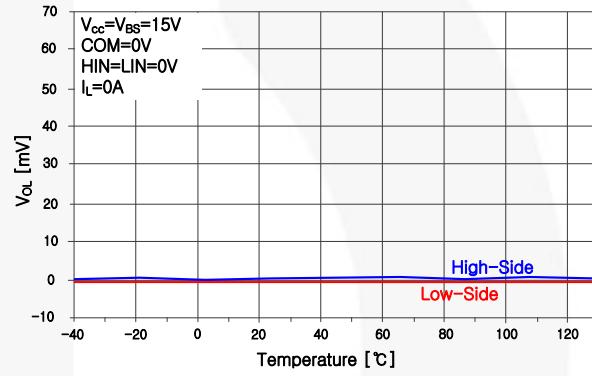


Figure 26. Low-Level Output Voltage vs. Temperature

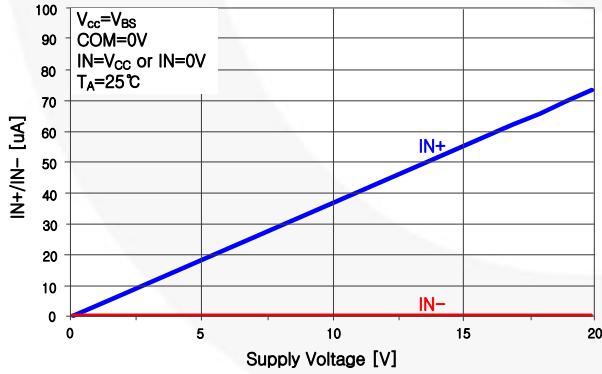


Figure 27. Input Bias Current vs. Supply Voltage

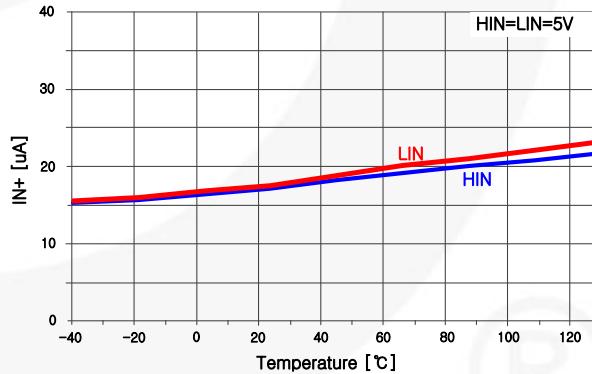


Figure 28. Input Bias Current vs. Temperature

## Typical Characteristics (Continued)

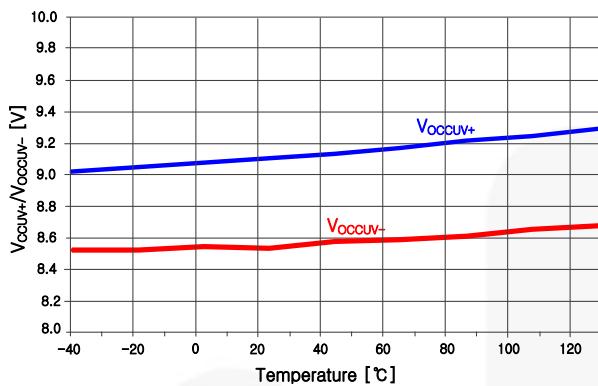
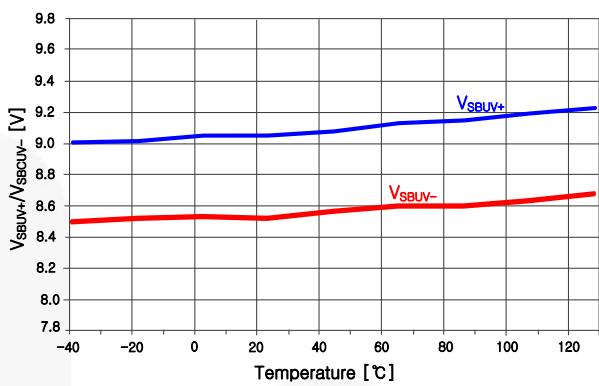
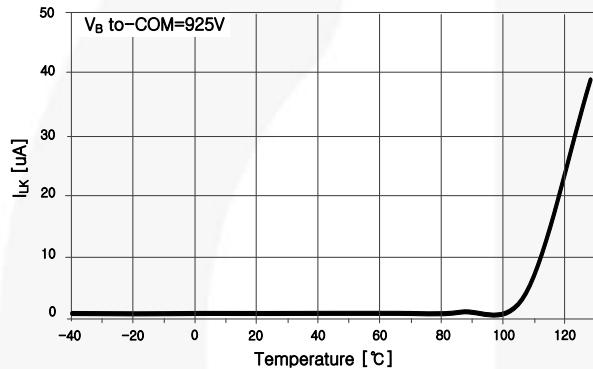
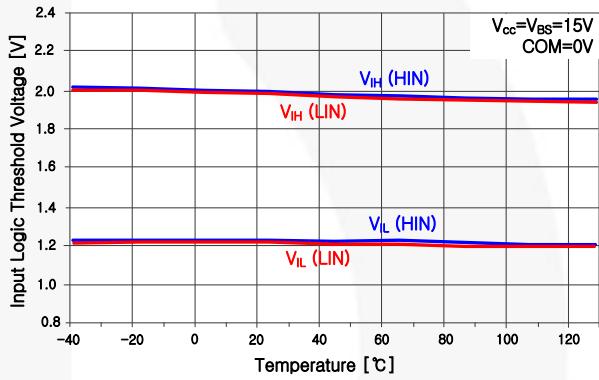
Figure 29.  $V_{cc}$  UVLO Threshold Voltage vs. TemperatureFigure 30.  $V_{BS}$  UVLO Threshold Voltage vs. TemperatureFigure 31.  $V_B$  to COM Leakage Current vs. Temperature

Figure 32. Input Logic Threshold Voltage vs. Temperature

## Switching Time Definitions

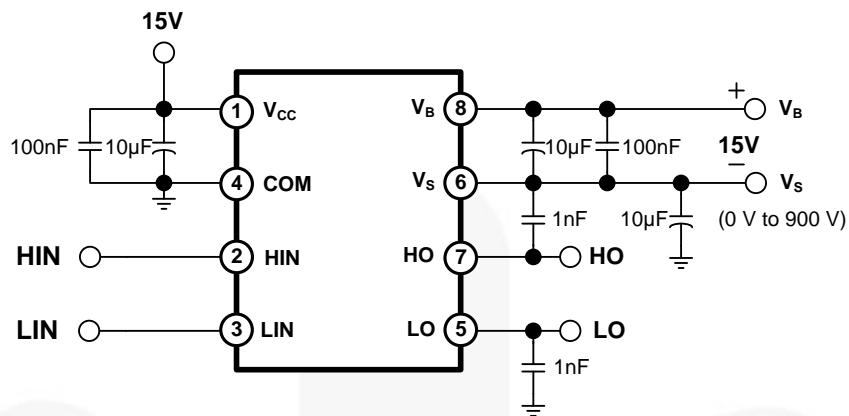


Figure 33. Switching Time Test Circuit

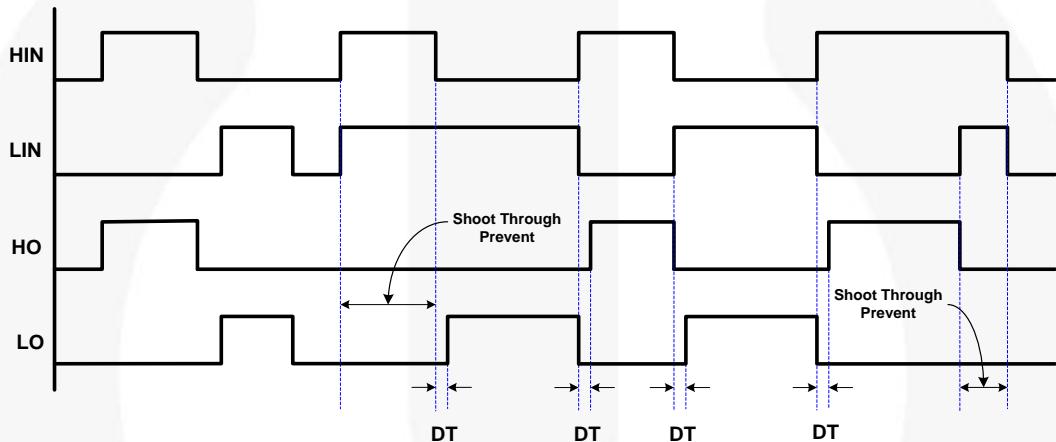


Figure 34. Input / Output Timing Diagram

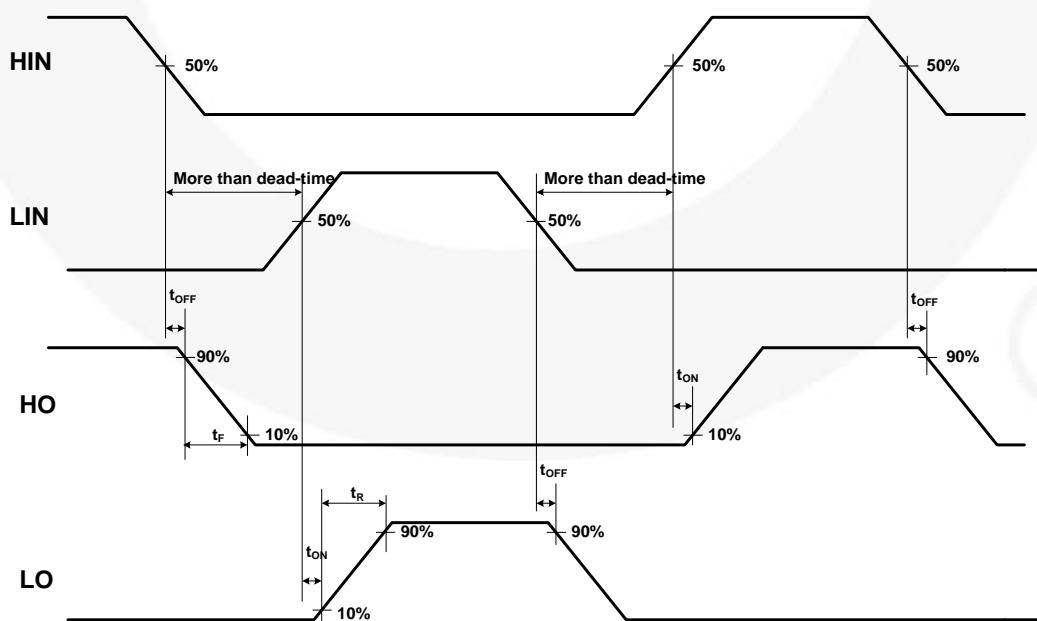


Figure 35. Switching Time Definition

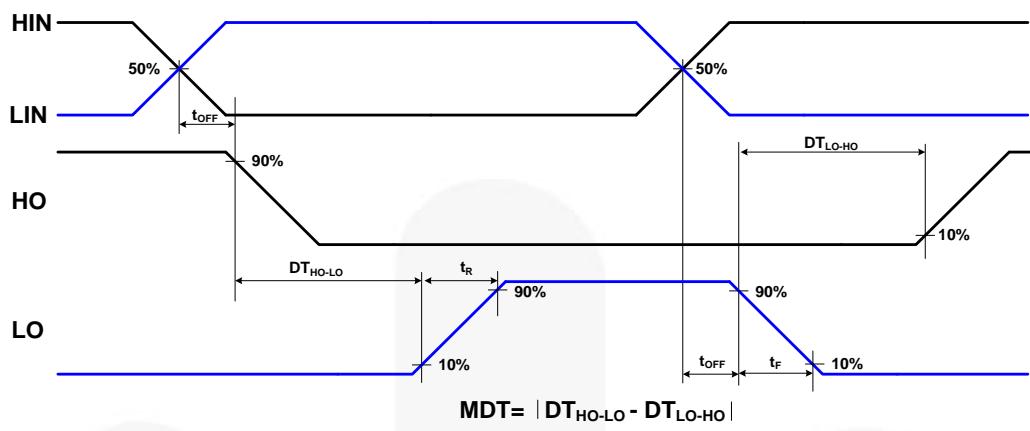
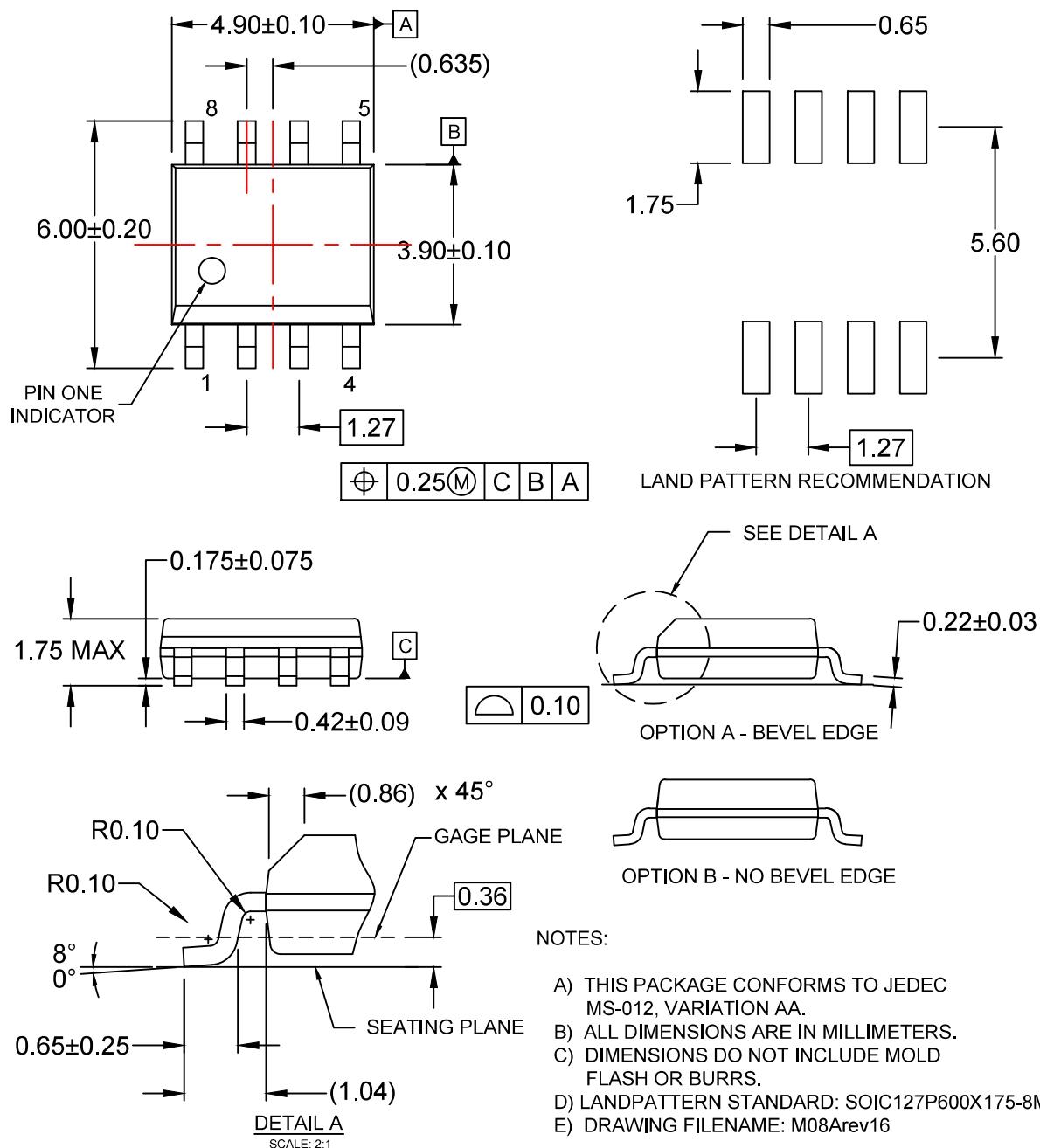
**Switching Time Definitions (Continued)**

Figure 36. Internal Dead Time Definition



## NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILE ENAME: M08Arev16

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