

# Dual D-Type Positive Edge-Triggered Flip-Flop

## MC74AC74, MC74ACT74

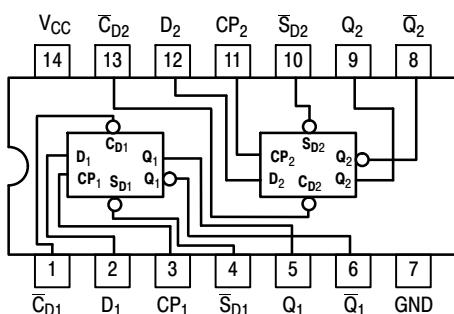
The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary ( $Q, \bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets  $Q$  to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets  $Q$  to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both  $Q$  and  $\bar{Q}$  HIGH

### Features

- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs
- These are Pb-Free Devices

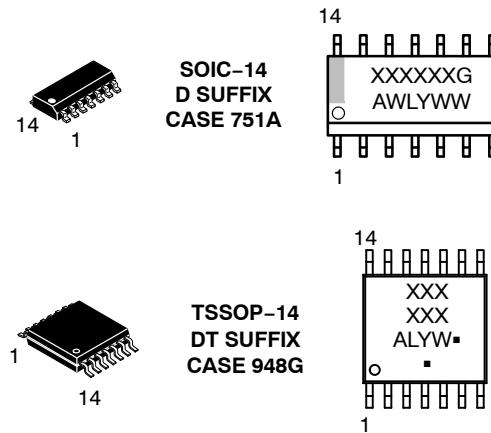


**Figure 1. Pinout: 14-Lead Packages Conductors  
(Top View)**

### PIN ASSIGNMENT

PIN	FUNCTION
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

### MARKING DIAGRAMS



XXX = Specific Device Code  
 A = Assembly Location  
 WL or L = Wafer Lot  
 Y = Year  
 WW or W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

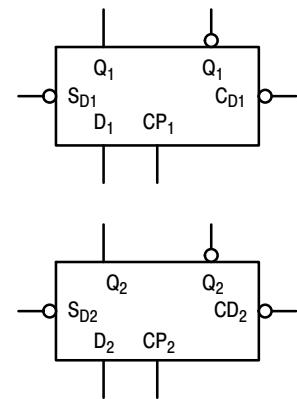
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MC74AC74, MC74ACT74

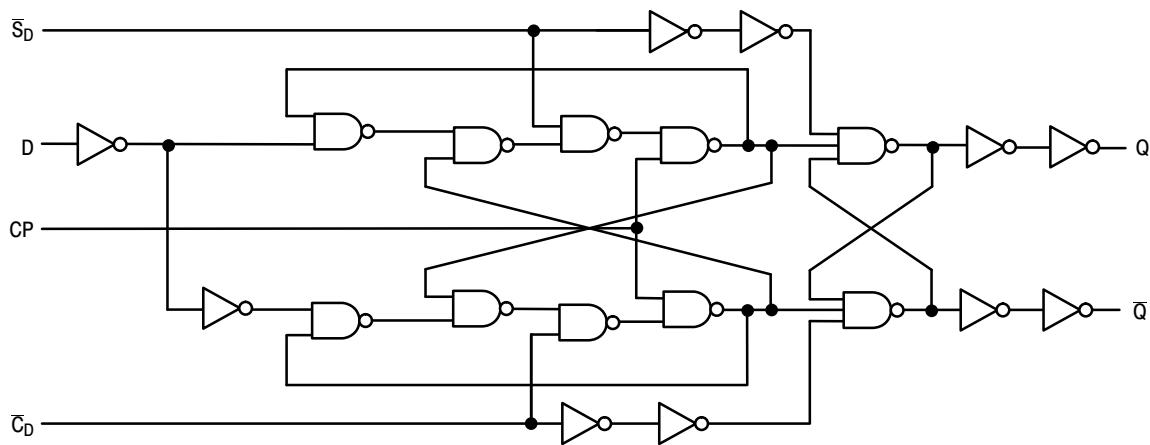
**TRUTH TABLE (Each Half)**

Inputs			Outputs		
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	—	H	H	L
H	H	—	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

NOTE: H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial;  
 — = LOW-to-HIGH Clock Transition  
 $Q_0(\bar{Q}_0)$  = Previous Q( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock



**Figure 2. Logic Symbol**



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

# MC74AC74, MC74ACT74

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	−0.5 to +6.5	V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
$V_O$	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	±20	mA
$I_{OK}$	DC Output Diode Current	±50	mA
$I_O$	DC Output Sink/Source Current	±50	mA
$I_{CC}$	DC Supply Current per Output Pin	±50	mA
$I_{GND}$	DC Ground Current per Output Pin	±50	mA
$T_{STG}$	Storage Temperature Range	−65 to +150	°C
$T_L$	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction temperature under Bias	+150	°C
$\theta_{JA}$	Thermal Resistance (Note 2)	SOIC TSSOP 116 150	°C/W
$P_D$	Power Dissipation in Still Air at 25°C	SOIC TSSOP 1077 833	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 3) Charged Device Model (Note 4)	> 2000 > 1000
$I_{Latch-Up}$	Latch-Up Performance Above $V_{CC}$ and Below GND at 85°C (Note 5)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $I_O$  absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	$V_{CC}$	V
$t_r, t_f$	Input Rise and Fall Time (Note ) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0$ V	–	150	–
		$V_{CC} @ 4.5$ V	–	40	–
		$V_{CC} @ 5.5$ V	–	25	–
$t_r, t_f$	Input Rise and Fall Time (Note ) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5$ V	–	10	–
		$V_{CC} @ 5.5$ V	–	8.0	–
$T_A$	Operating Ambient Temperature Range	−40	25	85	°C
$I_{OH}$	Output Current – High	–	–	−24	mA
$I_{OL}$	Output Current – Low	–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1.  $V_{in}$  from 30% to 70%  $V_{CC}$ ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2.  $V_{in}$  from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

# MC74AC74, MC74ACT74

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74AC		74AC	Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I <sub>OUT</sub> = -50 μA
		3.0 4.5 5.5	— — —	2.56 3.86 4.86	2.46 3.76 4.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -12 mA -24 mA -24 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I <sub>OUT</sub> = 50 μA
		3.0 4.5 5.5	— — —	0.36 0.36 0.36	0.44 0.44 0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> 12 mA 24 mA 24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	—	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	—	—	75	mA	V <sub>OLD</sub> = 1.65 V Max
I <sub>OH</sub>		5.5	—	—	-75	mA	V <sub>OH</sub> = 3.85 V Min
I <sub>CC</sub>		5.5	—	4.0	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.

## AC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			74AC	Unit	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	100 140	125 160	— —	95 125	— —	MHz
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	5.0 3.5	8.0 6.0	12.5 9.0	4.0 3.0	13.0 10.0	ns
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q̄ <sub>n</sub> or Q <sub>n</sub>	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	3.5 2.5	13.5 10.5	ns
t <sub>PLH</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	4.0 3.0	16.0 10.5	ns
t <sub>PHL</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	3.5 2.5	14.5 10.5	ns

\*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC74, MC74ACT74

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC		Unit	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum		
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	1.5	4.0	ns	
		5.0	1.0	3.0		
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	-2.0	0.5	ns	
		5.0	-1.5	0.5		
t <sub>w</sub>	C <sub>Pn</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	ns	
		5.0	2.5	4.5		
t <sub>rec</sub>	Recovery Time $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP	3.3	-2.5	0	ns	
		5.0	-2.0	0		

\*Voltage Range 3.3 V is 3.3 V  $\pm 0.3$  V.

Voltage Range 5.0 V is 5.0 V  $\pm 0.5$  V.

# MC74AC74, MC74ACT74

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		74ACT		Unit	Conditions		
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C					
			Typ	Guaranteed Limits						
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4		V	I <sub>OUT</sub> = -50 μA		
		4.5 5.5	— —	3.86 4.86	3.76 4.76		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -24 mA		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1		V	I <sub>OUT</sub> = 50 μA		
		4.5 5.5	— —	0.36 0.36	0.44 0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> 24 mA		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	—	±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND		
ΔI <sub>CCT</sub>	Additional Max. I <sub>CC</sub> /Input	5.5	0.6	—	1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	—	—	75		mA	V <sub>OLD</sub> = 1.65 V Max		
I <sub>OHD</sub>		5.5	—	—	-75		mA	V <sub>OHD</sub> = 3.85 V Min		
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	—	4.0	40		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND		

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			74ACT		Unit	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	145	210	—	125	—	MHz	
t <sub>PLH</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns	
t <sub>PHL</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $\bar{Q}_n$ or Q <sub>n</sub>	5.0	3.0	6.0	10.0	3.0	11.5	ns	
t <sub>PLH</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or $\bar{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns	
t <sub>PHL</sub>	Propagation Delay C <sub>Pn</sub> to $\bar{Q}_n$ or Q <sub>n</sub>	5.0	3.5	6.0	10.0	3.0	11.5	ns	

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC74, MC74ACT74

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		74ACT	Unit
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.5	ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0	1.0	ns
t <sub>w</sub>	C <sub>PN</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0	ns
t <sub>rec</sub>	Recovery Time $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP	5.0	-2.5	0	0	ns

\*Voltage Range 5.0 V is 5.0 V  $\pm$ 0.5 V.

## CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	35	pF	V <sub>CC</sub> = 5.0 V

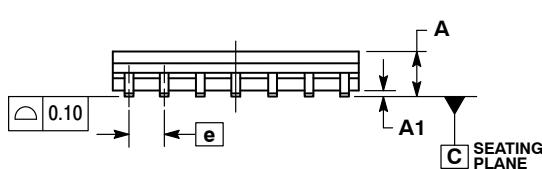
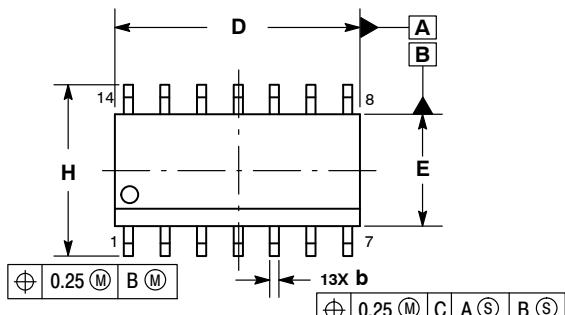
## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74AC74DG	AC74	SOIC-14	55 Units/Rail
MC74AC74DR2G	AC74	SOIC-14	2500/Tape & Reel
MC74AC74DTR2G	AC 74	TSSOP-14	2500/Tape & Reel
MC74ACT74DG	ACT74	SOIC-14	55 Units/Rail
MC74ACT74DR2G	ACT74	SOIC-14	2500/Tape & Reel
MC74ACT74DTR2G	ACT 74	TSSOP-14	2500/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

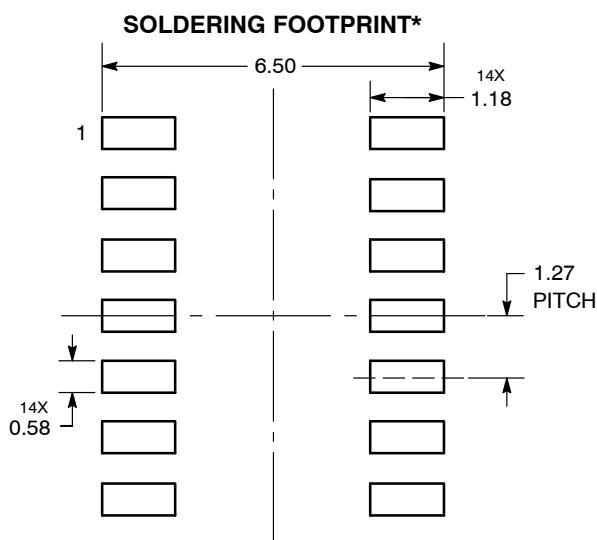
SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

## NOTES:

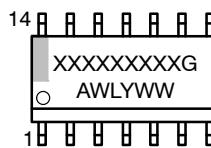
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*

XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

**onsemi** and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**SOIC-14**  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

**STYLE 1:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 2:**  
CANCELLED

**STYLE 3:**  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

**STYLE 4:**  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 5:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

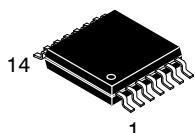
**STYLE 6:**  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

**STYLE 7:**  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

**STYLE 8:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

<b>DOCUMENT NUMBER:</b>	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	SOIC-14 NB	<b>PAGE 2 OF 2</b>

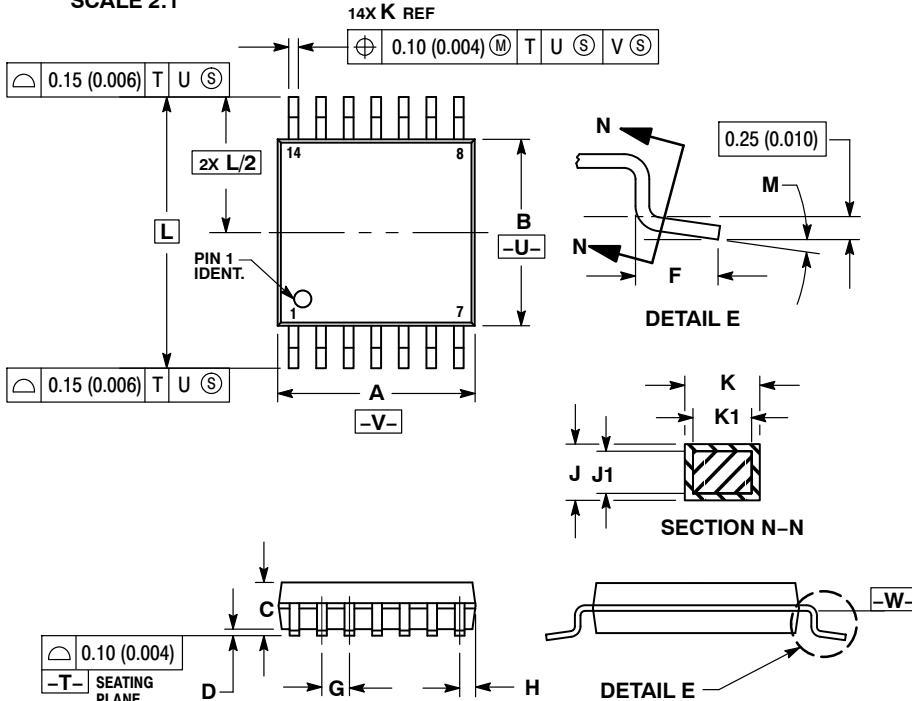
onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



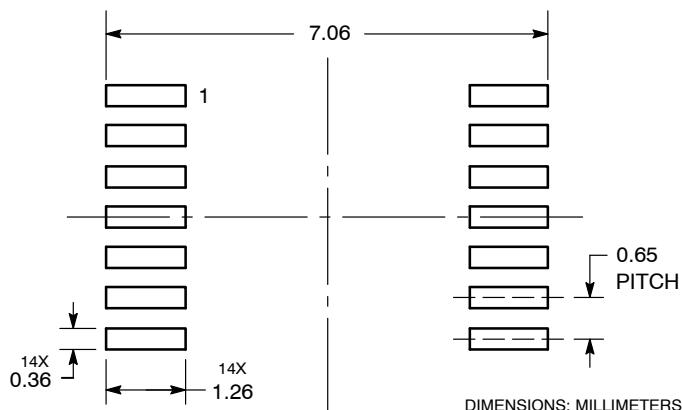
**TSSOP-14 WB**  
**CASE 948G**  
**ISSUE C**

DATE 17 FEB 2016

**SCALE 2:1**



**RECOMMENDED  
SOLDERING FOOTPRINT\***



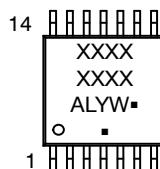
\*For additional information on our Pb-Free strategy and soldering details, please download the [onsemi](#) Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM  $MPA\text{NE}$  -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	----	1.20	----	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

## GENERIC MARKING DIAGRAM\*



A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot ":", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98ASH70246A</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSSOP-14 WB</b>	<b>PAGE 1 OF 1</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **ONSEMI**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi](#):

[MC74AC74DG](#) [MC74AC74DR2G](#) [MC74AC74DTR2G](#) [MC74ACT74DG](#) [MC74ACT74DR2G](#) [MC74ACT74DTR2G](#)  
[NLV74AC74DR2G](#)