

# Hot Swap Smart Fuse

## NCP81295, NCP81296

The NCP81295 and NCP81296 are 50 A, electronically re-settable, in-line fuses for use in 12 V, high current applications such as servers, storage and base stations. The NCP81295/6 offers a very low 0.65 mΩ integrated MOSFET to reduce solution size and minimize power loss. It also integrates a highly accurate current sensor for monitoring and overload protection.

### Power Features

- Co-packaged Power Switch, Hotswap Controller and Current Sense
- Up to 60 A Peak Current Output, 50 A Continuous
- Vin Range: 4.5 V to 18 V
- 0.65 mΩ, no R<sub>SENSE</sub> Required

### Control Features

- Enable Input
- Optional Enable-controlled Output Pulldown when Disabled
- Programmable Soft-Start
- Programmable, Multi-level Current Limit

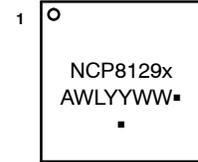
### Reporting Features

- Accurate Analog Load Current Monitor
- Programmable Over Current Alert Output
- Analog Temperature Output
- Status Fault OK Output

### Other Features

- 5 mm x 5 mm QFN32 Package
- Operating Temperature: -40°C to 125°C
- Can be Paralleled for Higher Current Applications
- Built-in Insertion Delay for Hotswap Applications
- NCP81295: Latch off for Following Protection Features
- NCP81296: Auto-Retry Mode for Following Protection Features
  - ◆ Current-limit after Delay
  - ◆ Fast Short-circuit Protection
  - ◆ Over-Temperature Shutdown
  - ◆ Excessive Soft-start Duration
- Internal Switch Fault Diagnostics
- Low-power Auxiliary Output Voltage

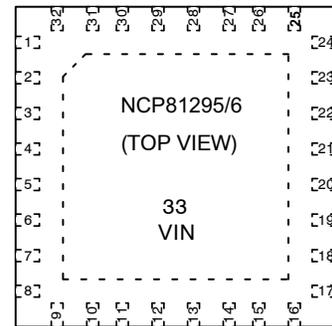
### MARKING DIAGRAM



NCP8129x = Specific Device Code  
 x = 5 or 6  
 A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week  
 ■ = Pb-Free Package (may or may not be present)

(Note: Microdot may be in either location)

### PINOUT

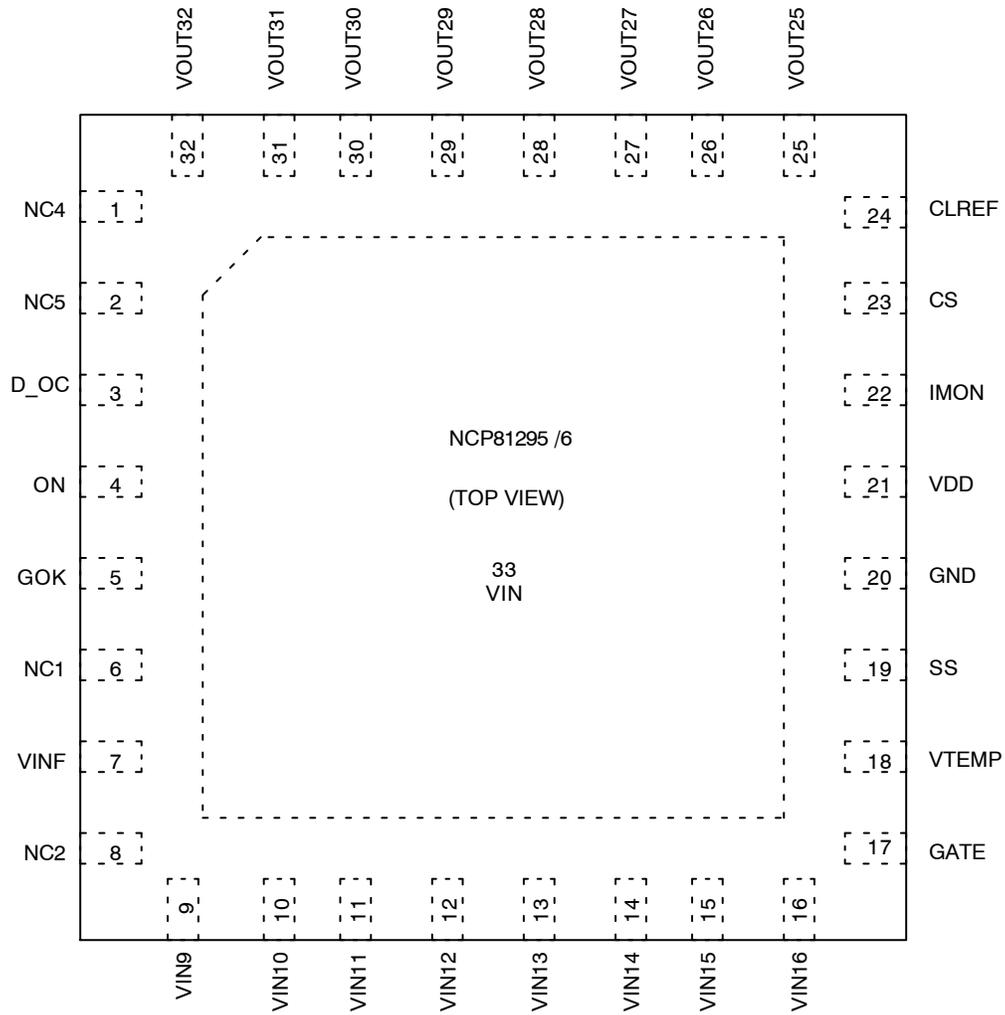


For more details see Figure 1.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NCP81295, NCP81296



**Figure 1. Pin Configuration**

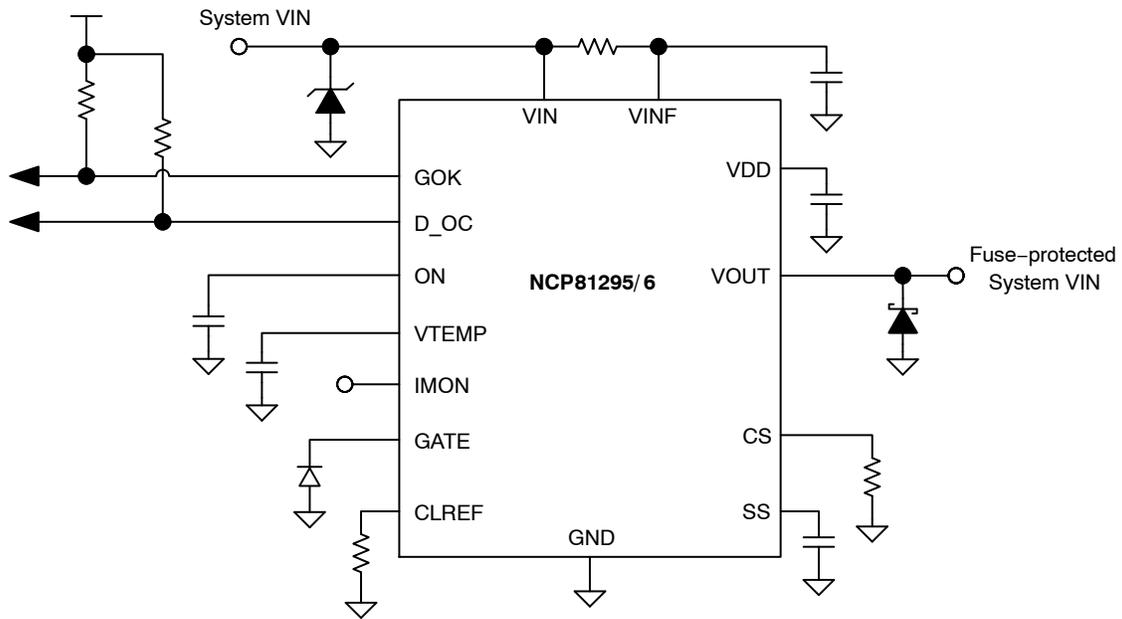
## Ordering Information

**Table 1. AVAILABLE DEVICES**

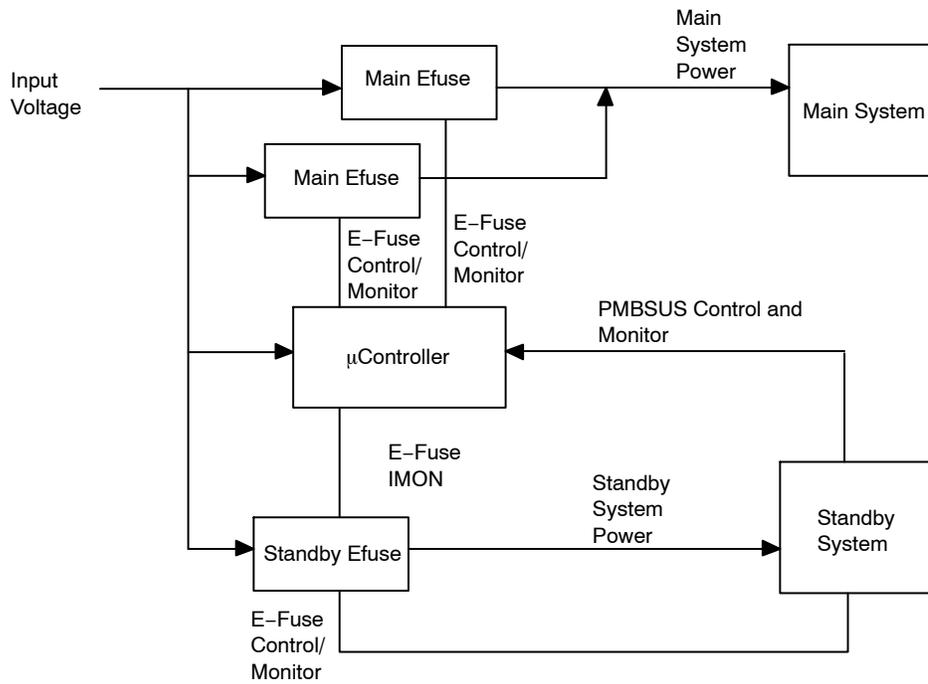
| Device        | Package | Shipping <sup>†</sup> |
|---------------|---------|-----------------------|
| NCP81295MNTXG | QFN32   | 2500 / Tape & Reel    |
| NCP81296MNTXG | QFN32   | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## NCP81295, NCP81296



**Figure 2. Typical Application**



**Figure 3. Typical Application Diagram**

# NCP81295, NCP81296

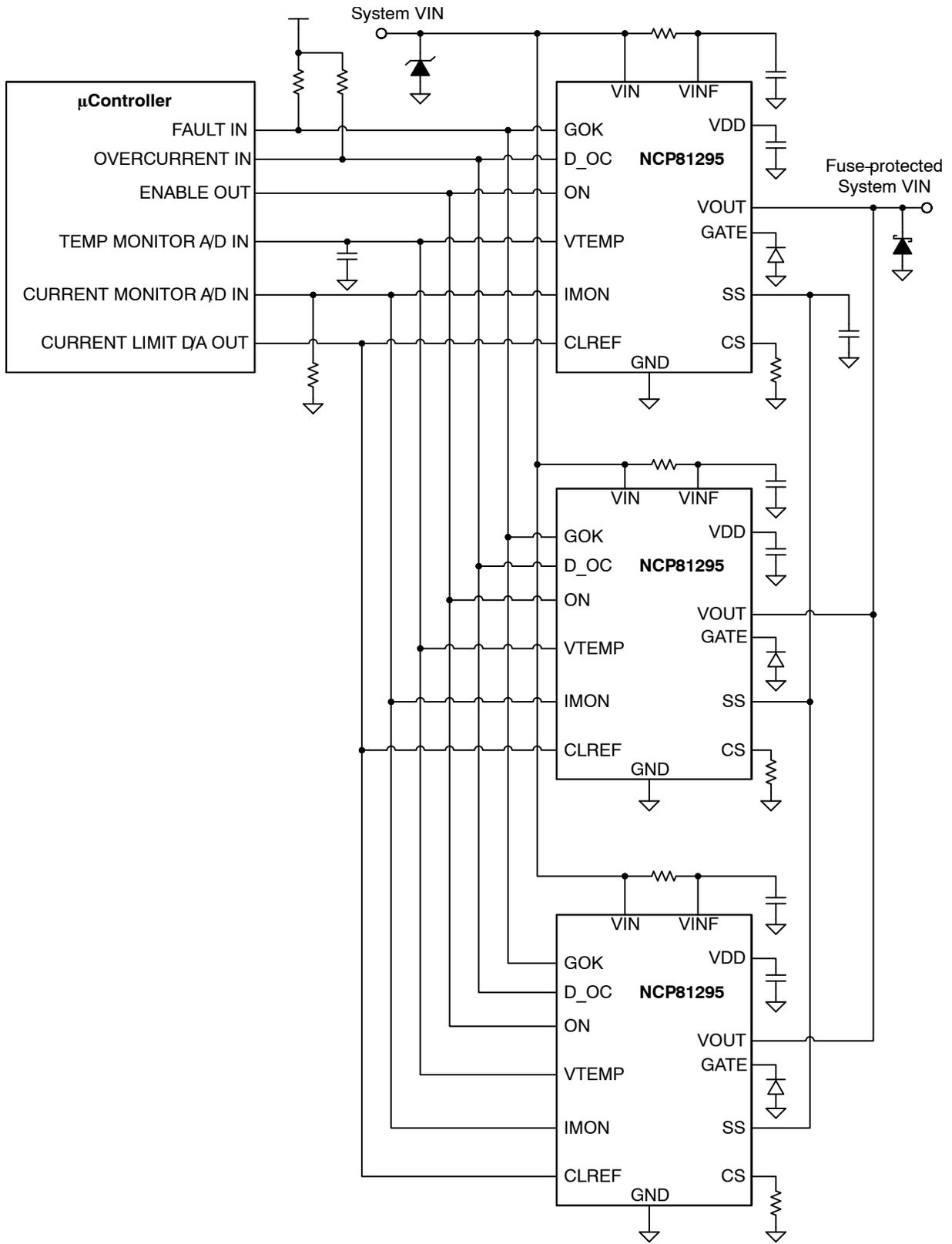
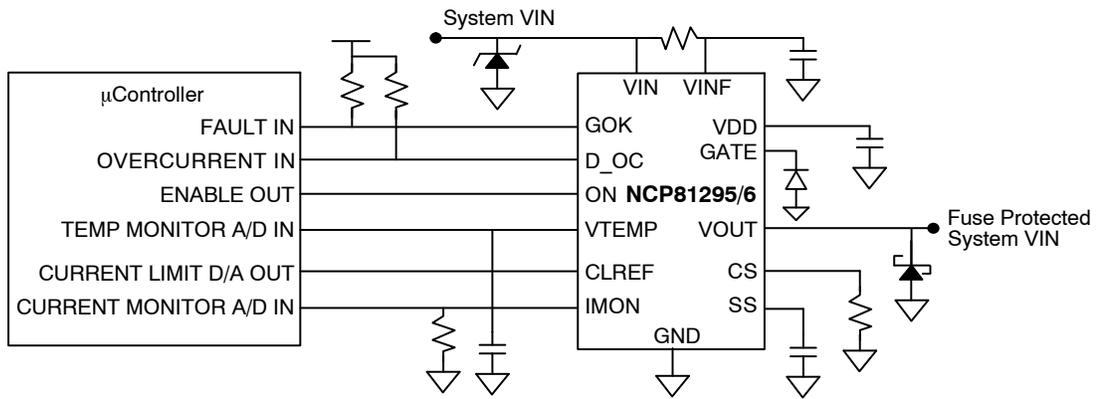
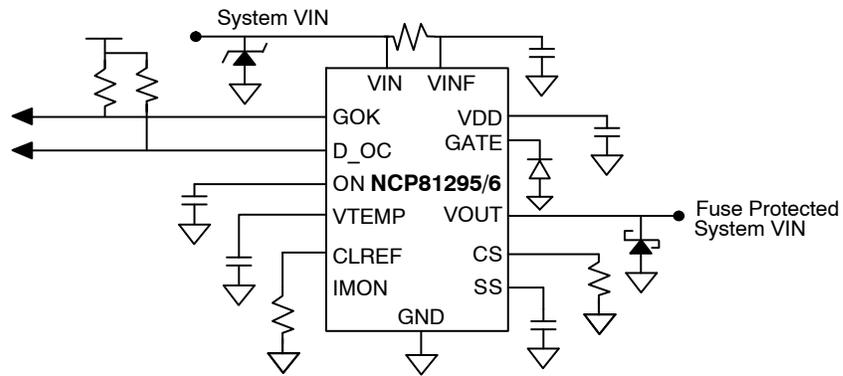


Figure 4. Application Schematic – Parallel Fuse Operation with Controller

## NCP81295, NCP81296



**Figure 5. Application Schematic – Single eFuse with Controller**



**Figure 6. Application Schematic – Stand-alone Single eFuse**

# NCP81295, NCP81296

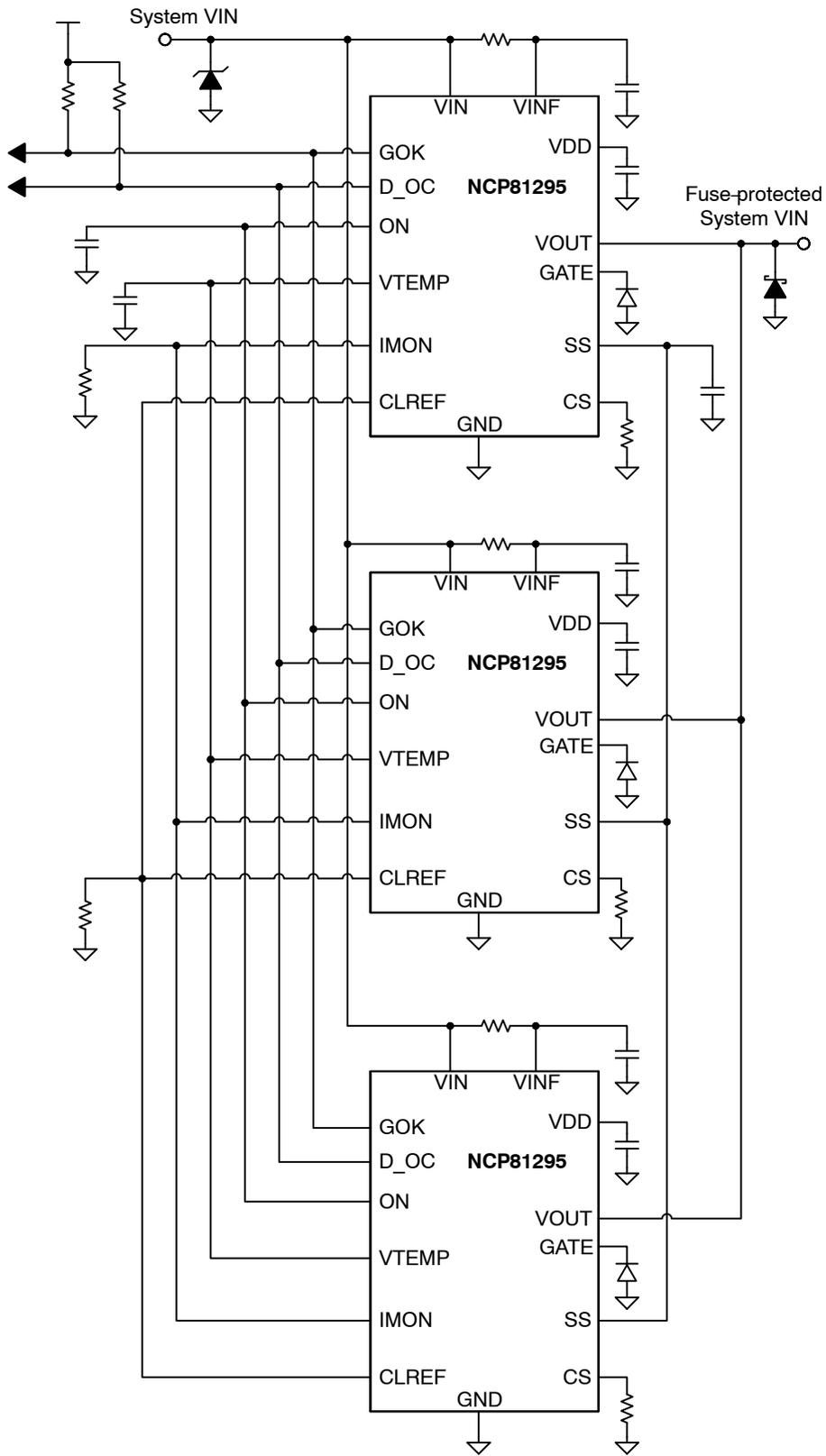


Figure 7. Application Schematic – Stand-alone Parallel EFuse

# NCP81295, NCP81296

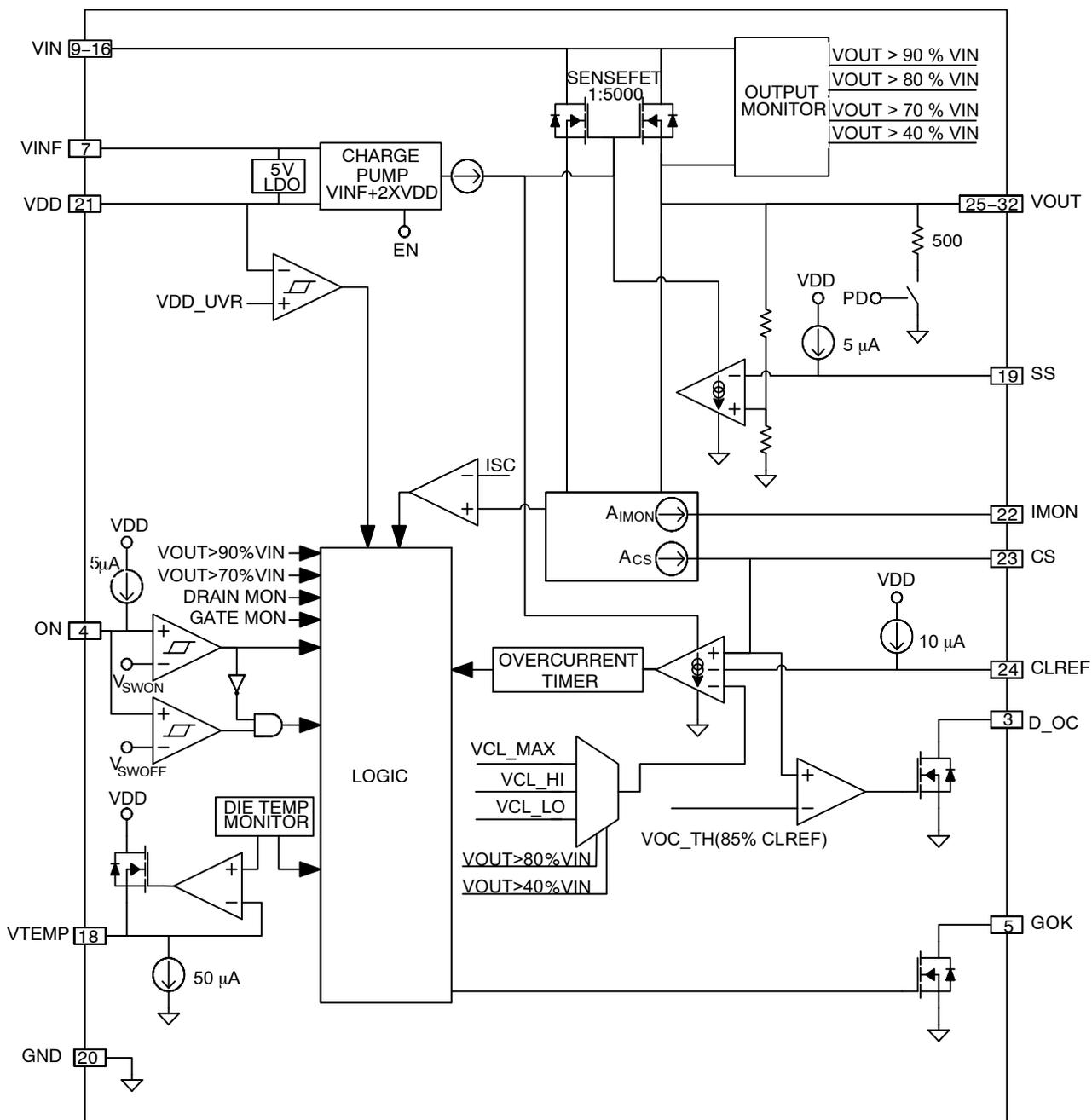


Figure 8. Block Diagram

## NCP81295, NCP81296

**Table 2. PIN DESCRIPTION**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | NC4    | No electrical connection internally. May connect to any potential  |
| 2       | NC5    | No electrical connection internally. May connect to any potential  |
| 3       | D_OC   | Overcurrent indicator output (open drain). Low indicates the NCP81295 is limiting current. The D_OC output does not report current limiting during soft-start.   |
| 4       | ON     | Enable input and output pulldown resistance control.   |
| 5       | GOK    | OK status indicator output (open drain). Low indicates that the NCP81295 was turned off by a fault.  |
| 6       | NC1    | Test pin. Do not connect to this pin. Leave floating   |
| 7       | VINF   | Control circuit power supply input. Connect to VIN pins through an RC filter. (1 $\Omega$ / 0.1 $\mu$ F)   |
| 8       | NC2    | Internal FET sense pin. Do not connect to this pin. Leave floating   |
| 9       | VIN09  | Input of high current output switch  |
| 10      | VIN10  | Input of high current output switch  |
| 11      | VIN11  | Input of high current output switch  |
| 12      | VIN12  | Input of high current output switch  |
| 13      | VIN13  | Input of high current output switch  |
| 14      | VIN14  | Input of high current output switch  |
| 15      | VIN15  | Input of high current output switch  |
| 16      | VIN16  | Input of high current output switch  |
| 17      | GATE   | Internal FET gate pin. Connect to the cathode of an anode grounded diode such as BAS16P2T5G. A 4.7 nF ceramic capacitor is reserved between this pin and GND for NCP81295 to mitigate the oscillation risk when small amount of output capacitance (< 100 $\mu$ F) or long input/output cable (large $L_{IN}$ / $L_{OUT}$ ) happens. |
| 18      | VTEMP  | Analog temperature monitor output.   |
| 19      | SS     | Soft Start time programming pin. Connect a capacitor to this pin to set the softstart time.  |
| 20      | GND    | Ground   |
| 21      | VDD    | Linear regulator output  |
| 22      | IMON   | Analog current monitor output  |
| 23      | CS     | Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and overcurrent indicator D_OC.   |
| 24      | CLREF  | Current limit setpoint input for normal operation (after soft-start).  |
| 25      | VOUT25 | Output of high current output switch   |
| 26      | VOUT26 | Output of high current output switch   |
| 27      | VOUT27 | Output of high current output switch   |
| 28      | VOUT28 | Output of high current output switch   |
| 29      | VOUT29 | Output of high current output switch   |
| 30      | VOUT30 | Output of high current output switch   |
| 31      | VOUT31 | Output of high current output switch   |
| 32      | VOUT32 | Output of high current output switch   |
| 33      | VIN33  | Input of high current output switch  |

# NCP81295, NCP81296

**Table 3. MAXIMUM RATINGS**

| Rating  | Symbol                               | Min                    | Max       | Unit |
|---|--------------------------------------|------------------------|-----------|------|
| Pin Voltage Range (Note 1) Vout enabled   | VINx, VINf                           | -0.3                   | 20        | V    |
| Pin Voltage Range (Note 1) Vout disabled (Note 2)                                 | VINx, VINf                           | -0.3                   | 30        | V    |
| OUT Pin Voltage Range (Note 1)  | VOUTx                                | -0.3<br>-1 (<500 ms)   | 20        | V    |
| VDD Pin Voltage Range (Note 1)  | VDD                                  | -0.3                   | 6.0       | V    |
| GATE Pin Voltage Range  | V <sub>GATE</sub>                    | -0.3,<br>-0.8 (< 1 ms) | 30        | V    |
|   | V <sub>GATE</sub> - V <sub>OUT</sub> | -20                    | 20        | V    |
| Pin Voltage Range (Note 3)  | All Other Pins                       | -0.3                   | VDD + 0.3 | V    |
| Operating Junction Temperature  | T <sub>J(max)</sub>                  |                        | 150       | °C   |
| Storage Temperature Range   | T <sub>STG</sub>                     | -55                    | 150       | °C   |
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Pb-Free Versions (Note 4) | T <sub>SLD</sub>                     |                        | 260       | °C   |
| Electrostatic Discharge - Charged Device Model                                    | ESD <sub>CDM</sub>                   |                        | 2.0       | kV   |
| Electrostatic Discharge - Human Body Model  | ESD <sub>HBM</sub>                   |                        | 2.5       | kV   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.
2. Vout disable is the state of output OFF when internal FET has turned off by disable ON or FAULTs protection.
3. Pin ratings referenced to VDD apply with VDD at any voltage within the VDD Pin Voltage Range.
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**Table 4. THERMAL CHARACTERISTICS**

| Rating   | Symbol            | Value | Unit |
|--|-------------------|-------|------|
| Thermal Resistance, Junction-to-Ambient (Note 5) | R <sub>θJA</sub>  | 30    | °C/W |
| Thermal Resistance, Junction-to-Top-Case         | R <sub>θJCT</sub> | 50    | °C/W |
| Thermal Resistance, Junction-to-Bottom-Case      | R <sub>θJCB</sub> | 1.5   | °C/W |
| Thermal Resistance, Junction-to-Board (Note 6)   | R <sub>θJB</sub>  | 1.5   | °C/W |
| Thermal Resistance, Junction-to-Case (Note 7)    | R <sub>θJC</sub>  | 1.5   | °C/W |

5. R<sub>θJA</sub> is obtained by simulating the device mounted on a 500 mm<sup>2</sup>, 1-oz Cu pad on a 80 mm x 80 mm, 1.6 mm thick 8-layer FR4 board.
6. R<sub>θJB</sub> value based on hottest board temperature within 1 mm of the package.
7. R<sub>θJC</sub> ≈ R<sub>θJCT</sub> // R<sub>θJCB</sub> (Two-Resistor Compact Thermal Model, JESD15-3).

**Table 5. RECOMMENDED OPERATING RANGES**

| Parameter                           | Symbol             | Min | Max  | Unit |
|-------------------------------------|--------------------|-----|------|------|
| VIN, VINf Pin Voltage Range         |                    | 4.5 | 18   | V    |
| Maximum Continuous Output Current   | I <sub>Ave</sub>   |     | 50   | A    |
| Peak Output Current                 | I <sub>PEAK</sub>  |     | 60   | A    |
| VDD Output Load Capacitance Range   | C <sub>VDD</sub>   | 2.2 | 10   | μF   |
| VTEMP Output Load Capacitance Range | C <sub>VTEMP</sub> | 0.1 |      | μF   |
| Softstart Duration                  | T <sub>SS</sub>    | 10  | 110  | ms   |
| CS Load Resistance Range            | R <sub>CS</sub>    | 1.8 | 4    | kΩ   |
| CLREF Voltage Range                 | V <sub>CLREF</sub> | 0.2 | 1.55 | V    |
| Operating Junction Temperature      | T <sub>J(OP)</sub> | -40 | 125  | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## NCP81295, NCP81296

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{INx} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VINf} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{VTEMP} = 0.1\ \mu\text{F}$ ,  $R_{VTEMP} = 1\ \text{k}\Omega$ ,  $C_{SS} = 100\ \text{nF}$  (unless specified otherwise) Min/Max values are valid for the temperature range  $-40^\circ\text{C} \leq T_A = T_J \leq 125^\circ\text{C}$  unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|-----------|--------|-----------------|-----|-----|-----|-------|
|-----------|--------|-----------------|-----|-----|-----|-------|

### VINF INPUT

|                   |  |   |  |      |     |    |
|-------------------|--|---|--|------|-----|----|
| Quiescent Current |  | $V_{ON} > 1.4\text{ V}$ , no load                 |  | 3.23 | 5.0 | mA |
|                   |  | $V_{ON} > 1.4\text{ V}$ , fault                   |  |      | 5.0 | mA |
|                   |  | $V_{ON} < 0.8\text{ V}$                           |  | 2.38 | 4.0 | mA |
|                   |  | $V_{ON} < 0.8\text{ V}$ , $V_{INF} = 16\text{ V}$ |  |      | 4.0 | mA |

### VDD REGULATOR

|                          |               |   |     |      |     |    |
|--------------------------|---------------|---|-----|------|-----|----|
| VDD Output Voltage       | $V_{DD\_NL}$  | $I_{VDD} = 0\text{ mA}$ , $V_{INF} = 6\text{ V}$    | 4.7 | 5.09 | 5.3 | V  |
| VDD Load Capability      | $I_{DDLOAD}$  | $V_{INF} = 5.5\text{ V}$                            |     |      | 30  | mA |
| VDD Current Limit        | $I_{DD\_CL}$  | $V_{INF} = 12\text{ V}$ and $V_{INF} = 6\text{ V}$  | 50  | 70   |     | mA |
| VDD Dropout Voltage      |               | $I_{VDD} = 25\text{ mA}$ , $V_{INF} = 4.5\text{ V}$ |     | 85   | 200 | mV |
| UVLO threshold – rising  | $V_{DD\_UVR}$ |   | 4.1 | 4.3  | 4.5 | V  |
| UVLO threshold – falling | $V_{DD\_UVF}$ |   | 3.8 | 4.0  | 4.2 | V  |

### ON INPUT

|                                      |                |  |      |      |      |                  |
|--------------------------------------|----------------|--|------|------|------|------------------|
| Bias Current                         | $I_{ON}$       | From pin into a 0 V or 1.5 V source                                      | 4.0  | 5.0  | 6.0  | $\mu\text{A}$    |
| Switch ON Threshold                  | $V_{SWON}$     |  | 1.33 | 1.4  | 1.47 | V                |
| Switch OFF/ Pulldown Upper Threshold | $V_{SWOFF}$    |  | 1.13 | 1.2  | 1.27 | V                |
| Pulldown Lower Threshold             | $V_{PDOFF}$    |  |      | 0.8  |      | V                |
| Switch ON Delay Timer                | $t_{ON}$       | From ON transitioning above $V_{SWON}$ to SS start                       | 0.6  | 1.0  | 2.5  | ms               |
| Switch OFF Delay Time (Note 8)       | $t_{OFF}$      | From ON transitioning below $V_{SWOFF}$ to GATE pulldown                 |      | 1.7  |      | $\mu\text{s}$    |
| ON Current Source Clamp Voltage      | $V_{ON\_CLMP}$ | Max pullup voltage of current source                                     |      | 3.0  |      | V                |
| Load Pulldown Delay Timer            | $t_{PD\_DEL}$  | From ON transitioning into the range between $V_{SWOFF}$ and $V_{PDOFF}$ |      | 2.0  |      | ms               |
| Output Pulldown Resistance           | $R_{PD}$       | $V_{OUT} = 12\text{ V}$ , PD mode = 1                                    |      | 0.77 |      | $\text{k}\Omega$ |

### SS PIN

|                     |              |                                   |      |      |      |               |
|---------------------|--------------|-----------------------------------|------|------|------|---------------|
| Bias Current        | $I_{SS}$     | From pin into a 0 V or 1 V source | 4.62 | 5.15 | 5.62 | $\mu\text{A}$ |
| Gain to VOUT        | $A_{VSS}$    |                                   | 9.6  | 10   | 10.4 | V/V           |
| SS Pulldown Voltage | $V_{OL\_SS}$ | 0.1 mA into pin during ON delay   |      | 22   |      | mV            |

### GOK OUTPUT

|                           |               |                         |  |  |     |               |
|---------------------------|---------------|-------------------------|--|--|-----|---------------|
| Output Low Voltage        | $V_{OL\_GOK}$ | $I_{GOK} = 1\text{ mA}$ |  |  | 0.1 | V             |
| Off-state Leakage Current | $I_{LK\_GOK}$ | $V_{GOK} = 5\text{ V}$  |  |  | 1.0 | $\mu\text{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

## NCP81295, NCP81296

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{INx} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VINf} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{VTEMP} = 0.1\ \mu\text{F}$ ,  $R_{VTEMP} = 1\ \text{k}\Omega$ ,  $C_{SS} = 100\ \text{nF}$  (unless specified otherwise) Min/Max values are valid for the temperature range  $-40^\circ\text{C} \leq T_A = T_J \leq 125^\circ\text{C}$  unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

| Parameter   | Symbol                      | Test Conditions                      | Min                  | Typ | Max | Units         |
|---|-----------------------------|--------------------------------------|----------------------|-----|-----|---------------|
| <b>IMON/CS OUTPUT</b>   |                             |                                      |                      |     |     |               |
| IMON or CS Current (single EFuse)<br>Based on $10\ \mu\text{A}/\text{A} + 5\ \mu\text{A}$ | $I_{IMON}/I_{CS}$           | $T_J = 0\text{ to }85^\circ\text{C}$ | IOUT = 5 A (Note 8)  |     | 55  | $\mu\text{A}$ |
|   |                             |                                      | IOUT = 10 A (Note 8) |     | 105 | $\mu\text{A}$ |
|   |                             |                                      | IOUT = 25 A (Note 8) |     | 255 | $\mu\text{A}$ |
|   |                             |                                      | IOUT = 50 A (Note 8) |     | 505 | $\mu\text{A}$ |
| Accuracy (single EFuse)   |                             | $T_J = 0\text{ to }85^\circ\text{C}$ | IOUT = 5 A (Note 8)  | -6  | +6  | %             |
|   |                             |                                      | IOUT = 10 A (Note 8) | -4  | +4  | %             |
|   |                             |                                      | IOUT = 25 A (Note 8) | -4  | +4  | %             |
|   |                             |                                      | IOUT = 50 A (Note 8) | -4  | +4  | %             |
| IMON or CS Current Source Clamp Voltage   | $V_{IM\_CLMP}/V_{CS\_CLMP}$ | Max pullup voltage of current source |                      | 3.0 |     | V             |
| Pre-Biased Offset Current Load for Auto-Zero Op-Amp                                       | $I_{AZ\_BIAS}$              |                                      |                      | 5.0 |     | $\mu\text{A}$ |

### CURRENT LIMIT & CLREF PIN

|                                     |                |  |      |     |      |               |
|-------------------------------------|----------------|--|------|-----|------|---------------|
| Current Limit Voltage               | $V_{CL\_TH}$   | If $V_{CS} > V_{CL\_TH}$ current limiting regulation occurs via gate | 95   | 98  | 101  | $\%V_{CLREF}$ |
| Current Limit Enact Offset Voltage  | $V_{ENACT}$    | $0.2\text{ V} < V_{CLREF} < 1.4\text{ V}$                            | -70  | -24 | 12   | mV            |
| Current Limit Clamp Voltage         | $V_{CL\_LO}$   | $V_{OUT} < 40\% V_{IN}$ , $V_{CLREF} > 0.15\text{ V}$                | 143  | 152 | 162  | mV            |
|                                     | $V_{CL\_HI}$   | $40\% V_{IN} < V_{OUT} < 80\% V_{IN}$<br>$V_{CLREF} > 0.5\text{ V}$  | 480  | 504 | 520  | mV            |
| Max Current Limit Reference Voltage | $V_{CL\_MX}$   | $V_{OUT} > 80\% V_{IN}$ , $V_{CLREF} > 1.6\text{ V}$                 | 1.55 | 1.6 | 1.65 | V             |
| Response Time (Note 8)              | $t_{CL\_REG}$  | $V_{CS} > V_{CLREF}$ until current limiting                          |      | 200 |      | $\mu\text{s}$ |
| CLREF Bias Current                  | $I_{CL}$       | From pin into a 1.2 V source   | 9.6  | 10  | 10.4 | $\mu\text{A}$ |
| CLREF Current Source Clamp Voltage  | $V_{CL\_CLMP}$ | Max pullup voltage of current source                                 |      | 3.0 |      | V             |
| FET Turn-off Timer                  | $t_{CL\_LA}$   | Delay between current limit detection and FET turn-off (GOK = 0)     |      | 250 |      | $\mu\text{s}$ |

### D\_OC OUTPUT

|                           |               |   |    |     |     |               |
|---------------------------|---------------|---|----|-----|-----|---------------|
| Overcurrent Threshold     | $V_{OC\_TH}$  | If $V_{CS} > V_{OC\_TH}$ D_OC pin pulls low | 83 | 86  | 90  | $\%V_{CLREF}$ |
| Output Low Voltage        | $V_{OL\_DOC}$ | $I_{DOC} = 1\ \text{mA}$                    |    |     | 0.1 | V             |
| Off-state Leakage Current | $I_{LK\_DOC}$ | $V_{DOC} = 5\text{ V}$                      | -  |     | 1.0 | $\mu\text{A}$ |
| Delay (rising) (Note 8)   |               | $V_{CS} < \text{limit}$ until D_OC rising   | -  | 1.0 |     | $\mu\text{s}$ |
| Delay (falling) (Note 8)  |               | $V_{CS} > \text{limit}$ until D_OC falling  | -  | 1.0 |     | $\mu\text{s}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

## NCP81295, NCP81296

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{INx} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VINf} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{VTEMP} = 0.1\ \mu\text{F}$ ,  $R_{VTEMP} = 1\ \text{k}\Omega$ ,  $C_{SS} = 100\ \text{nF}$  (unless specified otherwise) Min/Max values are valid for the temperature range  $-40^\circ\text{C} \leq T_A = T_J \leq 125^\circ\text{C}$  unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

| Parameter                       | Symbol           | Test Conditions   | Min | Typ  | Max | Units                |
|---------------------------------|------------------|---|-----|------|-----|----------------------|
| <b>SHORT CIRCUIT PROTECTION</b> |                  |   |     |      |     |                      |
| Current Threshold (Note 8)      | $I_{SC}$         | NCP81295  |     | 100  |     | A                    |
|                                 |                  | NCP81296  |     | 80   |     | A                    |
| Response Time (Note 8)          | $t_{SC}$         | From $I_{OUT} > I_{LIMSC}$ until gate pulldown                                |     | 500  |     | ns                   |
| <b>VTEMP OUTPUT</b>             |                  |   |     |      |     |                      |
| Bias Voltage                    | $V_{VTEMP25}$    | At $25^\circ\text{C}$   |     | 450  |     | mV                   |
| Gain (Note 8)                   | $A_{VTEMP}$      | $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$                             |     | 10   |     | mV/ $^\circ\text{C}$ |
| Load Capability                 | $R_{VTEMP}$      | At $25^\circ\text{C}$   |     | 1    |     | k $\Omega$           |
| Pulldown Current                | $I_{VTEMP}$      | At $25^\circ\text{C}$   |     | 50   |     | $\mu\text{A}$        |
| <b>THERMAL SHUTDOWN</b>         |                  |   |     |      |     |                      |
| Temperature Shutdown (Note 8)   | $T_{TSD}$        | GOK pulls dow   |     | 140  |     | $^\circ\text{C}$     |
| <b>OUTPUT SWITCH (FET)</b>      |                  |   |     |      |     |                      |
| On Resistance                   | $R_{DSon}$       | $T_J = 25^\circ\text{C}$  |     | 0.65 | 1.0 | m $\Omega$           |
| Off-state leakage current       | $I_{DSoff}$      | $V_{IN} = 16\text{ V}$ , $V_{ON} < 1.2\text{ V}$ , $T_J = 25^\circ\text{C}$   |     |      | 1.0 | $\mu\text{A}$        |
| <b>FAULT detection</b>          |                  |   |     |      |     |                      |
| $V_{DS}$ Short Threshold        | $V_{DS\_TH}$     | Startup postponed if $V_{OUT} > V_{DS\_TH}$ at $V_{ON} > V_{SWON}$ transition |     | 88.8 |     | % $V_{IN}$           |
| $V_{DS}$ Short OK Threshold     | $V_{DS\_OK}$     | Startup resumed if $V_{OUT} < V_{DS\_OK}$ anytime after postponed             |     | 68.6 |     | % $V_{IN}$           |
| $V_{GD}$ Short Threshold        | $V_{DG\_TH}$     | Startup postponed if $V_G > V_{DG\_TH}$ at $V_{ON} > V_{SWON}$ transition     |     | 3.1  |     | V                    |
| $V_{GD}$ Short OK Threshold     | $V_{DG\_OK}$     | Startup resumed if $V_G < V_{DG\_OK}$ anytime after postponed                 |     | 3.0  |     | V                    |
| $V_G$ Low Threshold             | $V_G\_TH$        | Latch/Restart if $V_{GD} < V_G\_TH$ after $t_{SSF\_END}$ or $t_{GATE\_FLT}$   |     | 5.4  |     | V                    |
| $V_{OUT}$ Low Threshold         | $V_{OUTL\_TH}$   | Latch/Restart if $V_{OUT} < V_{OUTL\_TH}$ after $t_{SSF\_END}$                |     | 90   |     | % $V_{IN}$           |
| Gate Fault Timer (Note 8)       | $t_{GATE\_FLT}$  | Time from $V_{GD} < V_G\_TH$ transition after $t_{SSF\_END}$ completed        |     | 200  |     | ms                   |
| Startup Timer Failsafe (Note 8) | $t_{SSF\_END}$   | Time from $V_{ON} > V_{SWON}$ transition, Max programmable softstart time     |     | 200  |     | ms                   |
| <b>AUTO-RETRY (NCP81296)</b>    |                  |   |     |      |     |                      |
| Auto-Retry Delay                | $t_{DLY\_RETRY}$ | Delay from power-down to retry of startup                                     |     | 1000 |     | ms                   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

# NCP81295, NCP81296

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$

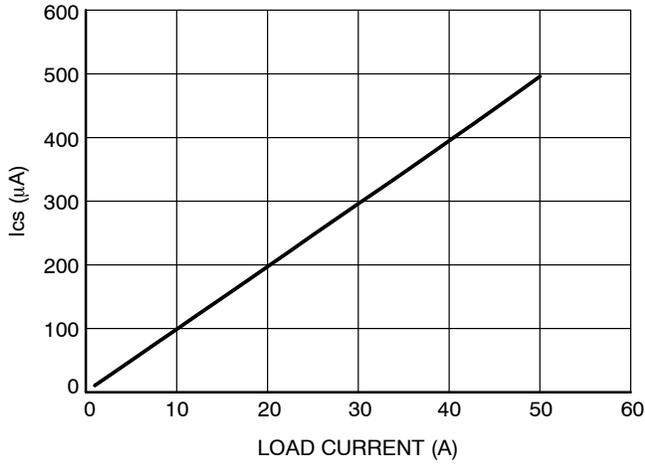


Figure 9. Ics vs. Load Current

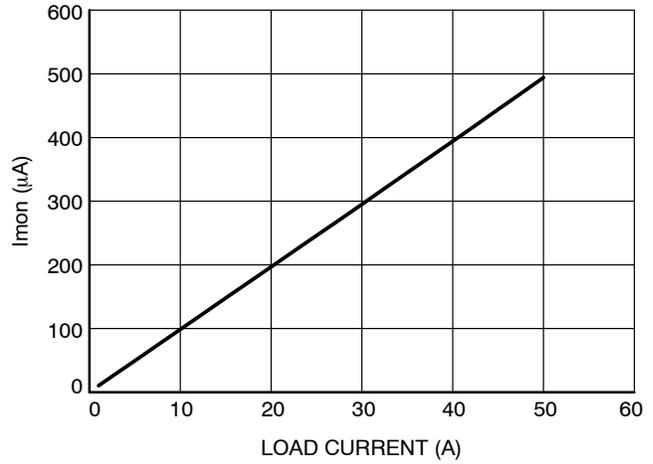


Figure 10. Imon vs. Load Current

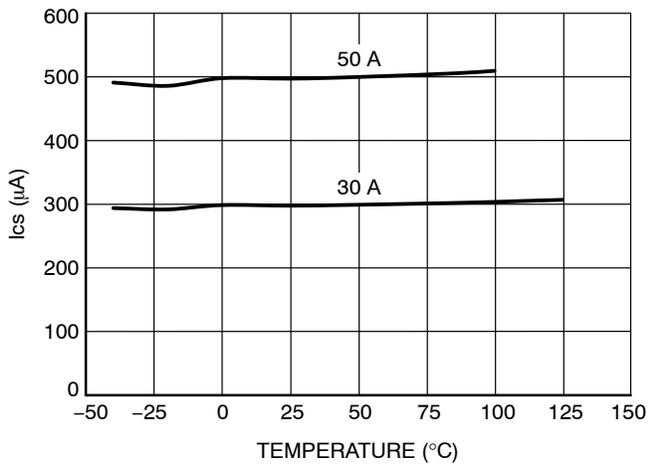


Figure 11. Ics vs. Temperature

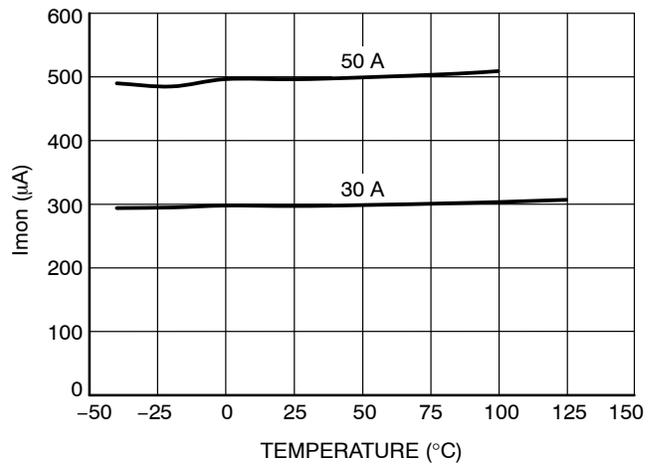


Figure 12. Imon vs. Temperature

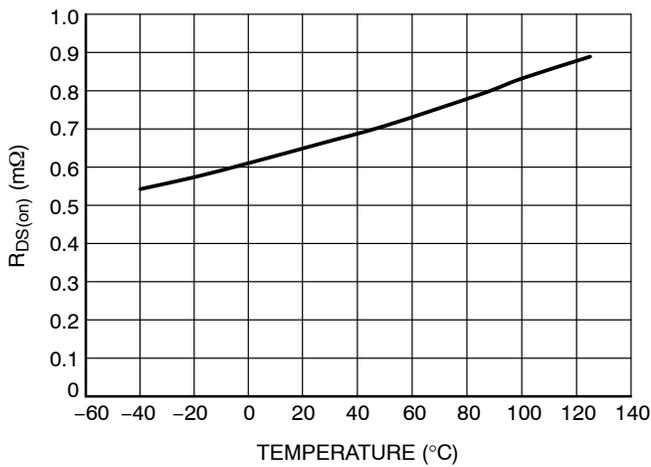


Figure 13. Output Switch  $R_{DS(on)}$  @ 22 A vs. Temperature

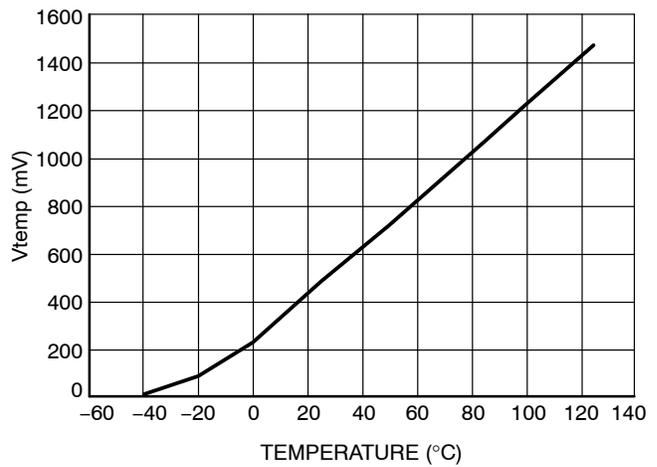
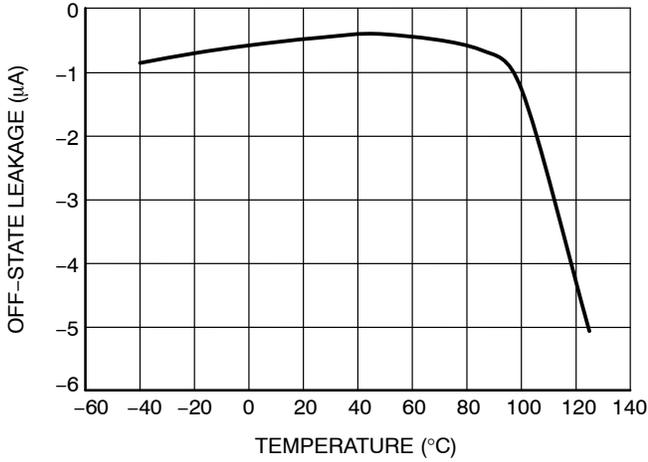


Figure 14. Vtemp vs. Temperature (no load)

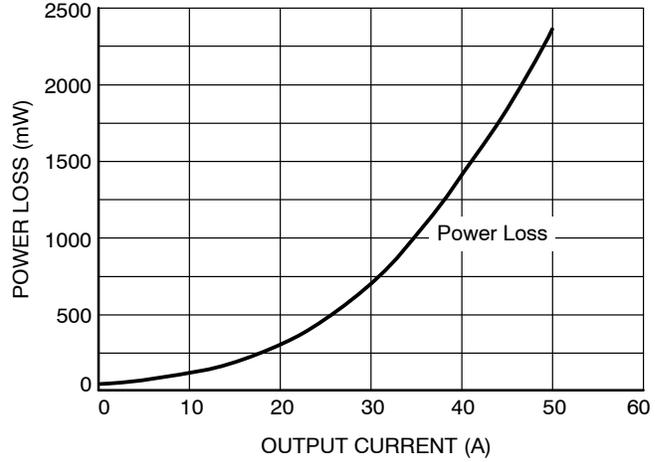
# NCP81295, NCP81296

## TYPICAL CHARACTERISTICS

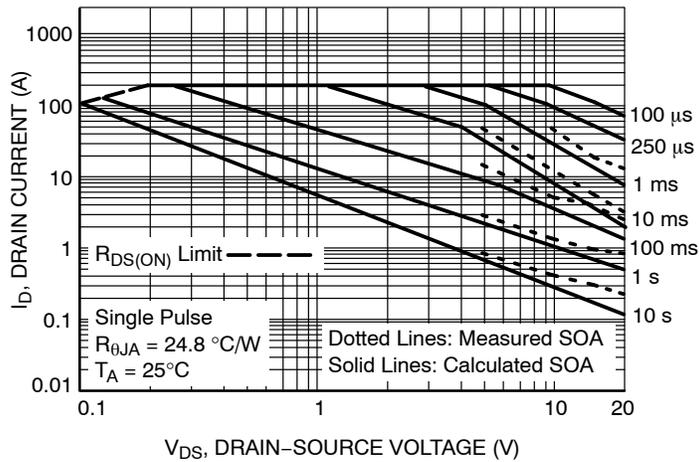
Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$



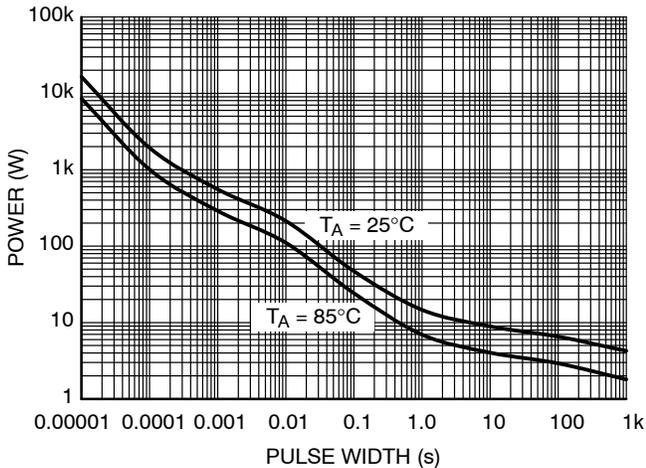
**Figure 15. Output Switch Off-state Leakage vs. Temperature**



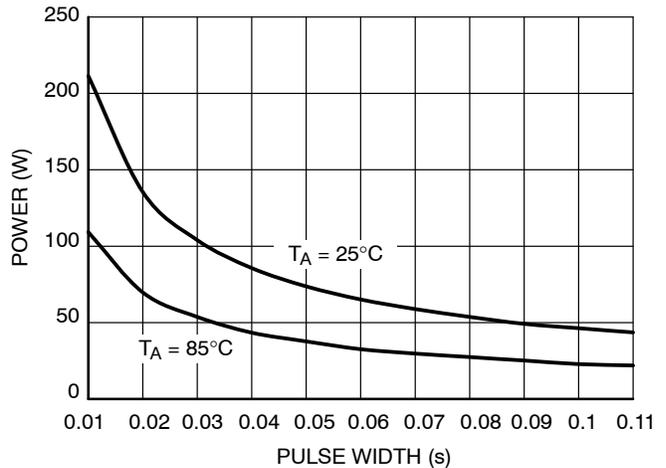
**Figure 16. Power Loss vs. Load Current**



**Figure 17. Internal FET's Safe Operating Area (SOA)**



**Figure 18. Single Pulse Power Rating (10 µs - 1000 s, Junction-to-Ambient, Note 4)**



**Figure 19. Single Pulse Power Rating (10 ms - 110 ms, Junction-to-Ambient, Note 4)**

# NCP81295, NCP81296

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$

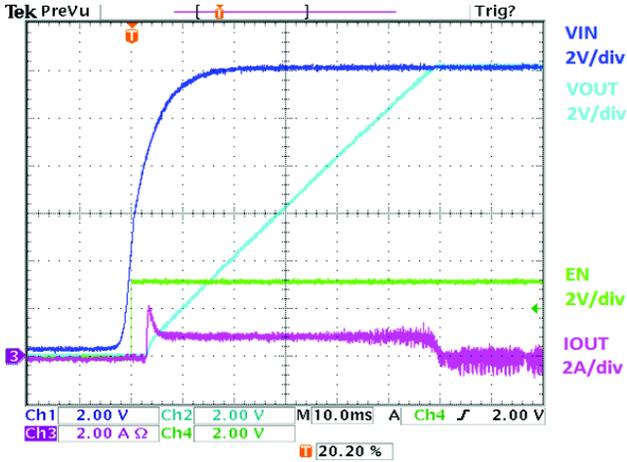


Figure 20. Start Up by VIN (Iout = 0 A)

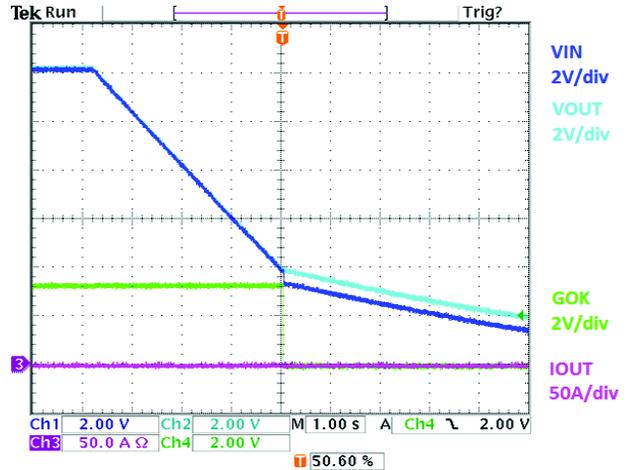


Figure 21. Shut Down by VIN (Iout = 0 A)

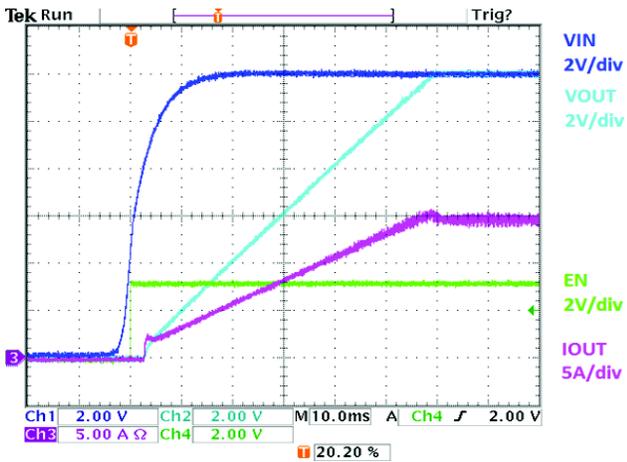


Figure 22. Start Up by VIN (Iout = 15 A)

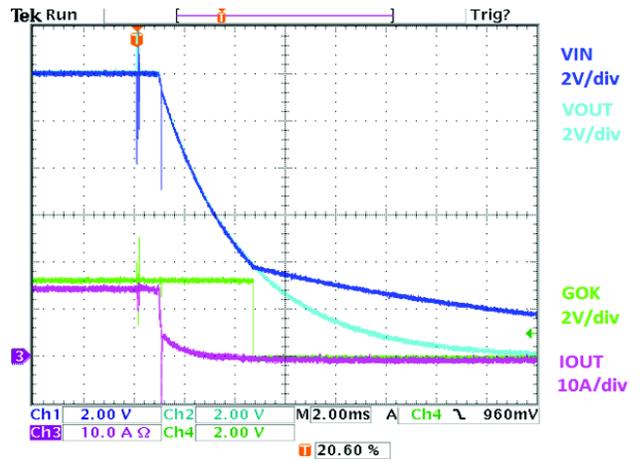


Figure 23. Shut Down by VIN (Iout = 15 A)

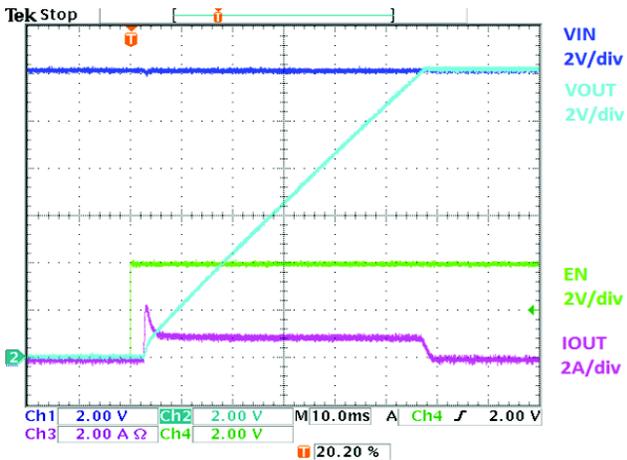


Figure 24. Start Up by EN (Iout = 0 A)

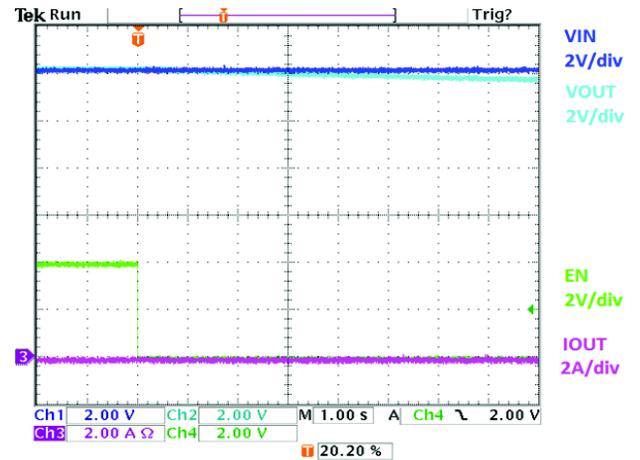


Figure 25. Shut Down by EN (Iout = 0 A)

# NCP81295, NCP81296

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$

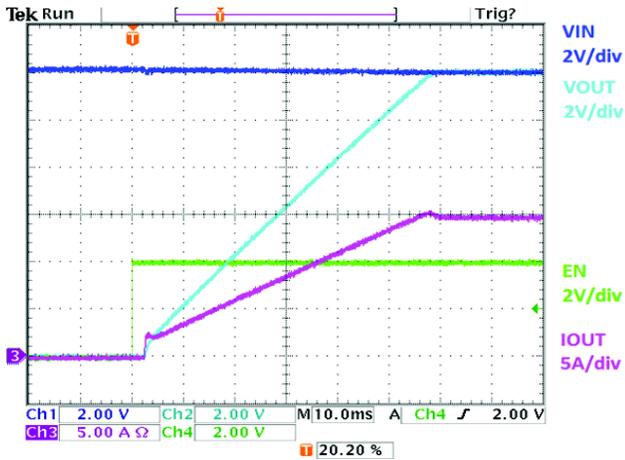


Figure 26. Start Up by EN (Iout = 15 A)

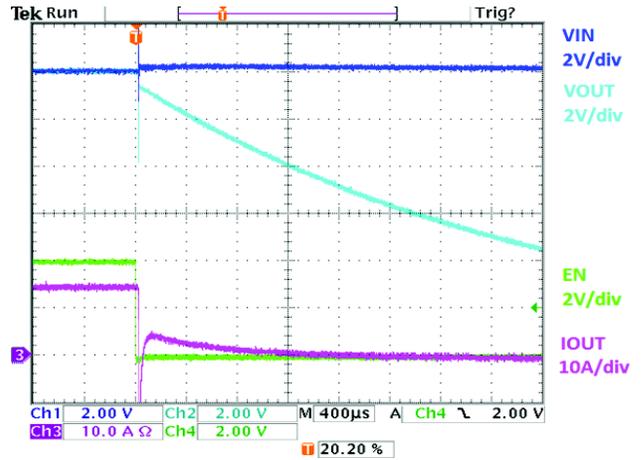


Figure 27. Shut Down by EN (Iout = 15 A)

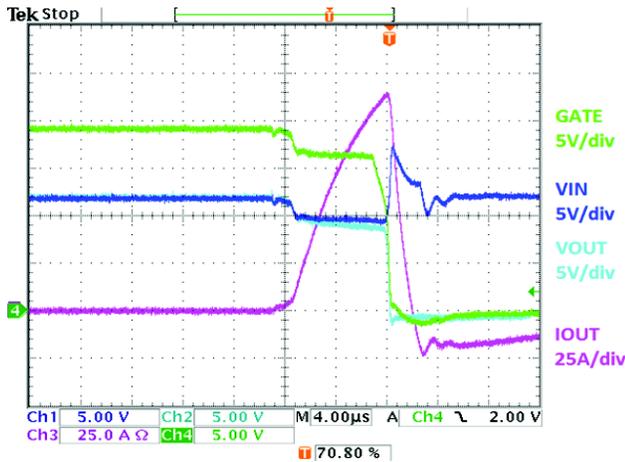


Figure 28. Short Circuit during Normal Operation (Iout = 0 A)

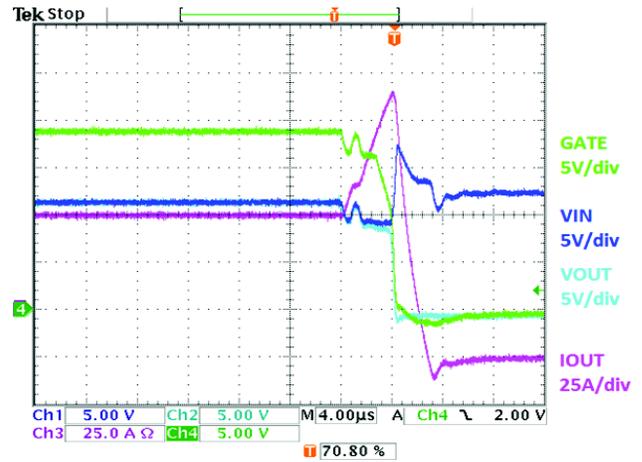


Figure 29. Short Circuit during Normal Operation (Iout = 50 A)

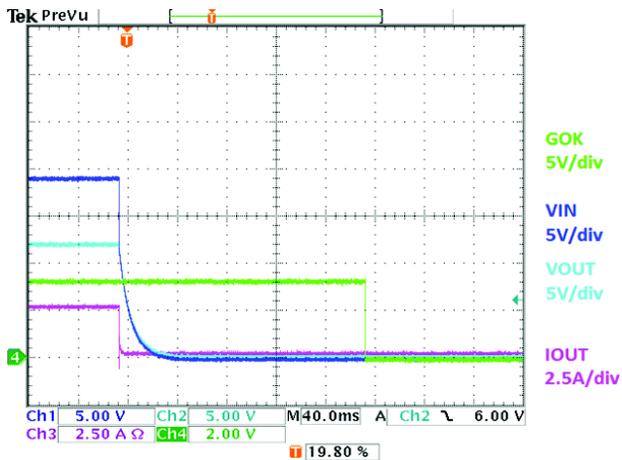


Figure 30. Short FET's Gate During Normal Operation (Iout = 2.5 A)

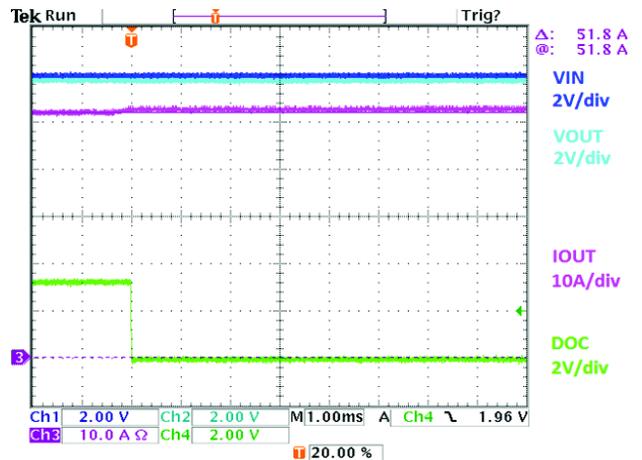


Figure 31. DOC Index for Current Limit during Normal Operation (Iout = 51.8 A)

# NCP81295, NCP81296

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$

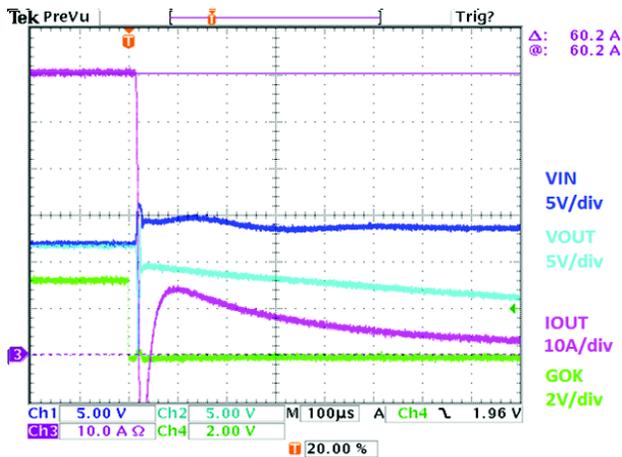


Figure 32. OCP during Normal Operation( $I_{out}=60.2\text{A}$ )

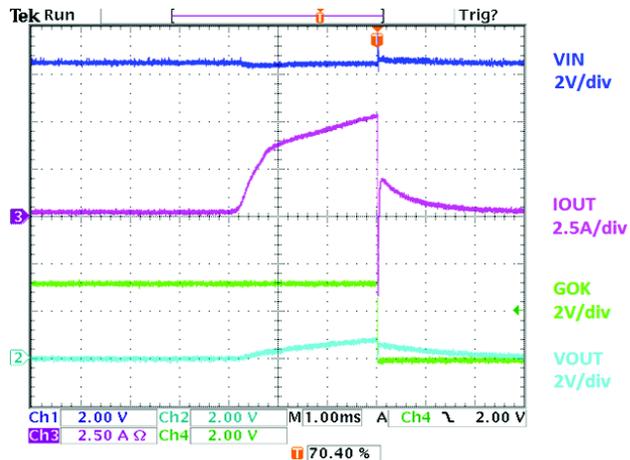


Figure 33. OCP during Power Up by Enable

**General Information**

The NCP81295/6 is an N-channel MOSFET co-packaged with a smart hotswap controller. It is suited for high-side current limiting and fusing in hot-swap applications. It can be used either alone, or in a parallel configuration for higher current applications.

**VDD Output (Auxiliary Regulated Supply)**

An internal linear regulator draws current from the VIN pin to produce and regulate voltage at the VDD pin. This auxiliary output supply is current-limited to  $I_{DD\_CL}$ . A ceramic capacitor in the range of 2.2  $\mu\text{F}$  to 10  $\mu\text{F}$  must be placed between the VDD and GND pins, as close to the NCP81295/6 as possible. The voltage difference between VIN and VIN pin voltage should be within 0.4 V for better CS/IMON performance. Small time constant R/C filter such as 1  $\Omega$ /0.1  $\mu\text{F}$  on the VIN pin is recommended.

**ON Input (Device Enable)**

When the ON pin voltage ( $V_{ON}$ ) is higher than  $V_{SWON}$ , and no undervoltage (UVLO) or output switch faults are present, the output switch turns on. When  $V_{ON}$  is lower than  $V_{SWOFF}$ , the output switch is off. If  $V_{ON}$  is between  $V_{PDOFF}$  and  $V_{SWOFF}$  for longer than  $t_{PD\_DEL}$ , the output switches off, and a pull-down resistance to ground, of  $R_{PD}$ , is applied to VOUT. In other words, there is behavior as follows:

- When  $V_{ON} < 0.8\text{ V}$ , FET turns off.
- When  $0.8\text{ V} < V_{ON} < 1.2\text{ V}$ , VOUT will discharge with  $\sim 15\text{ mA}$ .
- When  $V_{ON} > 1.2\text{ V}$ , FET turns on.

For standalone applications, the ON pin sources current  $I_{ON}$ , which can be used to delay output switch turn-on for some time after the appearance of input voltage by connecting a capacitor from the ON pin to ground.

A bi-level control signal driving to ground can be biased up with a resistive divider to produce ON input levels between  $V_{PDOFF} < V_{ON} < V_{SWON}$  and  $V_{ON} > V_{SWON}$  in order to always apply the output pull-down when the output switch is off.

**SS Output (Soft-Start)**

When the output switch first turns on, it does so in a controlled manner. The output voltage (VOUT) follows the voltage at the SS pin, produced by current  $I_{SS}$  into a capacitor from SS to ground. The duration of soft-start can be programmed by selection of the capacitor value. In parallel fuse applications, the SS pins of all fuses should be shorted together to one shared SS capacitor. Internal soft-start load balancing circuitry will ensure the soft-start current is shared between paralleled devices, so as not to stress one device more than another or hit a soft start-current limit.

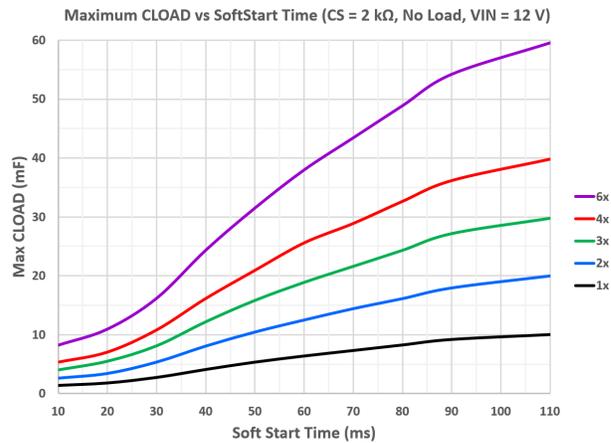
The soft-start capacitor value can be calculated by:

$C_{SS} = (t_{SS} * I_{SS} * AV_{SS})/V_{IN}$  (where  $t_{SS}$  is the target soft-start time). The recommended range of  $t_{SS}$  is 10 – 110 ms (see Table 5).

The typical  $C_{SS}$  values for different  $t_{SS}$  are listed below:

| $C_{SS}$ (nF) | $t_{SS}$ (ms) | $C_{SS}$ (nF) | $t_{SS}$ (ms) |
|---------------|---------------|---------------|---------------|
| 47            | 11            | 180           | 41            |
| 68            | 15            | 220           | 51            |
| 82            | 19            | 270           | 62            |
| 100           | 23            | 330           | 76            |
| 120           | 28            | 390           | 90            |
| 150           | 35            | 470           | 110           |

The maximum load capacitor value NCP81295/6 can power up depends on the device soft-start time. When  $V_{IN} = 12\text{ V}$ ,  $R_{CS} = 2\text{ k}\Omega$ , no load, their relationship for different paralleled operations are shown as below chart (above line device shuts down safely due to protection, below line device powers up successfully without trigger protection):



**GOK Output (Gate OK)**

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

- $V_{DD}$  voltage is below UVLO voltage at any time.
- $V_{ON}$  disabled and  $V_{DS\_OK}$  is false (indicates a short from  $\bar{V}_{IN}$  to VOUT).
- $V_{ON}$  disabled and  $V_{DG\_OK}$  is false (indicates a short from GATE to VIN).
- $V_{ON}$  enabled and  $V_{SS\_OK}$  is false at  $t_{SSF\_END}$  (indicates  $V_{OUT} < 90\%$  after soft-start completes – FET latches off for NCP81295/auto-retries for NCP81296).
- $V_{ON}$  enabled and  $V_G$  is below  $V_{G\_TH}$  at  $t_{SSF\_END}$  (indicates leakage on GATE in startup – FET latches off for NCP81295/auto-retries for NCP81296).
- $V_{ON}$  enabled and  $V_G$  is below  $V_{G\_TH}$  after  $t_{GATE\_FLT}$  (indicates leakage on GATE during normal operation – FET latches off for NCP81295/auto-retries for NCP81296).
- $V_{ON}$  enabled and a current-limiting condition lasts longer than  $t_{OC\_LA}$  (FET latches off for NCP81295/auto-retries for NCP81296).

- $V_{ON}$  enabled and device temperature is above  $T_{TSD}$  (indicates an over-temperature is detected – FET latches off for NCP81295/auto-retries for NCP81296).

Usually GOK can't be used as power good to indicate the output voltage is in the normal range. Bringing VDD below the UVLO voltage is required to release a latching condition.

### IMON Output (Current Monitor)

The IMON pin sources a current that is  $A_{IMON}$  (10  $\mu$ A/A) times the VOUT output current and plus  $I_{AZ\_BIAS}$ . A resistor connected from the IMON pin to ground can be used to monitor current information as a voltage up to  $V_{IM\_CLMP}$ . A capacitor of any value in parallel with the IMON resistor can be used to low-pass filter the IMON signal without affecting any internal operation of the device.

### CLREF Pin (Current Limit and Over-Current Reference)

The CLREF pin voltage determines the current-limit regulation point and over-current indication point via its interaction with the CS pin voltage. The CLREF voltage can be applied by an external source, such as a hot-swap controller or D-to-A converter, or developed across a programming resistor to ground by the CLREF bias current,  $I_{CL}$ . The recommended range of CLREF voltage is 0.2 – 1.4 V (see Table 5).

### CS Input/Output (Current Set)

The CS pin is both an input and an output. The CS pin sources a current that is  $A_{CS}$  (10  $\mu$ A/A) times the VOUT current and plus  $I_{AZ\_BIAS}$ . This produces a voltage on the CS pin that is the product of the CS pin current and an external CS pin resistance to ground.

The voltage generated on  $V_{CS}$  determines the  $D\_OC$  over-current indicator trip point and the current-limit regulation point, via its interaction with the voltage on CLREF pin.

When the voltage on the CS pin is higher than  $V_{OC\_TH}$ ,  $D\_OC$  is pulled low. If the CS pin voltage drops below  $V_{OC\_TH}$ , the  $D\_OC$  pin is released to and gets pulled high by the external pullup resistor.  $D\_OC$  transitions based on the following formula:

$$I_{OUT} = \frac{\frac{V_{OC\_TH} + V_{ENACT}}{R_{CS}} - I_{AZ\_BIAS}}{10 \mu} \quad (\text{eq. 1})$$

The  $V_{OC\_TH}$  trip point is based on a percentage of  $V_{CLREF}$  (86%).

During normal operation ( $V_{ON} > V_{SWON}$  for longer than  $t_{SS\_END}$ ), if the voltage on the CS pin is above  $V_{CL\_TH}$  ( $V_{CL\_TH}$  is clamped at  $V_{CL\_MX}$  if  $V_{CL\_TH} > V_{CL\_MX}$ ), then the gate voltage of the FET is modulated to limit current into the output based on the following formula:

$$I_{OUT} = \frac{\frac{V_{CL\_TH} + V_{ENACT}}{R_{CS}} - I_{AZ\_BIAS}}{10 \mu} \quad (\text{eq. 2})$$

The  $V_{CL\_TH}$  regulation point is equal to  $V_{CLREF}$ .

During startup ( $V_{ON} > V_{SWON}$  for less than  $t_{SS\_END}$ ), the current limit reference voltage is clamped according to the following:

- When  $V_{OUT} < 40\%$  of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_LO}$  or  $V_{CLREF}$  (whichever is lower).
- When  $V_{OUT}$  is between 40% and 80% of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_HI}$  or  $V_{CLREF}$  (whichever is lower).
- When  $V_{OUT}$  exceeds 80% of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_MX}$  or  $V_{CLREF}$  (whichever is lower).

If a current limiting condition exists anytime for a continuous duration  $> t_{CL\_LA}$ , then the device latches off (NCP81295) or restarts (NCP81296).

The CS pin must have no capacitive loading other than parasitic device/board capacitance to function correctly. The recommended range of  $R_{CS}$  is 1.8 – 4  $k\Omega$  (see Table 5).

### CS AMP OFFSET BIAS

NCP81295/6 use an auto-zero Op-Amp with low input offset to sense current in FET with high-accuracy, and an pre-biased offset current load,  $I_{AZ\_BIAS}$  is need for this Op-Amp to always keep it to maintain this low input offset ( $< 100 \mu$ V). The internal IMON and CS current source follow below relationship:

$$I_{OUT} = \frac{I_{CS} - I_{AZ\_BIAS}}{10 \mu} \quad (\text{eq. 3})$$

and

$$I_{OUT} = \frac{I_{MON} - I_{AZ\_BIAS}}{10 \mu} \quad (\text{eq. 4})$$

For typical 5  $\mu$ A  $I_{AZ\_BIAS}$ , there has 0.5 A positive off-set in  $I_{OUT}$  sense.

### D\_OC Output (Over-current Indicator)

The  $D\_OC$  pin is an open-drain output that indicates when an over-current condition exists after soft-start is complete. When the voltage on the CS pin is higher than  $V_{OC\_TH}$ ,  $D\_OC$  is pulled low. If output current drops below  $V_{OC\_TH}$ , the  $D\_OC$  pin is released and gets pulled high by an external pullup resistor.

### VTEMP Output (Temperature Indicator)

VTEMP is a voltage output proportional to device temperature, with an offset voltage. The VTEMP output can source much more current than it can sink, so that if multiple VTEMP outputs are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest NCP81295/6. A 100 nF capacitor or greater must be connected from the VTEMP pin to ground.

## Auto-Retry Restart (NCP81296)

Under certain fault conditions, the FET is turned off and another soft-start procedure takes place. Between the fault and the new soft-start, there is a delay of  $t_{DLY\_RETRY}$ . The protection features that use this hiccup mode restart are:

- Over-Current
- Short-Circuit Detection
- Over-Temperature
- Excessive Soft-Start Duration
- Gate Leakage

## Protection Features

For the following protection features, the FET either latches off (NCP81295) or the FET turns off and initiates a restart (NCP81296), unless noted otherwise.

### Excessive Current Limiting

If a current limiting condition exists anytime for a continuous duration  $> t_{CL\_LA}$ , then the FET latches/restarts.

### Excessive Soft-Start Duration

If  $V_{OUT} < V_{OUTL\_TH}$  when  $t_{SSF\_END}$  expires, then the FET latches/restarts.

### Short Circuit Detection

If switch current exceeds  $I_{SC}$ , the device reacts within  $t_{SC}$ , and the FET latches/restarts. The short-circuit current monitor is independent of CS, CLREF, IMON and current limit setting (cannot be changed externally).

### Over-Temperature Shutdown

If the FET controller temperature  $> T_{TSD}$ , then the FET latches/restarts.

## FET Fault Detection

The device contains various FET monitoring circuits:

- VIN to VOUT short, non-latching/non-auto-retry condition. If the device is disabled and  $V_{OUT} > V_{DS\_TH}$  then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once  $V_{OUT} < V_{DS\_OK}$ .
- GATE to VIN short, non-latching/non-auto-retry condition. If the device is disabled and  $GATE (Pin 8) > V_{DG\_TH}$ , then GOK is pulled low and device is prevented from powering up. The device allowed to power up once  $GATE < V_{DG\_OK}$ .
- GATE leakage – startup.  
If  $(GATE - V_{INF}) < V_{G\_TH}$  at  $t_{SSF\_END}$ , then GOK is pulled low and FET latches/restarts.
- GATE leakage – normal operation.  
If  $(GATE - V_{INF}) < V_{G\_TH}$  for  $t_{GATE\_FLT}$  time after the soft-start timer completes, then GOK is pulled low and device latches/restarts.

## FET SOA Limits

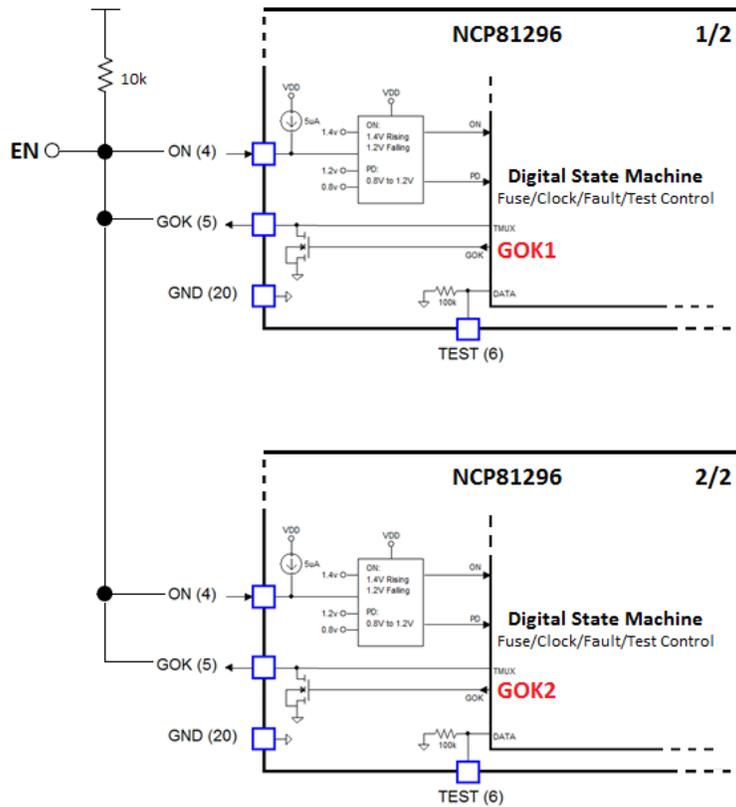
In-built timed current limits and fault-monitoring circuits ensure the copackaged FET is always kept within SOA limits.

## Multiple Fuse Power Up

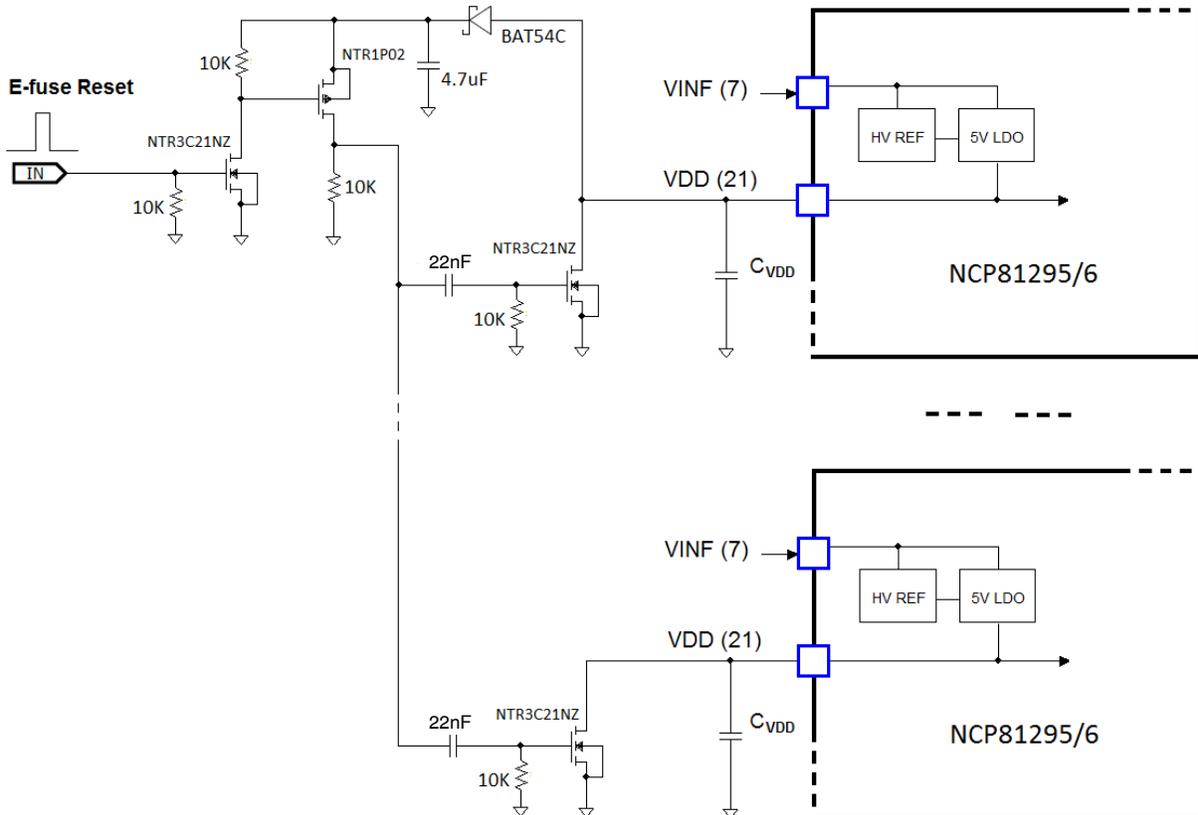
When multiple NPC81295 are paralleled together as shown in Figure 4, the NPC81295s will turn on together.

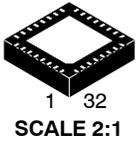
**Due to NCP81296 is featured by Auto-Retry Mode protection, please follow the below reference schematic of NCP81296 for paralleled operation.**

# NCP81295, NCP81296



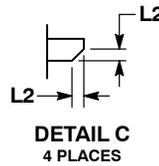
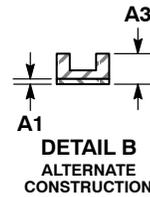
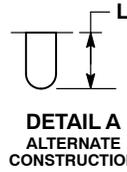
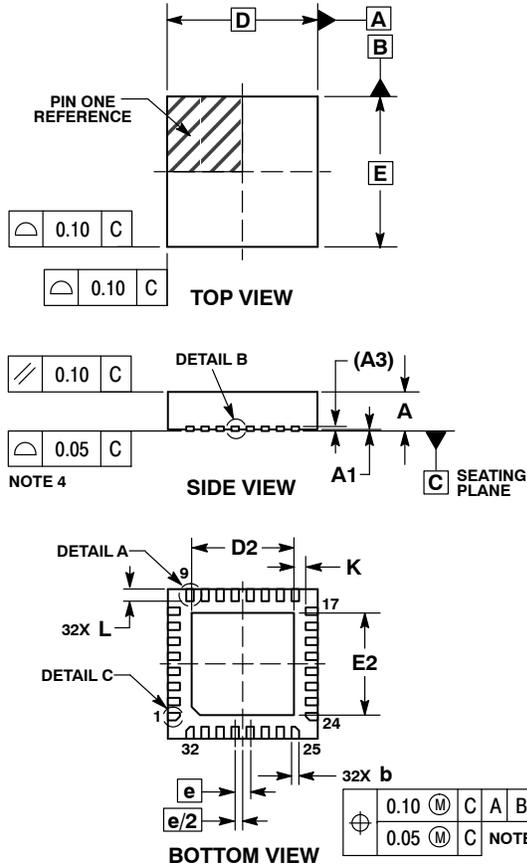
When paralleled multiple NCP81295 encounter fault, the system can recover the E-fuse by resetting their VDD with below buffer and reset circuit.





LQFN32 5x5, 0.5P  
CASE 487AA  
ISSUE A

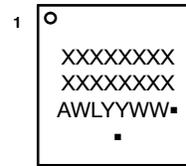
DATE 03 OCT 2017



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  - CONTROLLING DIMENSION: MILLIMETERS.
  - DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
  - COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 1.20 | 1.40 |
| A1          | ---  | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.18 | 0.30 |
| D           | 5.00 | BSC  |
| D2          | 3.30 | 3.50 |
| E           | 5.00 | BSC  |
| E2          | 3.30 | 3.50 |
| e           | 0.50 | BSC  |
| L           | 0.30 | 0.50 |
| L2          | 0.13 | REF  |

GENERIC  
MARKING DIAGRAM\*

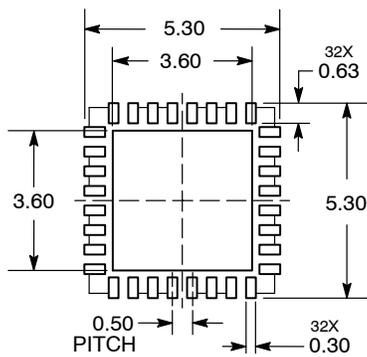


- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED  
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                   |  |
|------------------|-------------------|--|
| DOCUMENT NUMBER: | 98AON11454G       | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | LQFN32, 5x5, 0.5P | PAGE 1 OF 1  |

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[NCP81295MNTXG](#) [NCP81296MNTXG](#)