

# MOSFET - Power, DUAL COOL® N-Channel, DFN8 5x6 40 V, 0.87 mΩ, 310 A

## NVMFSC0D9N04C

### Features

- Advanced Dual-sided Cooled Packaging
- Small Footprint (5x6 mm) for Compact Design
- Ultra Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant
- MSL1 Robust Packaging Design

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	40	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	313	A
Power Dissipation $R_{\theta JC}$ (Note 2)			$P_D$	166	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	48.9	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			$P_D$	4.1	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	900	A	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	°C	
Source Current (Body Diode)		$I_S$	158	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 34 \text{ A}$ )		$E_{AS}$	578	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	300	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

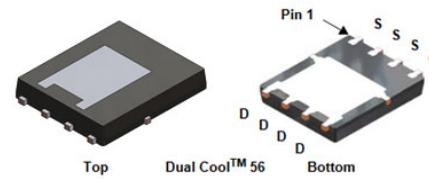
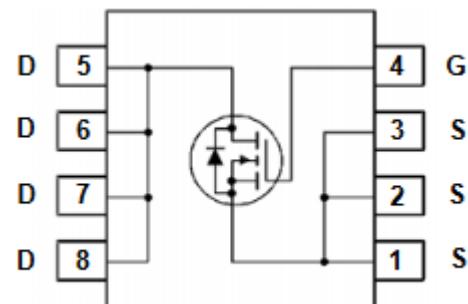
### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Bottom) – Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction-to-Case (Top) – Steady State (Note 2)	$R_{\theta JC}$	1.4	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	37	

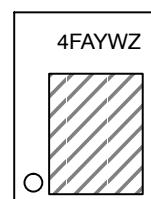
- Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.87 mΩ @ 10 V	310 A

### N-Channel MOSFET



### MARKING DIAGRAM



4F = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 Z = Assembly Lot Code

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMFSC0D9N04C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25°C		10	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20 V			100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.5		3.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		-8.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 50 A	0.69	0.87	mΩ

### CHARGES & CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		6100		pF
Output Capacitance	C <sub>OSS</sub>			3400		
Reverse Transfer Capacitance	C <sub>RSS</sub>			70		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V; I <sub>D</sub> = 50 A		86		nC
Gate-to-Source Charge	Q <sub>GS</sub>			28		
Gate-to-Drain Charge	Q <sub>GD</sub>			14		
Plateau Voltage	V <sub>GP</sub>			4.9		V

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 50 A, R <sub>G</sub> = 2.5 Ω		54		ns
Rise Time	t <sub>r</sub>			160		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			220		
Fall Time	t <sub>f</sub>			170		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 50 A			91		ns
Charge Time	t <sub>a</sub>				42		
Discharge Time	t <sub>b</sub>				49		
Reverse Recovery Charge	Q <sub>RR</sub>				159		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

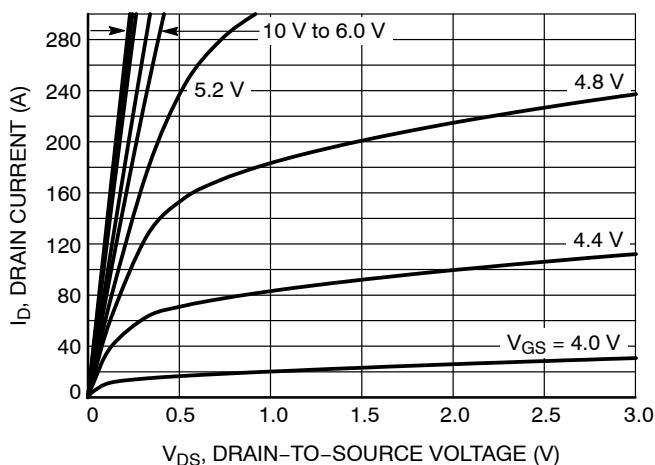


Figure 1. On-Region Characteristics

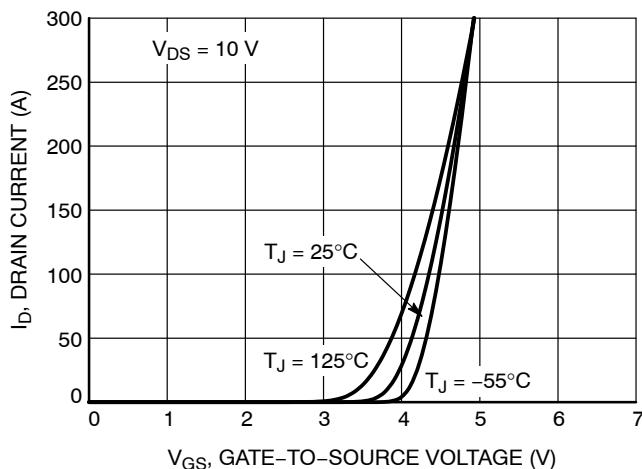


Figure 2. Transfer Characteristics

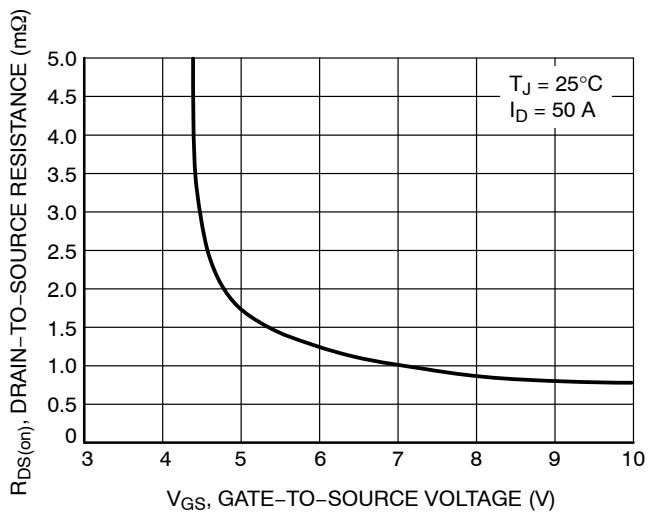


Figure 3. On-Resistance vs. Gate-to-Source Voltage

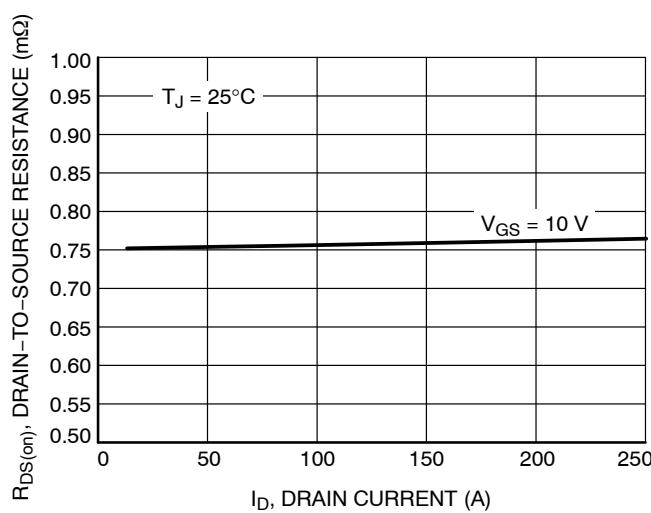


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

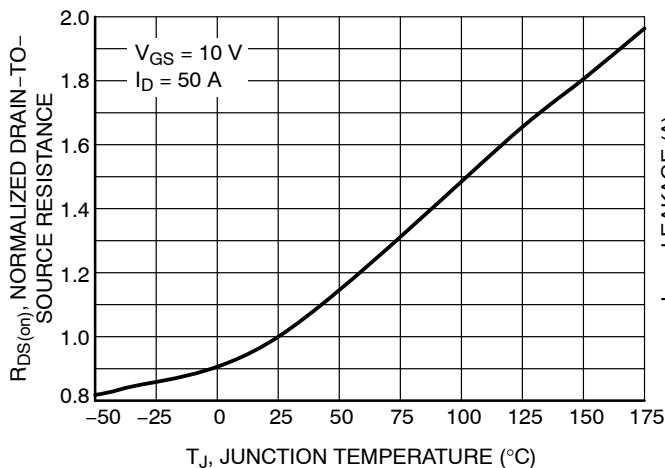


Figure 5. On-Resistance Variation with Temperature

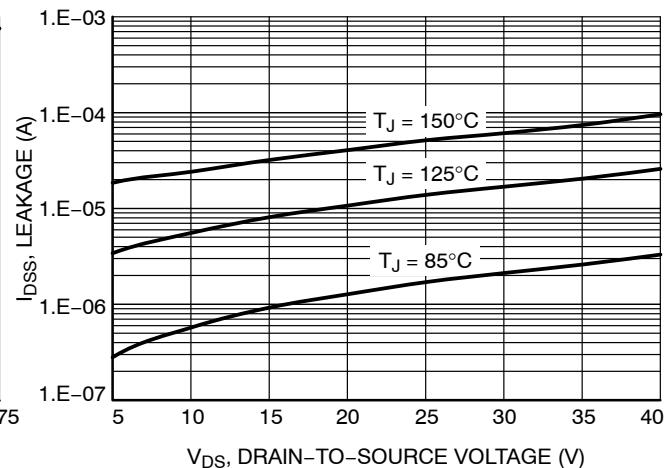
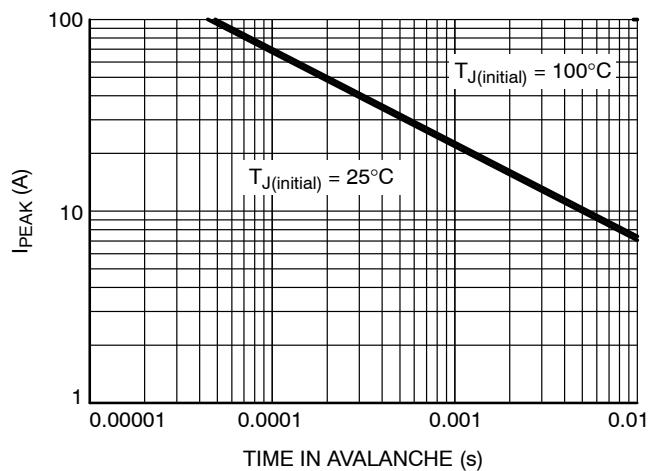
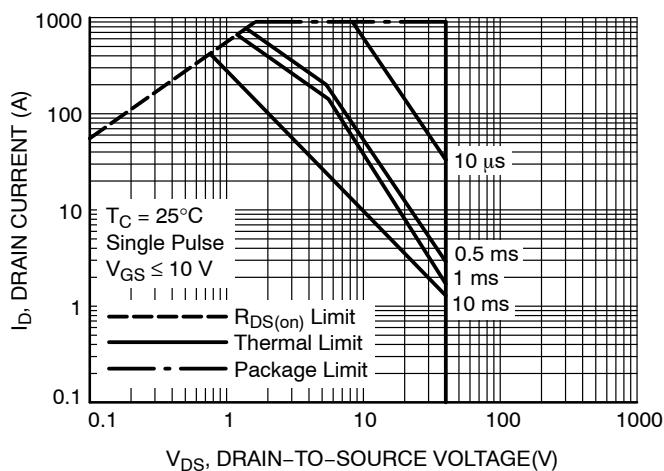
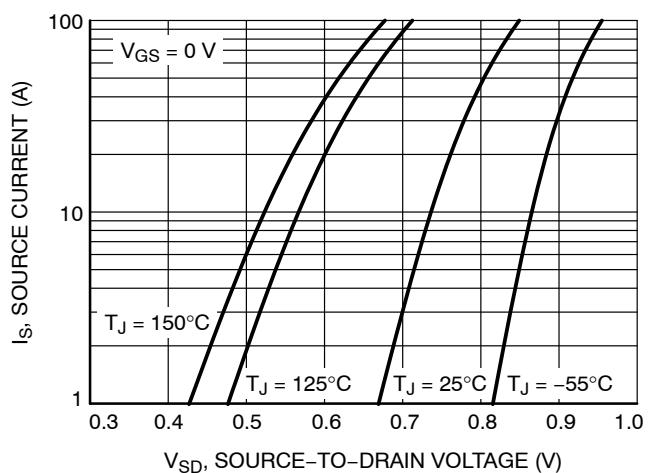
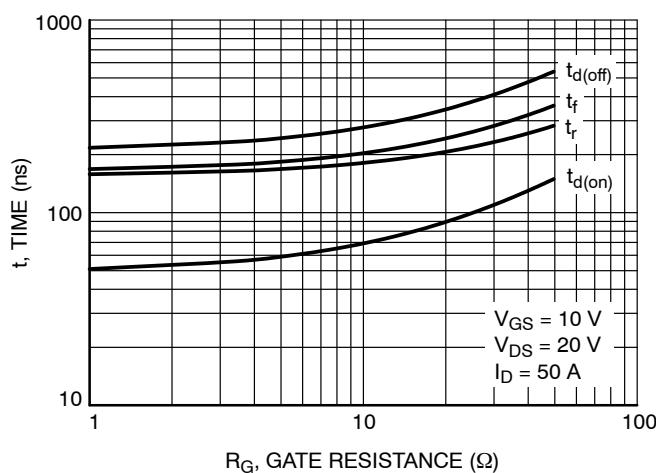
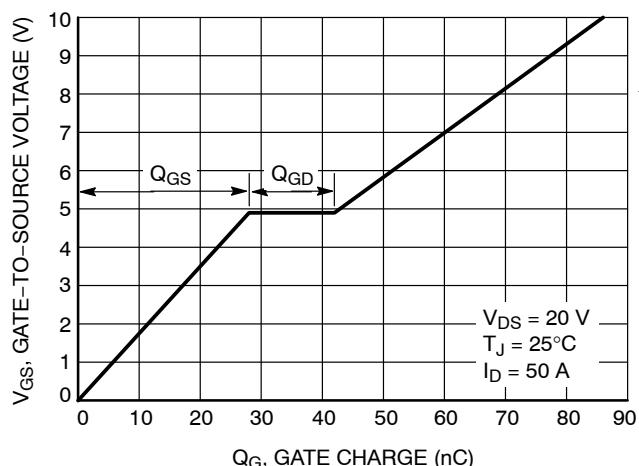
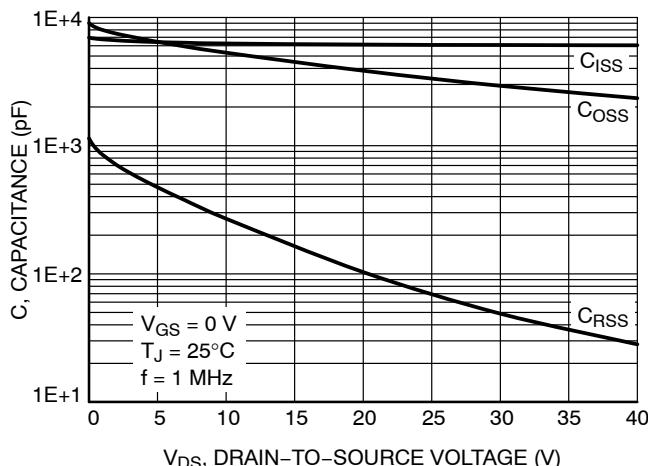
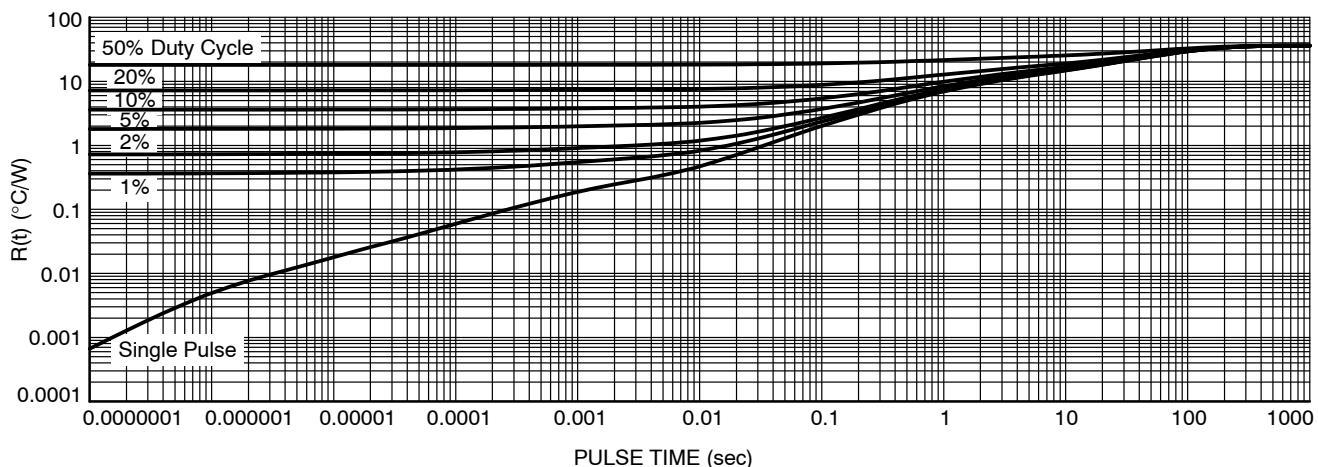


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS****Figure 13. Thermal Characteristics****ORDERING INFORMATION**

Device	Device Marking	Package	Shipping <sup>†</sup>
NVMFSC0D9N04C	4F	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

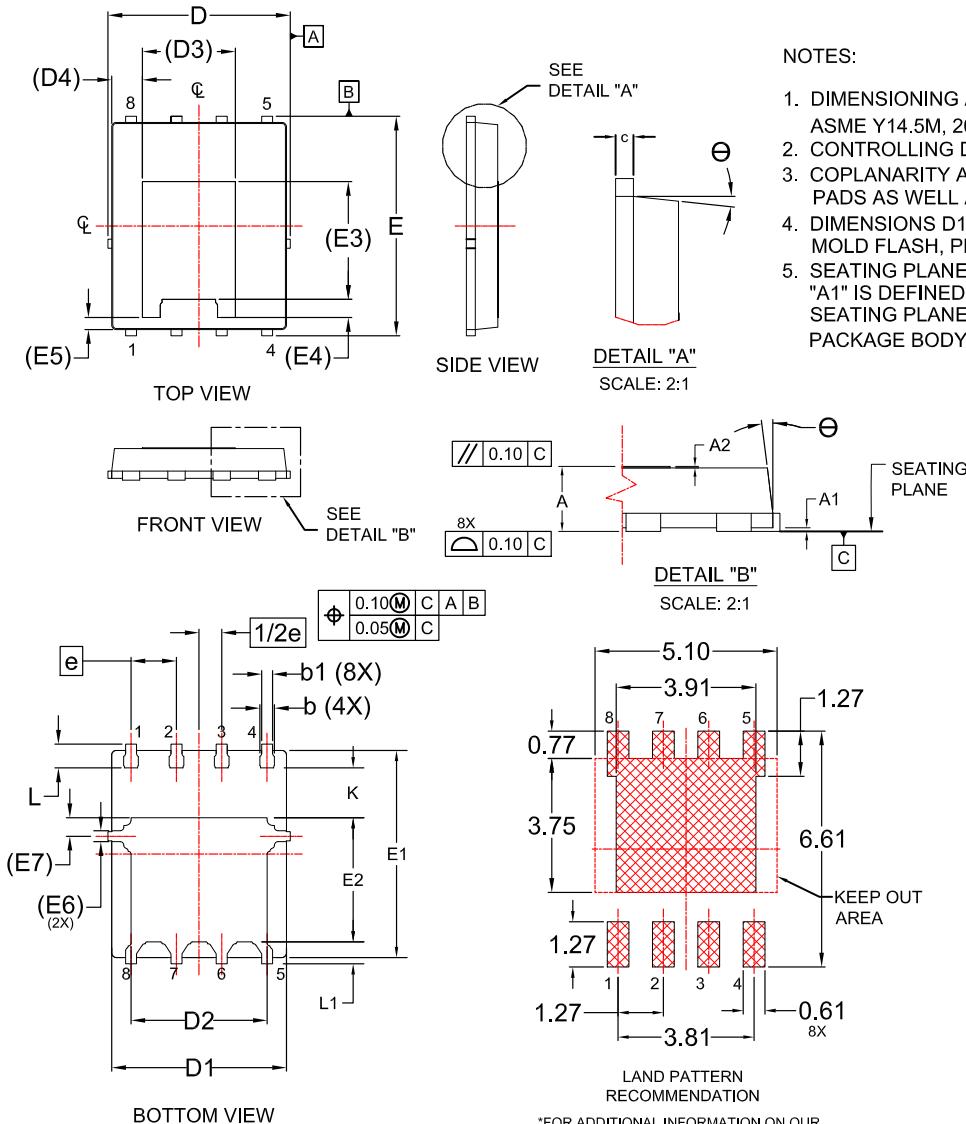
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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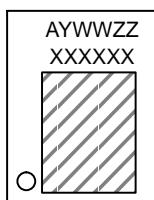


**DFN8 5x6.15, 1.27P, DUAL COOL**  
CASE 506EG  
ISSUE D

DATE 25 AUG 2020



**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SODERRM/D.

\*This information is generic. Please refer to  
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