

## MOSFET – Power, Single, N-Channel

**80 V, 9.5 mΩ, 68 A**

## NVTFS6H850N

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFS6H850NWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	80	V
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Notes 1, 2, 3, 4)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	68
		T <sub>C</sub> = 100°C		48
		T <sub>C</sub> = 25°C	P <sub>D</sub>	107
		T <sub>C</sub> = 100°C		53
Continuous Drain Current R <sub>θJA</sub> (Notes 1 & 3, 4)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	11
		T <sub>A</sub> = 100°C		8.4
		T <sub>A</sub> = 25°C	P <sub>D</sub>	3.2
		T <sub>A</sub> = 100°C		1.6
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	300	A
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)		I <sub>S</sub>	89	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 3.4 A)		E <sub>AS</sub>	271	mJ
Lead Temperature for Soldering Purposes (1/8" from Case for 10 s)		T <sub>L</sub>	260	°C

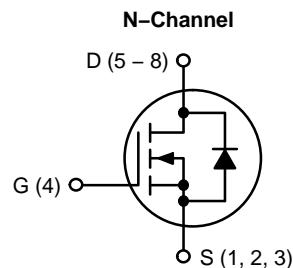
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

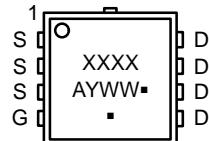
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	R <sub>θJC</sub>	1.4	°C/W
Junction-to-Ambient – Steady State (Note 3)	R <sub>θJA</sub>	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
80 V	9.5 mΩ @ 10 V	68 A



### MARKING DIAGRAM



XXXX = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVTFS6H850N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V			10	μA
		T <sub>J</sub> = 25°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 70 μA	2.0		4.0	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		8.5	9.5	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		63		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 40 V		1140		pF
Output Capacitance	C <sub>oss</sub>			175		
Reverse Transfer Capacitance	C <sub>rss</sub>			10		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 10 A		3.6		nC
Gate-to-Source Charge	Q <sub>GS</sub>			6.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.7		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 10 A		19		nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 6.0 V, V <sub>DS</sub> = 64 V, I <sub>D</sub> = 10 A		11		ns
Rise Time	t <sub>r</sub>			32		
Turn-Off Delay Time	t <sub>d(off)</sub>			34		
Fall Time	t <sub>f</sub>			8.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 10 A			40		ns
Charge Time	t <sub>a</sub>				24		
Discharge Time	t <sub>b</sub>				16		
Reverse Recovery Charge	Q <sub>RR</sub>				40		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

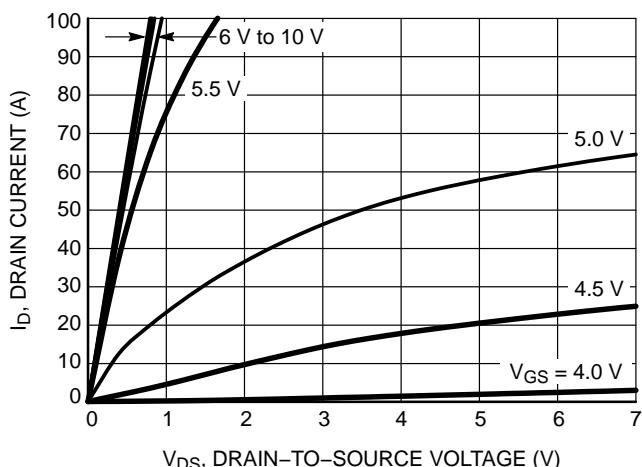


Figure 1. On-Region Characteristics

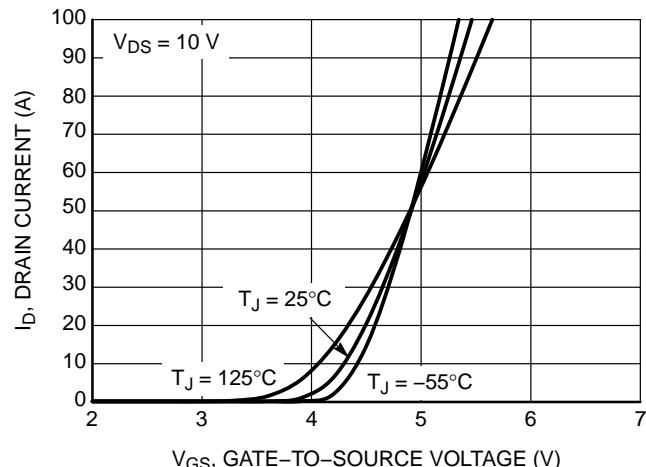


Figure 2. Transfer Characteristics

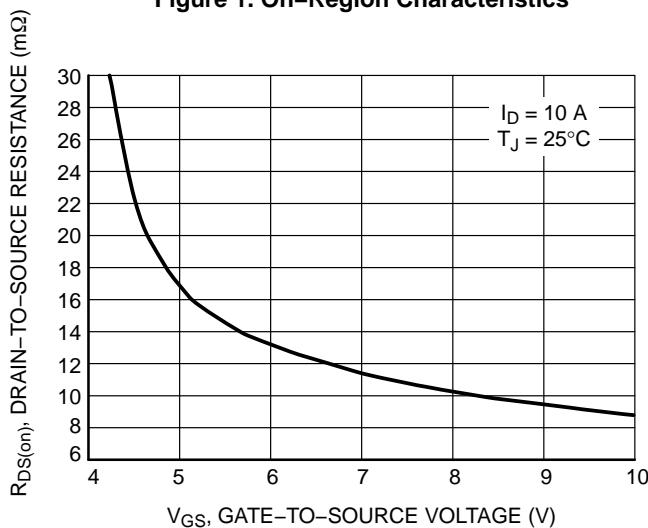


Figure 3. On-Resistance vs. Gate-to-Source Voltage

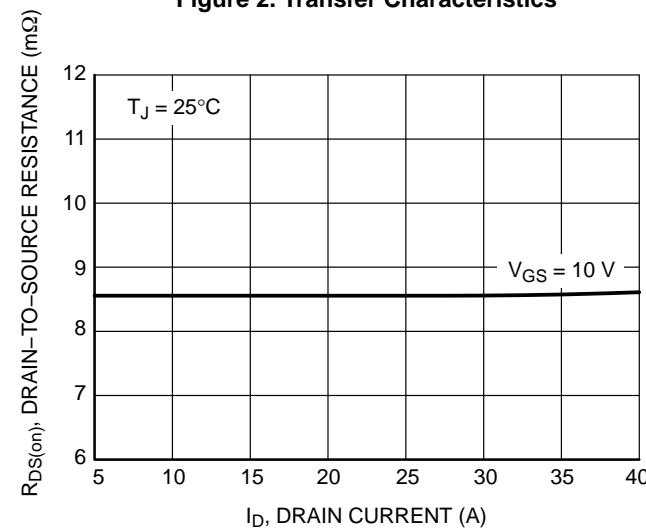


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

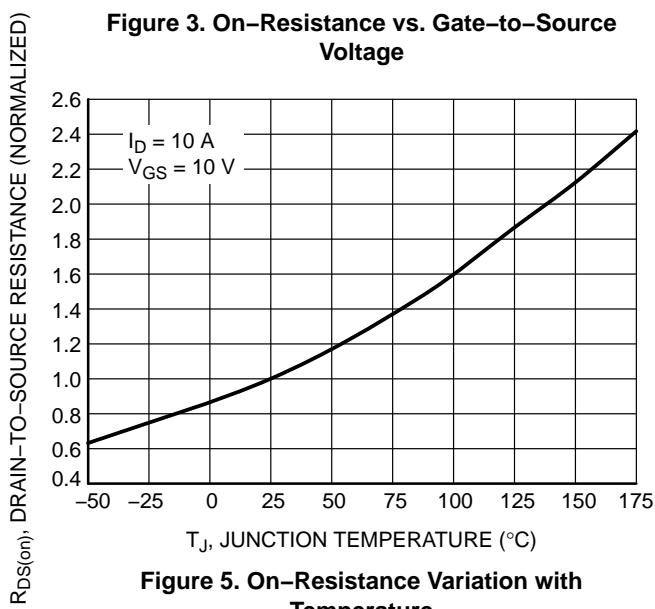


Figure 5. On-Resistance Variation with Temperature

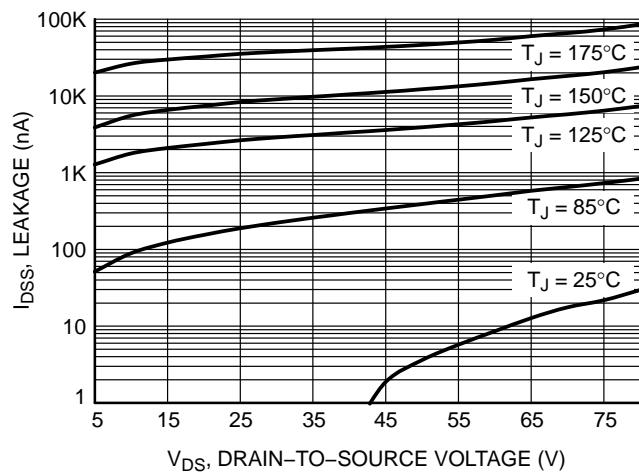


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

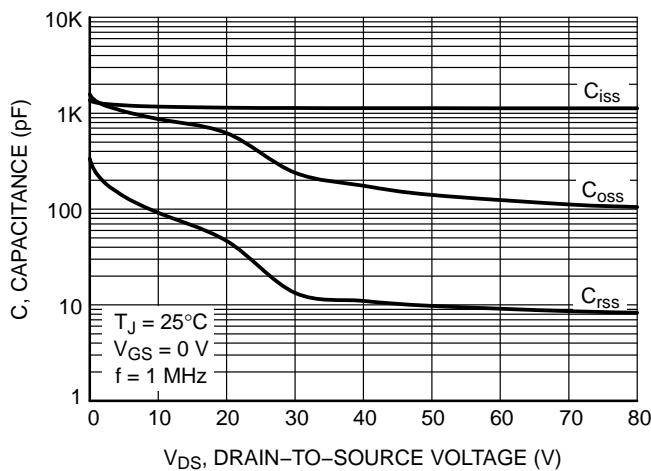


Figure 7. Capacitance Variation

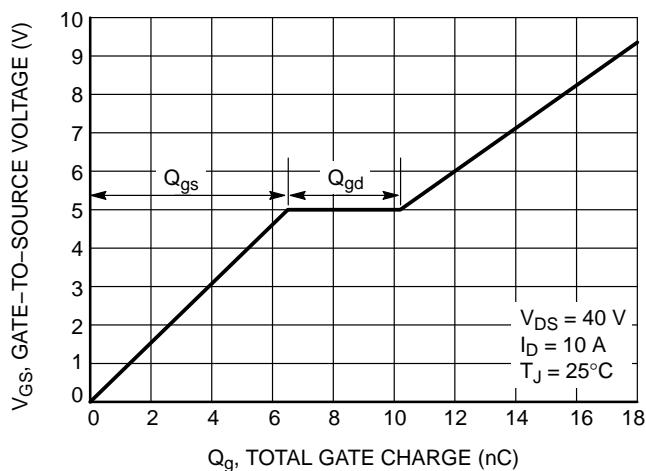


Figure 8. Gate-to-Source vs. Total Charge

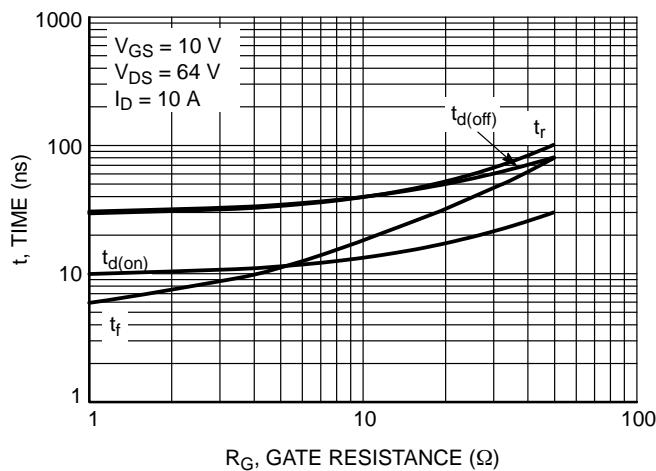


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

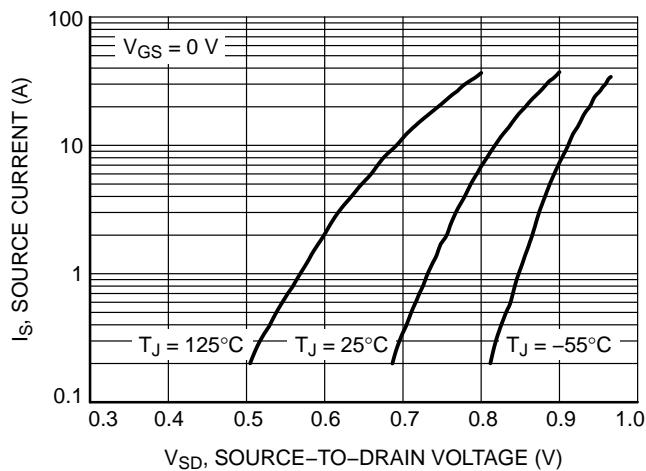


Figure 10. Diode Forward Voltage vs. Current

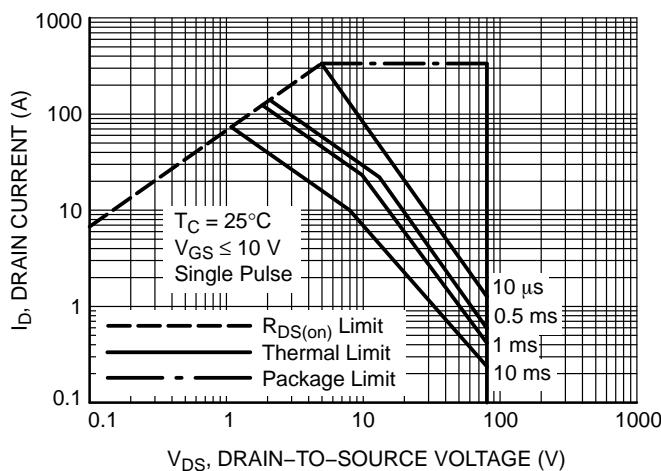


Figure 11. Maximum Rated Forward Biased Safe Operating Area

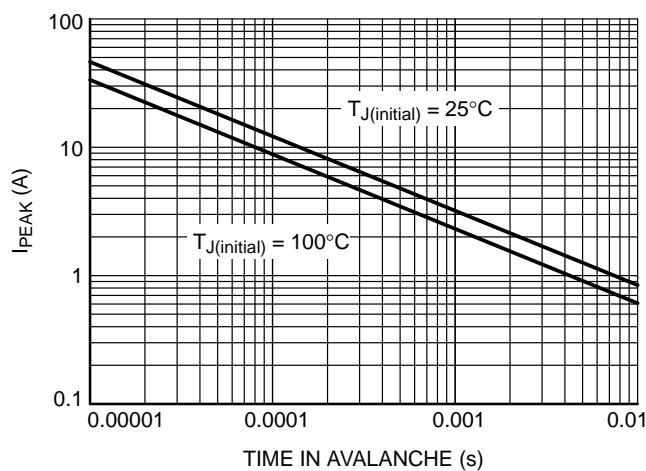


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVTFS6H850N

## TYPICAL CHARACTERISTICS

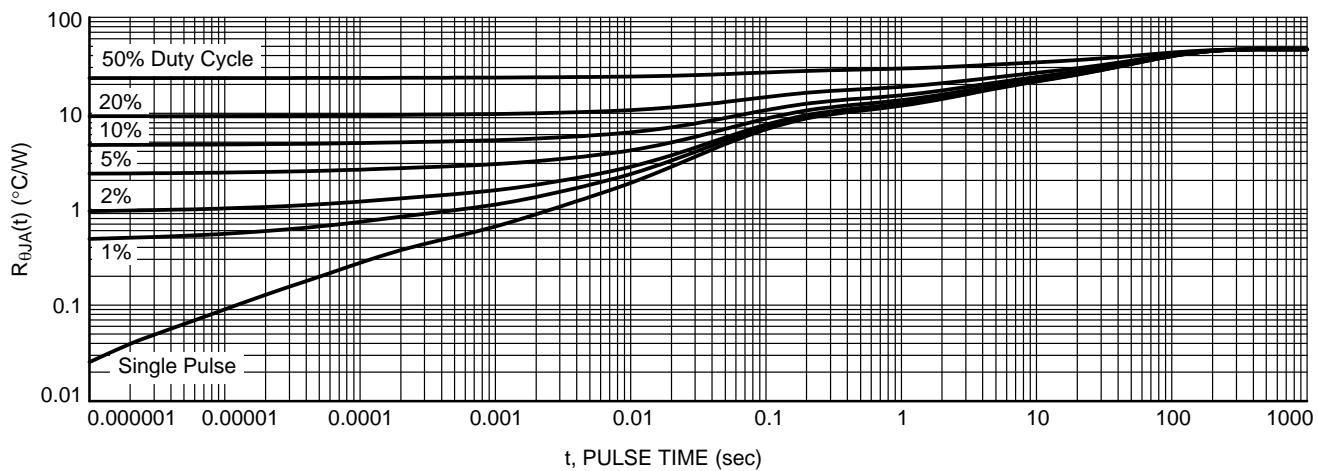


Figure 13. Thermal Response

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVTFS6H850NTAG	850N	WDFN8 3.3x3.3, 0.65P (Pb-Free)	1500 / Tape & Reel
NVTFS6H850NWFTAG	50NW	WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF) (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

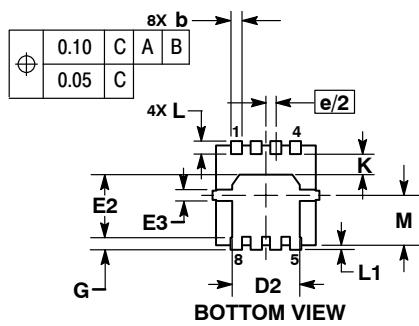
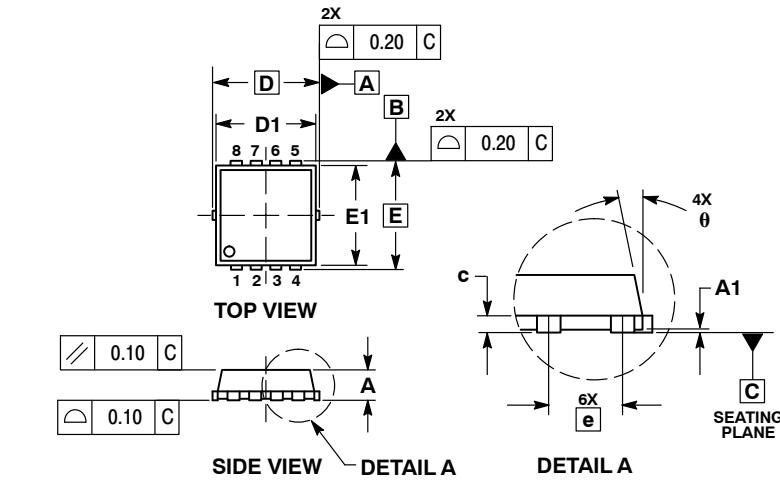
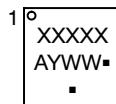
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

WDFN8 3.3x3.3, 0.65P  
CASE 511AB  
ISSUE D

DATE 23 APR 2012

GENERIC  
MARKING DIAGRAM\*

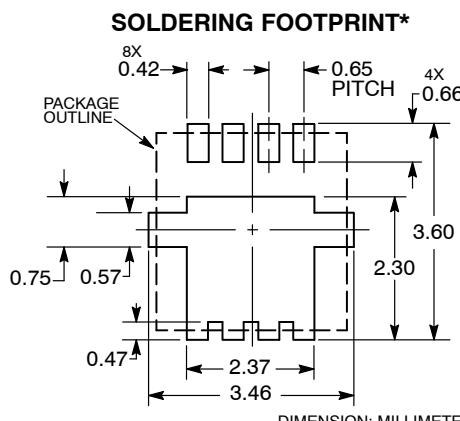
XXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30	BSC	3.30	0.130	BSC	0.130
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30	BSC	3.30	0.130	BSC	0.130
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65	BSC	0.65	0.026	BSC	0.026
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0	0°	---	12°	0°	---



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

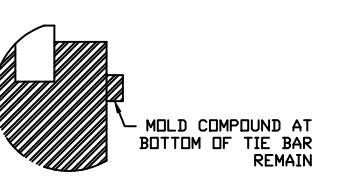
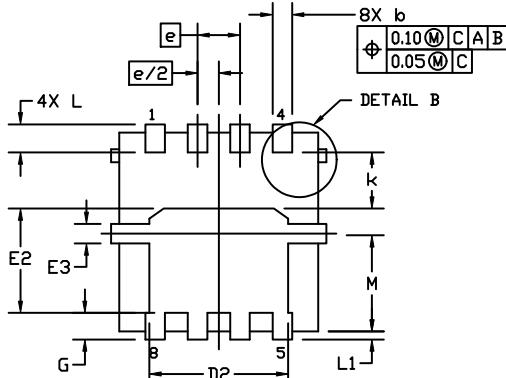
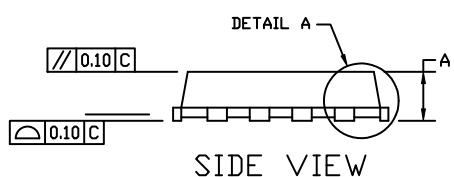
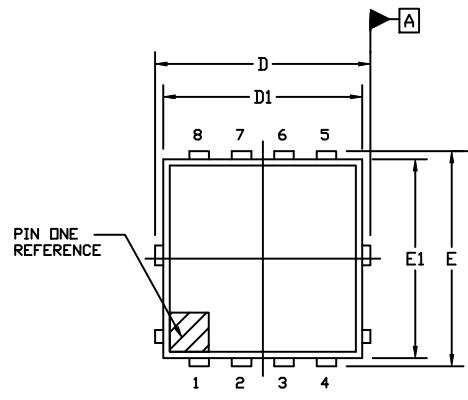
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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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**WDFNW8 3.3x3.3, 0.65P (Full-Cut  $\mu$ 8FL WF)**  
**CASE 515AN**  
**ISSUE O**

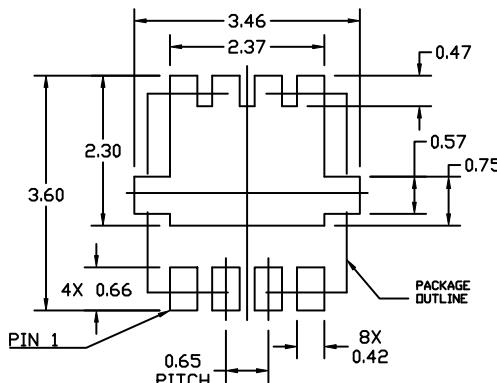
DATE 25 AUG 2020



DETAIL B

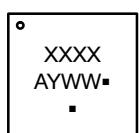
MOLD COMPOUND AT  
BOTTOM OF TIE BAR  
REMAIN

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERMM/D.

**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
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(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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