Description

The F1958 is part of IDT's *Glitch-Free™* family of DSAs optimized for the demanding requirements of Base Station (BTS) radio cards and numerous other applications. This device is offered in a compact 4mm x 4mm 24-pin package with 50Ω input and output impedance for ease of integration into the radio or RF system.

The F1958 offers very high reliability due to its construction from a monolithic silicon die in a QFN package. The insertion loss is very low with minimal distortion. Additionally, the device is designed to have extremely accurate attenuation levels. These accurate attenuation levels improve system SNR and/or ACLR by ensuring system gain is as close to the targeted level as possible. In addition, the very fast settling time in parallel mode is ideal for fast switching systems. Finally, the device uses our *Glitch-Free™* technology in contrast to competing DSAs.

Features

- Serial and 7-bit parallel interface
- 31.75dB range
- 0.25dB steps
- *Glitch-Free™*: low transient overshoot
- 500ns settling time for 0.25dB steps
- Ultra linear > 63dBm IIP3
- Low insertion loss < 1.7dB at 4GHz
- Attenuation error < ±0.2dB at 4GHz
- Bi-directional RF use
- 3.3V or 5V supply
- -40°C to +105°C operating temperature
- 4mm x 4mm Thin QFN 24-pin package

Competitive Advantage

- Lowest insertion loss for best SNR
- *Glitch-Free™* technology to protect power amplifiers or ADC during transitions between attenuation states
- Extremely accurate attenuation levels
- Ultra-low distortion
- MSL1 and 2000 V HBM ESD

Typical Applications

- 3G/4G/4G+ Base Station Systems
- Distributed Antenna Systems, DAS
- Remote Radio Heads
- Active Antenna Systems, AAS Broadband Satellite Equipment
- NFC Infrastructure
- Military Communication Equipment

Block Diagram

Figure 1. Block Diagram

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Pin Assignments

Figure 2. Pin Assignments for 4mm x 4mm x 0.75mm TQFN Package – Top View

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	D0	Parallel control pin – 0.25dB. Pull high for attenuation.
2	V_{DD}	Power supply input. Bypass to ground with capacitors as close as possible to pin.
3	V_{MODE}	Parallel or serial programming mode pin. Leave open or logic LOW for parallel mode. Logic HIGH for serial mode.
4, 6 - 13, 15	GND	Internally grounded. These pins must be grounded as close to the device as possible.
5	RF1	RF Port 1. Can be used as either the input or output RF (bi-directional). Port must be at 0V DC. An external AC coupling capacitor **must** be used if there is a DC voltage present.
14	RF2	RF Port 2. Can be used as either the input or output RF (bi-directional). Port must be at 0V DC. An external AC coupling capacitor **must** be used if there is a DC voltage present.
16	LE	Serial latch enable.
17	CLK	Serial clock input.
18	DATA	Serial data input.
19	D6	Parallel control pin – 16dB. Pull HIGH for attenuation. [a]
20	D5	Parallel control pin – 8dB. Pull HIGH for attenuation. [a]
21	D4	Parallel control pin – 4dB. Pull HIGH for attenuation. [a]
22	D3	Parallel control pin – 2dB. Pull HIGH for attenuation. [a]
23	D2	Parallel control pin – 1dB. Pull HIGH for attenuation. [a]
24	D1	Parallel control pin – 0.5dB. Pull HIGH for attenuation. [a]
	– EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

[a] There is a 500kΩ pull-down resistor to ground.

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Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1958 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{DD}	-0.3	5.8	V
V_{MODE}, DATA, CLK, LE, D[6:0]	V_{CTRL}	-0.3	Lower of (V_{DD}+0.25, 5.8)	V
RF1, RF2	V_{RF}	-0.3	0.3	V
Maximum RF Input Power to RF1 or RF2 (> 100 MHz)	P_{MAX}		+34	dBm
Junction Temperature	T_{JMAX}		+150	°C
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHMB}		2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		1000 (Class C3)	V

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Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage	V_{DD}		3.0		5.5	V
Operating Temperature Range	T_{EP}	Exposed paddle	-40		+105	°C
RF Frequency Range	f_{RF}		0.001		6	GHz
Maximum Input Power	P_{MAX}	RF1 or RF2			See Figure 3	dBm
RF Peak Input Power	P_{PEAK}	RF1 Port, V_{DD} = 3.3V, T_{EP}= 85°C, f_{RF} > 500MHz, WCDMA, 3GPP, Downlink, 64 DPCH, Chip rate =3.84MSPS, Avg. P_{IN} = +22dBm				
		1 %			28.9	dBm
		0.1 %			30.7	
		0.01 %			32.3	
		0.001 %			33.2	
RF1 Port Impedance	Z_1			50		Ω
RF2 Port Impedance	Z_2			50		Ω

Figure 3. Maximum Operating CW Input Power vs. Input Frequency

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Electrical Characteristics – Part 1

Table 4. Electrical Characteristics

Specifications apply at V_{DD} = 3.3V, T_{EP} = 25°C, f_{RF} = 2GHz, LSB = 0.25dB steps and Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted. Minimum attenuation D[6:0] = [0000000], Maximum attenuation D[6:0] = [1111111].

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH	V_{IH}	All logic pins	***2.6*** [a]		5.5	V
Logic Input LOW	V_{IL}	All logic pins	0		1	V
Logic Current	I_{IH}, I_{IL}		***-15***		***+15***	µA
DC Current	I_{DD}	V_{DD} = 3.3V		250	***400***	µA
		V_{DD} = 5.5V		310		
Attenuation Range		No missing codes		31.75		dB
Minimum Gain Step for Monotonicity	LSB	f_{RF} < 4.0GHz		0.25		dB
		f_{RF} < 6.0GHz		0.50		
		f_{RF} < 8.0GHz		1.00		
DSA Settling Time [b]	t_{SET}	Max to min attenuation to settle to within 0.5dB of final value		1.2		µs
		Min to max attenuation to settle to within 0.5dB of final value		2.0		
Maximum Video Feed-Through	VID_{FT}	Measured with 10ns rise time, 0V to 3.3V control pulse		10		mV_{pp}
Maximum Spurious Level on any RF Port [c]	$SPUR_{MAX}$	Unused RF ports terminated into 50Ω		-118		dBm
Serial Clock Speed	f_{CLK}				***10***	MHz
Parallel to Serial Setup	t_{PS}		100			ns
Serial Data Hold Time	t_H		10			ns
LE Delay		Time from final serial clock rising edge	10			ns
Maximum Switch Rate	SW_{RATE}			25		kHz

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Speeds are measured after SPI programming is completed (data latched with LE = LOW to HIGH transition).

[c] Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

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Electrical Characteristics – Part 2

Table 5. Electrical Characteristics

Specifications apply at V_{DD} = 3.3V, T_{EP} = 25°C, f_{RF} = 2GHz, LSB = 0.25dB steps and Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted. Minimum attenuation D[6:0] = [0000000], Maximum attenuation D[6:0] = [1111111].

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss	IL	1MHz ≤ f_{RF} ≤ 1GHz		1.1	***1.2*** [a]	dB
		1GHz < f_{RF} ≤ 2GHz		1.3	1.5	
		2GHz < f_{RF} ≤ 3GHz		1.5	1.7	
		3GHz < f_{RF} ≤ 4GHz		1.6	2.2	
		4GHz < f_{RF} ≤ 5GHz		1.9	2.6	
		5GHz < f_{RF} ≤ 6GHz		2.6	3.0	
Relative Phase Between the Minimum and Maximum Attenuation	Φ_{Δ}	f_{RF} = 1GHz		12		deg
		f_{RF} = 2GHz		25		
		f_{RF} = 4GHz		50		
		f_{RF} = 6GHz		70		
Step Error	DNL	Maximum error between any two adjacent attenuation levels		0.15	0.28	dB
Absolute Attenuation Error	INL	Max. error for state 19.75dB, f_{RF} = 2000MHz	***-0.5***		***+0.5***	dB
		Max. error, over all states f_{RF} = 2000MHz	-0.8	-0.25 +0.08	+0.5	
RF1 Port Return Loss	RL_1	1MHz ≤ f_{RF} ≤ 2GHz		20		dB
		2GHz < f_{RF} ≤ 4GHz		17		
		4GHz < f_{RF} ≤ 6GHz		13		
RF2 Port Return Loss	RL_2	1MHz ≤ f_{RF} ≤ 2GHz		20		dB
		2GHz < f_{RF} ≤ 4GHz		16		
		4GHz < f_{RF} ≤ 6GHz		12		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

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Electrical Characteristics – Part 3

Table 6. Electrical Characteristics

Specifications apply at V_{DD} = 3.3V, T_{EP} = 25°C, f_{RF} = 2GHz, LSB = 0.25dB steps and Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted. Minimum attenuation D[6:0] = [0000000], Maximum attenuation D[6:0] = [1111111].

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input IP3	IIP3	P_{IN} = +19dBm per tone 50MHz tone separation				
		Attn = 0.00dB		64		dBm
		Attn = 15.75dB		64		
		Attn = 31.75dB		64		
		P_{IN} = +16dBm per tone 1MHz tone separation				
		f_{RF} = 0.7GHz	60 [a]	63.3		dBm
		f_{RF} = 1.8GHz	60	63.7		
		f_{RF} = 2.2GHz	60	63.4		
		f_{RF} = 2.6GHz	60	63.7		
Input 0.1dB Compression [b]	$IP_{0.1dB}$			35		dBm

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] The input 0.1dB compression point is a linearity figure of merit. Refer to the Recommended Operating Conditions section and Figure 3 for the maximum operating power levels.

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Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	42	°C/W
Junction to Case Thermal Resistance (case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	8	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

- V_{DD} = 3.3V
- $Z_L = Z_S = 50\Omega$
- T_{EP} = 25°C
- f_{RF} = 2.0GHz
- Attenuation setting = 0 dB = D[6:0] =[0000000]
- P_{in} = +16dBm / tone
- 50MHz tone spacing
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

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Typical Performance Characteristics

Figure 4. Insertion Loss vs Frequency

Figure 5. Insertion Loss vs Attenuator Setting

Figure 6. Input Return Loss vs Frequency [All States]

Figure 7. Input Return Loss vs Attenuator Setting

Figure 8. Output Return Loss vs Frequency [All States]

Figure 9. Output Return Loss vs Attenuator Setting

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Figure 10. Worst Case Absolute Accuracy vs Frequency [LSB = 0.25dB]

Figure 11. Absolute Accuracy vs Attenuator Setting [LSB = 0.25dB]

Figure 12. Worst Case Absolute Accuracy vs Frequency [LSB = 0.50dB]

Figure 13. Absolute Accuracy vs Attenuator Setting [LSB = 0.50dB]

Figure 14. Worst Case Absolute Accuracy vs Frequency [LSB = 1.00dB]

Figure 15. Absolute Accuracy vs Attenuator Setting [LSB = 1.00dB]

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Figure 16. Worst Case Step Accuracy vs Frequency [LSB = 0.25dB]

Figure 17. Step Accuracy vs Attenuator Setting [LSB = 0.25dB]

Figure 18. Worst Case Step Accuracy vs Frequency [LSB = 0.50dB]

Figure 19. Step Accuracy vs Attenuator Setting [LSB = 0.50dB]

Figure 20. Worst Case Step Accuracy vs Frequency [LSB = 1.00dB]

Figure 21. Step Accuracy vs Attenuator Setting [LSB = 1.00dB]

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Figure 22. Relative Insertion Phase vs Frequency [All States]

Figure 23. Relative Insertion Phase vs Attenuator Setting

Figure 24. Attenuation vs Frequency [All States]

Figure 25. Attenuation vs Attenuator Setting

Figure 26. Insertion Loss vs Frequency [0dB]

Figure 27. Evaluation Board Insertion Loss

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Figure 28. Input IP3 vs Frequency [0dB]

Figure 29. Input IP3 vs Attenuation [2GHz]

Figure 30. Compression vs Input Power [2GHz]

Figure 31. Typical Switching Time for a 0.25dB Attenuation Transition

Figure 32. Switching Time between Maximum and Minimum Attenuation

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Programming

The F1958 can be programmed using either the parallel or the serial mode, which is selectable via V_{MODE} (pin 3). The serial mode is selected by pulling V_{MODE} to a logic HIGH, and the parallel mode is selected by floating V_{MODE} or setting it to logic LOW.

Serial Mode

F1958 Serial Mode is selected by pulling V_{MODE} to a logic HIGH. The serial interface uses a 8-bit word with only 7 bits used. The serial word is shifted in LSB (D0) first. When serial programming is used, all the parallel control input pins (1, 19 - 24) must be grounded.

Table 8. 7-Bit SPI Word Sequence

Data Bit	Symbol
D7	Not Used
D6	Attenuation 16 dB Control Bit
D5	Attenuation 8 dB Control Bit
D4	Attenuation 4 dB Control Bit
D3	Attenuation 2 dB Control Bit
D2	Attenuation 1 dB Control Bit
D1	Attenuation 0.5 dB Control Bit
D0	Attenuation 0.25 dB Control Bit

Table 9. Truth Table for Serial Control Word

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
X	0	0	0	0	0	0	0	0
X	0	0	0	0	0	0	1	0.25
X	0	0	0	0	0	1	0	0.5
X	0	0	0	0	1	0	0	1
X	0	0	0	1	0	0	0	2
X	0	0	1	0	0	0	0	4
X	0	1	0	0	0	0	0	8
X	1	0	0	0	0	0	0	16
X	1	1	1	1	1	1	1	31.75

In the Serial Mode, the F1958 is programmed via the serial port on the rising edge of Latch Enable (LE). It is required that LE be kept logic LOW until all data bits are clocked into the shift register. The F1958 will change attenuation state after the data word is latched into the active register. Refer to Figure 33.

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Figure 33. Serial Register Timing Diagram

Table 10. SPI Timing Diagram Values for the Serial Mode

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
CLK Frequency	f_C				25	MHz
CLK HIGH Duration Time	t_{CH}		20			ns
CLK LOW Duration Time	t_{CL}		20			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [a]	t_P		40			ns
CLK to Data Hold Time	t_H		10			ns
Final CLK Rising Edge to LE Rising Edge	t_{CLS}		10			ns
LE to CLK Setup Time	t_{LS}		10			ns
LE Trigger Pulse Width	t_L		10			ns
LE Trigger to CLK Setup Time [b]	t_{LC}		10			ns

[a] $(t_{CH} + t_{CL}) \geq 1/f_C$.

[b] Once all desired data has been clocked in, LE must transition from LOW to HIGH after the minimum setup time t_{LC} and before any further CLK signals.

Serial Mode Default Startup Condition

When the device is first powered up, it will default to the maximum attenuation of 31.75dB independent of the V_{MODE} and parallel pin [D6:D0] conditions.

Table 11. Default Setting Truth Table for Serial Control Word

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
X	1	1	1	1	1	1	1	31.75

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Parallel Control Mode

For the F1958, the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode

Direct Parallel Mode is selected when V_{MODE} is floating or a logic LOW and LE is a logic HIGH. In this mode, the device will immediately react to any voltage changes on the parallel control pins (1, 19 - 24). Use Direct Parallel Mode for the fastest settling time. The serial pins, CLK and DATA, can be either grounded or left opened in the Parallel Mode.

Latched Parallel Mode

Latched Parallel Mode is selected when V_{MODE} is floating or a logic LOW and LE is toggled from logic LOW to HIGH. To utilize Latched Parallel Mode:

- Set V_{MODE} to logic LOW or leave floating.
- Set LE to logic LOW.
- Adjust pins (1, 19 - 24) to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Set LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D6 - D0.
- If LE is set to a logic LOW then the attenuator will not change state.

The truth table for the Parallel Mode is identical for bits D6 to D0 as shown in the Serial Mode truth table; see Table 9.

Figure 34. Latch Parallel Timing Diagram

Table 12. Latched Parallel Timing Diagram Values

Parameter	Symbol	Min	Max	Units
Serial to Parallel Mode Setup Time	t_{SPS}	100		ns
Parallel Data Hold Time	t_{PDH}	10		ns
LE Minimum Pulse Width	t_{LE}	10		ns
Parallel Data Setup Time	t_{PDS}	10		ns

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Evaluation Kit Picture

Figure 35. Top View

Figure 36. Bottom View

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Evaluation Kit / Applications Circuit

Figure 37. Electrical Schematic

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Table 13. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 - C8, C11 - C13	11	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
C9, C15	2	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C10, C14	2	10nF ±5%, 50V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
R14	1	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R1 - R8, R11 - R13	11	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
R9	1	10kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
J5, J7, J8	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J10	1	CONN HEADER VERT SGL 4 X 2 POS GOLD	67997-108HLF	Amphenol FCI
J6	1	CONN HEADER VERT SGL 10 X 1 POS GOLD	961110-6404-AR	3M
J1 - J4, J11	5	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
SW1	1	SWITCH 8 POSITION DIP SWITCH	KAT1108E	E-Switch
U1	1	DSA	F1958NBGK	IDT
	1	Printed Circuit Board	F1958 EVKit Rev 01	IDT
J9, R10		Do Not Populate (DNP)		

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Evaluation Kit Operation

Power Supply Setup

Set up a power supply in the voltage range of 3.0V to 5.5V with the power supply output disabled. The voltage can be applied via one of the following connections (see Figure 38):

- J11 connector
- J5 header connection (note the polarity of the GND pin on this connector)
- Pin 9 (V_{DD}) and pin 10 (GND) on the J6 header connection

Figure 38. Power Supply Connections

Parallel Logic Control Setup

The Evaluation Board has the ability to control the F1958 in the Parallel Mode. For external control, apply logic voltages to the J6 header pins 1 through 7 (see Figure 39). For manual control, switches 1 through 7 on SW1 can be set. The switch is a three-position switch. The bottom position, "-" will ground the pin. The center position "O" will leave the pin open circuited. Setting the switch to the top position "+" will apply a voltage that is supplied to the switch.

The logic voltage can be applied in one of three ways:

- Apply a voltage through a SMA connector (J9). This connector is not supplied.
- Apply a voltage on pin 2 of the J7 header connector.
- Short out the two header connectors, J7 and J8, so a resistor divider will generate the correct logic voltage from the power supply on the Evaluation Board. The logic voltage will be V_{DD}.

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Figure 39. Parallel Logic Voltage Connections

Serial Logic Control Setup

The Evaluation Board has the ability to control the F1958 in the Serial Mode. Connect the serial controller to the J10 header connection as shown in Figure 40. To use the Serial Mode, set SW1 switch 8 to the "+" or "O" position.

The attenuation setting can be programmed according to Table 9.

Figure 40. Serial Logic Connections

Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the "Power Supply Setup" section and either the "Parallel Logic Control Setup" or "Serial Logic Control Setup" sections above.

- Enable the power supply.
- Enable the proper attenuation setting according to Table 9.

Power-Off Procedure

- Set the logic control pins to a logic LOW.
- Disable the power supply.

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Application Information

Digital Pin Voltage and Resistance Values

Table 14 provides the open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Table 14. Digital Pin Voltages and Resistance

Pin	Name	Open Circuit DC Voltage	Internal Connection
3, 16, 17, 18	V_{MODE}, LE, CLK, DATA	0V	500kΩ pull-down resistor to GND
1, 19 - 24	D0, D6 – D1	0V	500kΩ pull-down resistor to GND

Power Supplies

A common power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage changes or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to pins for the SPI (16, 17, 18), parallel (1, 19-24) and V_{MODE} pin (3) as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

Figure 41. Control Pin Interface for Signal Integrity

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Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nbnbg24-package-outline-40-x-40-mm-bodyepad-270mm-sq-050-mm-pitch-qfn

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1958NBGK	4mm x 4mm x 0.75mm 24 pin QFN	1	Tray	-40°C to +105°C
F1958NBGK8	4mm x 4mm x 0.75mm 24 pin QFN	1	Reel	-40°C to +105°C
F1958EVB	Evaluation Board			
F1958EVS	Evaluation Solution including the Evaluation Board, Controller Board, and cable. The Evaluation Software is available for download on the product page on the IDT website: http://www.idt.com/F1958			

Marking Diagram

1. Line 1 and 2 are the part number.
2. Line 3 “Z” is for die version.
3. Line 3 “yyww” = 1716 has two digits for the year and week that the part was assembled.
4. Line 3 “NG” denotes Assembly Lot number.

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Revision History

Revision Date	Description of Change
November 13, 2019	Updated J10 connector on Evaluation Schematic to show all 8 pins (previously only 4 were displayed).
August 22, 2018	Absolute Attenuator Error minimum value changed from -0.4 dB to -0.5 dB.
March 26, 2018	Initial release

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH

TOP VIEW

BOTTOM VIEW

SIDE VIEW

COMMON DIMENSION

SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED
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APPROVALS	DATE
DRAWN RAC	5/11/16
CHECKED	

TITLE NB/NBG24 PACKAGE OUTLINE
4.0 x 4.0 mm BODY,EPAD 2.70mm SQ
0.50 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4313-03	00

DO NOT SCALE DRAWING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH

RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL X± .1 XX± .05 XXX± .030 ANGULAR ±1°		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE NB/NBG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY,EPAD 2.70mm SQ 0.50 mm PITCH QFN	
DRAWN RAC	5/11/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4313-03 / REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

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