

## ISL1557A

12V xDSL Differential Line Driver with Enhanced Output Protection

FN6568  
Rev.4.00  
Aug 3, 2020

The [ISL1557A](#) is a dual operational amplifier designed for VDSL2 and ADSL line driving in DMT based solutions. This device features a high drive capability of 750mA while consuming only 6mA of supply current per amplifier and operating from a single 4.5V to 12V supply. The driver achieves a typical distortion of -80dBc at 150kHz into a 25Ω load. The ISL1557A is designed with stronger output clamps to enhance protection against lightning transients.

The ISL1557A is available in the thermally-enhanced 16 Ld QFN package and is specified for operation over the full -40°C to +85°C temperature range. The ISL1557A has two control pins (C<sub>0</sub> and C<sub>1</sub>) for controlling the bias and enable/disable of the outputs. These controls allow for lowering the power to fit the performance/power ratio for the application.

The ISL1557A is ideal for ADSL2+, SDSL, HDSL2, and VDSL line driving applications, including both 14.5dBm and 21dBm applications.

### Related Literature

For a full list of related documents, visit our website

- [ISL1557A](#) product page

### Features

- 21dBm output power capability
- Drives up to 750mA from a +12V supply
- 20V<sub>P-P</sub> differential output drive into 21Ω
- -80dBc typical driver output distortion at full output at 150kHz
- -75dBc typical driver output distortion at 4MHz
- -82dBc typical driver output distortion at 10MHz
- -79dBc typical driver output distortion at 17MHz
- Low quiescent current of 6mA per amplifier
- Supply range
  - ISL1557AIRZ ..... ±2.25V to ±6V, 4.5V to 12V
- 300MHz bandwidth
- Thermal shutdown
- Pb-free (RoHS compliant)

### Applications

- VDSL2 line drivers
- ADSL2+ CPE line driving
- G.SHDSL and HDSL2 line drivers

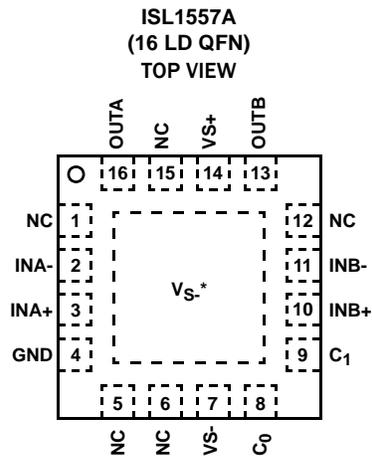
## Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL1557AIRZ	155 7AIRZ	-40 to +85	-	16 Ld 4x4 QFN	L16.4x4H
ISL1557AIRZ-T7	155 7AIRZ	-40 to +85	1k	16 Ld 4x4 QFN (Tape and Reel)	L16.4x4H

### NOTES:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
- For Moisture Sensitivity Level (MSL), see the [ISL1557A](#) device page. For more information about MSL, see [TB363](#).

## Pin Configurations



\*THERMAL PAD MUST BE CONNECTED TO NEGATIVE SUPPLY:  $V_{S-}$ . QFN PACKAGE CAN BE USED IN SINGLE AND DUAL SUPPLY APPLICATIONS.

## Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1, 5, 6, 12, 15	NC	No connect
2	INA-	Inverting input of Amplifier A
3	INA+	Non-inverting input of Amplifier A
4	GND	Ground connect
7	VS-	Negative supply
8	C <sub>0</sub> ( <a href="#">Note 4</a> )	Current control bias pin
9	C <sub>1</sub> ( <a href="#">Note 4</a> )	Current control bias pin
10	INB+	Non-inverting input of Amplifier B
11	INB-	Inverting input of Amplifier B
13	OUTB	Output of Amplifier B
14	VS+	Positive supply
16	OUTA	Output of Amplifier A

**NOTE:**

4. The single DSL port is made of Amplifiers A and B. C<sub>0</sub> and C<sub>1</sub> control I<sub>S</sub> settings for the DSL port.

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

$V_S+$ Voltage to Ground	-0.3V to +13.2V
$V_{IN+}$ Voltage	GND to $V_S+$
Current into any Input	8mA
Continuous Output Current	75mA
$C_0, C_1$ to Ground	+6.6V
ESD Rating	
Human Body Model	1kV
Machine Model	1.5kV

**Thermal Information**

Ambient Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Operating Junction Temperature	+150°C
Power Dissipation	see <a href="#">Figure 23 on page 8</a>
Pb-Free reflow profile	see <a href="#">TB493</a>

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**Electrical Specifications**  $V_S = 12\text{V}, R_F = 750\Omega, R_{L-DIFF} = 50\Omega, C_0 = C_1 = 0\text{V}, T_A = +25^\circ\text{C}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC PERFORMANCE</b>						
BW	-3dB Bandwidth	$R_F = 499\Omega, A_V = +5$		300		MHz
		$R_F = 750\Omega, A_V = +5$		250		MHz
		$R_F = 750\Omega, A_V = +10$		200		MHz
THD	Total Harmonic Distortion, Differential	$f = 4\text{MHz}, V_O = 4V_{P-P\_DIFF}, R_{L-DIFF} = 100\Omega$		-75		dBc
		$f = 10\text{MHz}, V_O = 4V_{P-P\_DIFF}, R_{L-DIFF} = 100\Omega$		-82		dBc
		$f = 17\text{MHz}, V_O = 4V_{P-P\_DIFF}, R_{L-DIFF} = 100\Omega$		-79		dBc
SR	Slew Rate, Single-ended	$V_{OUT}$ from -3V to +3V	750	1200		V/ $\mu\text{s}$
<b>DC PERFORMANCE</b>						
$V_{OS\_CM}$	Offset Voltage Common Mode		-40		+40	mV
$V_{OS\_DM}$	Offset Voltage Differential Mode		-7.5		+7.5	mV
$R_{OL}$	Differential Transimpedance	$V_{OUT} = 12V_{P-P}$ differential, unloaded		3.0		M $\Omega$
<b>INPUT CHARACTERISTICS</b>						
$I_{B+}$	Non-Inverting Input Bias Current		-7.0		+7.0	$\mu\text{A}$
$I_{B-DM}$	Inverting Input Bias Current Differential Mode		-75	3	+75	$\mu\text{A}$
$e_N$	Input Noise Voltage	$f = 10\text{kHz}$		8.2		$\text{nV}/\sqrt{\text{Hz}}$
$i_N$	Input Noise Current	$f = 10\text{kHz}$		25		$\text{pA}/\sqrt{\text{Hz}}$
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OUT}$	Loaded Output Swing (Single-ended)	$V_S = \pm 6\text{V}, R_{L-DIFF} = 50\Omega$	$\pm 4.85$	$\pm 5.0$		V
		$V_S = \pm 6\text{V}, R_{L-DIFF} = 20\Omega$	$\pm 4.4$	$\pm 4.7$		V
$I_{OUT}$	Output Current	$R_L = 0\Omega$		1000		mA
<b>SUPPLY</b>						
$V_S$	Supply Voltage	Single supply	4.5		13.2	V
$I_{S+}$ (Full Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = C_1 = 0\text{V}$	12	15	21.5	mA
$I_{S+}$ (Medium Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = 5\text{V}, C_1 = 0\text{V}$		11		mA
$I_{S+}$ (Low Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = 0\text{V}, C_1 = 5\text{V}$		6.0		mA
$I_{S+}$ (Power down)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = C_1 = 5\text{V}$		0.6	1.0	mA
$I_{INH}, C_0$ or $C_1$	$C_0, C_1$ Input Current, High	$C_0, C_1 = 6\text{V}$	100	175	250	$\mu\text{A}$
$I_{INL}, C_0$ or $C_1$	$C_0, C_1$ Input Current, Low	$C_0, C_1 = 0\text{V}$	-5		+5	$\mu\text{A}$
$V_{INH}, C_0$ or $C_1$	$C_0, C_1$ Input Voltage, High		2.0			V
$V_{INL}, C_0$ or $C_1$	$C_0, C_1$ Input Voltage, Low				0.8	V

# Typical Performance Curves

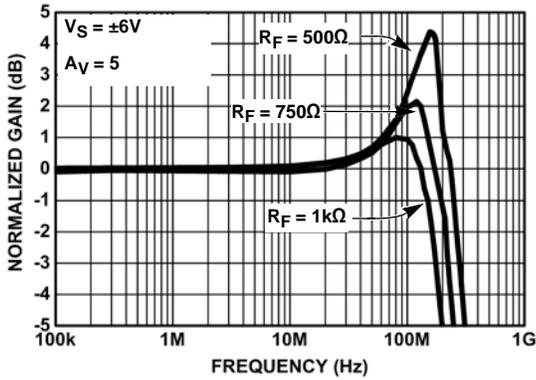


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (FULL BIAS MODE)

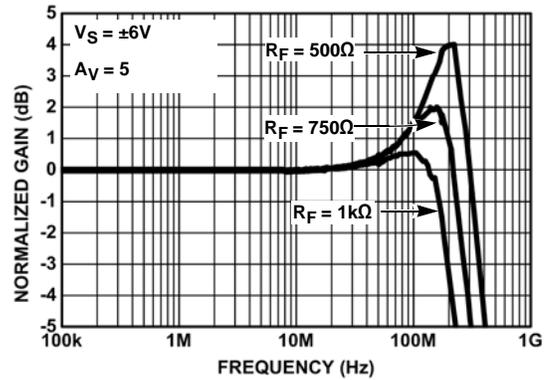


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (MEDIUM BIAS MODE)

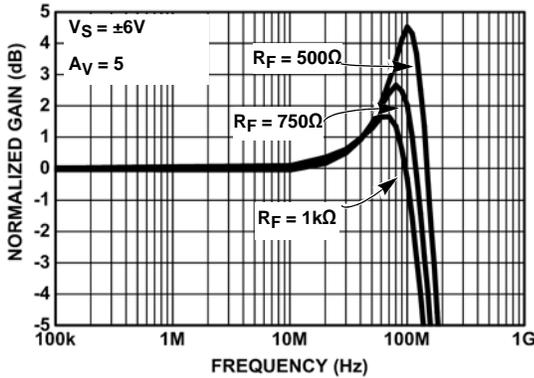


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (LOW BIAS MODE)

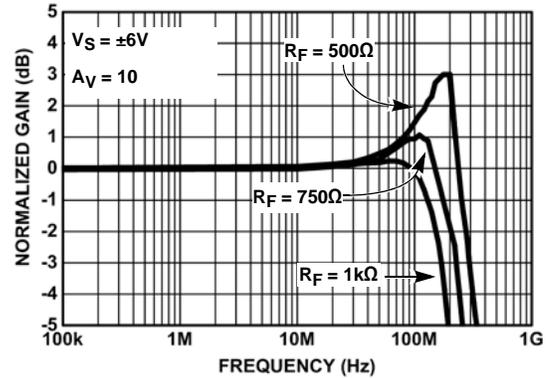


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (FULL BIAS MODE)

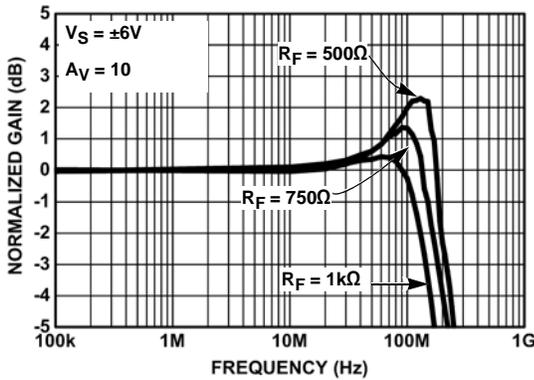


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (MEDIUM BIAS MODE)

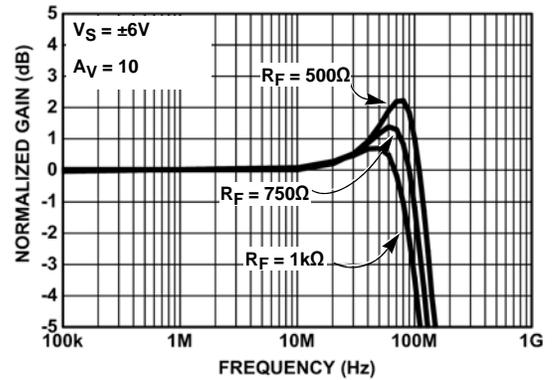


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS  $R_F$  (LOW BIAS MODE)

## Typical Performance Curves (Continued)

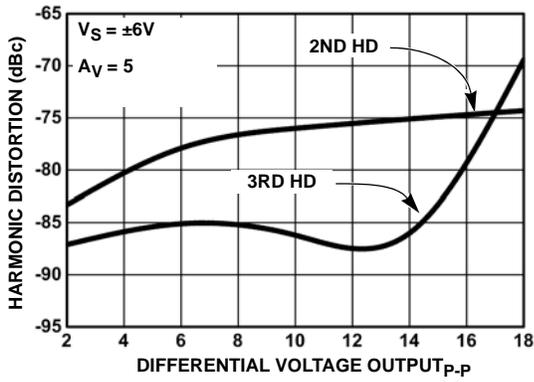


FIGURE 7. HARMONIC DISTORTION at 2MHz

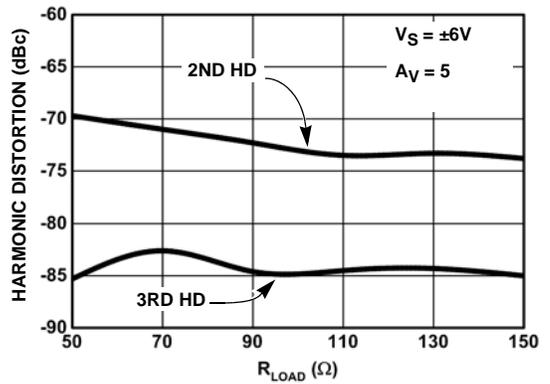


FIGURE 8. 2ND AND 3RD HARMONIC DISTORTION vs  $R_{LOAD}$  at 2MHz

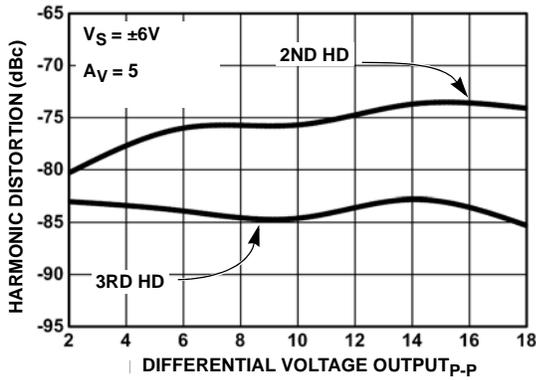


FIGURE 9. HARMONIC DISTORTION at 3MHz

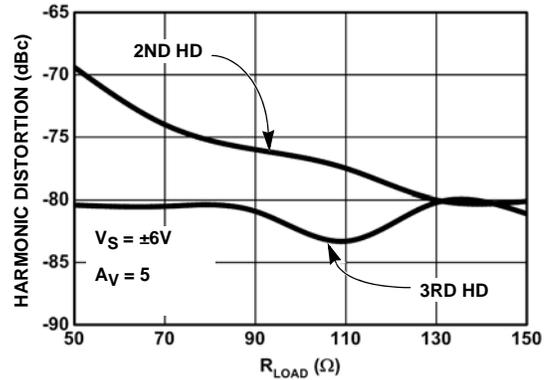


FIGURE 10. 2ND AND 3RD HARMONIC DISTORTION vs  $R_{LOAD}$  at 3MHz

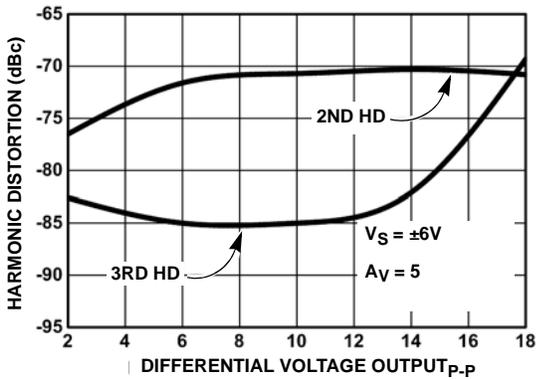


FIGURE 11. HARMONIC DISTORTION at 5MHz

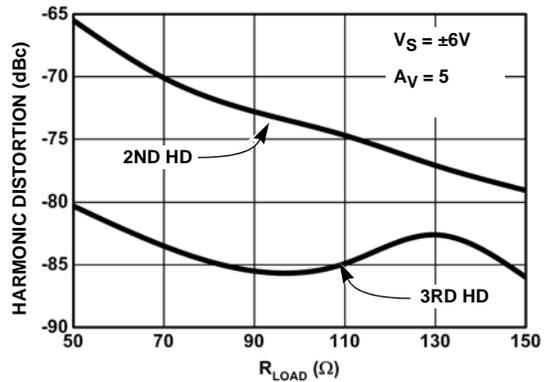


FIGURE 12. 2ND AND 3RD HARMONIC DISTORTION vs  $R_{LOAD}$  at 5MHz

# Typical Performance Curves (Continued)

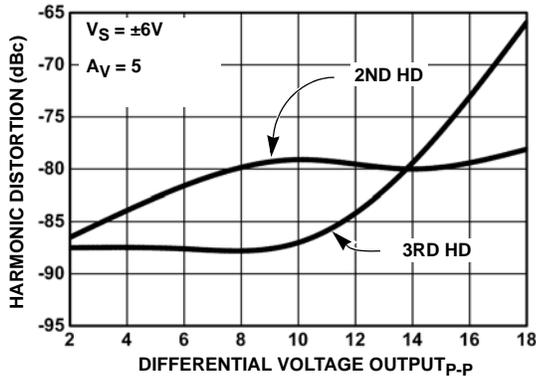


FIGURE 13. HARMONIC DISTORTION at 10MHz

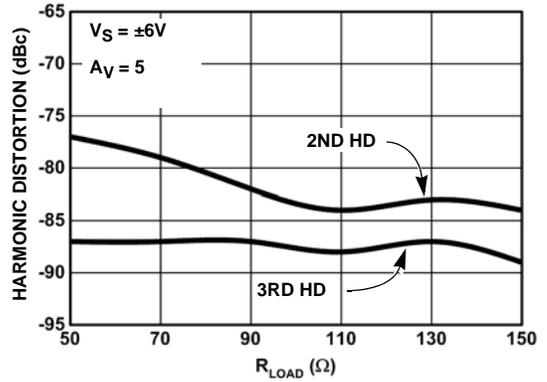


FIGURE 14. 2ND AND 3RD HARMONIC DISTORTION vs  $R_{LOAD}$  at 10MHz

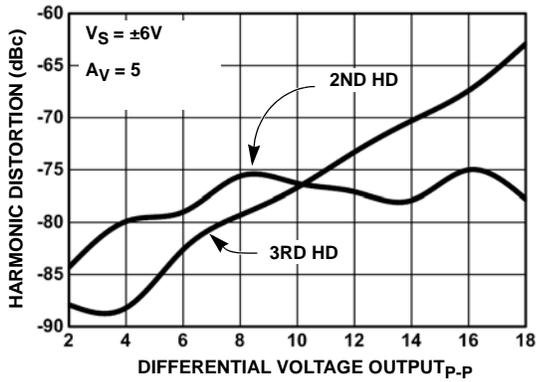


FIGURE 15. HARMONIC DISTORTION at 17MHz

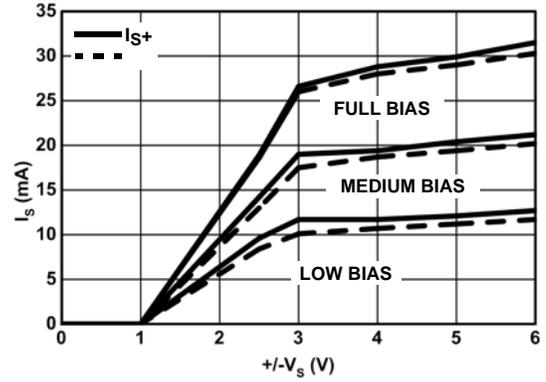


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

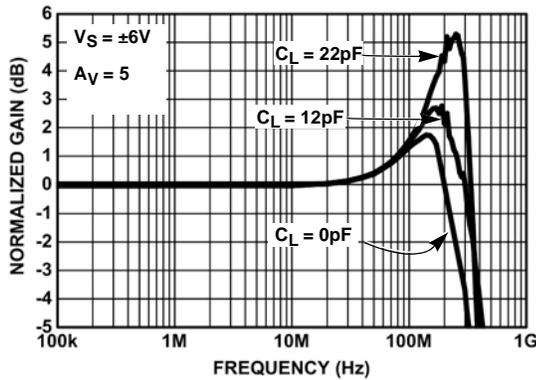


FIGURE 17. FREQUENCY RESPONSE WITH VARIOUS  $C_L$  (FULL BIAS MODE)

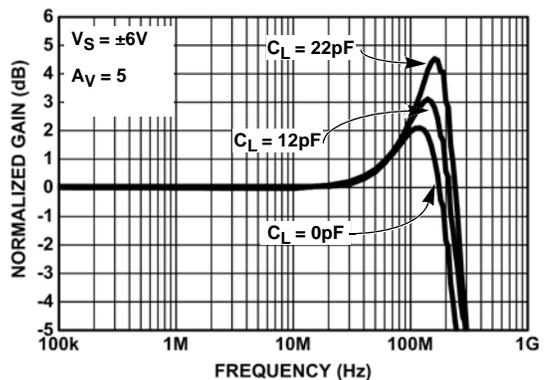
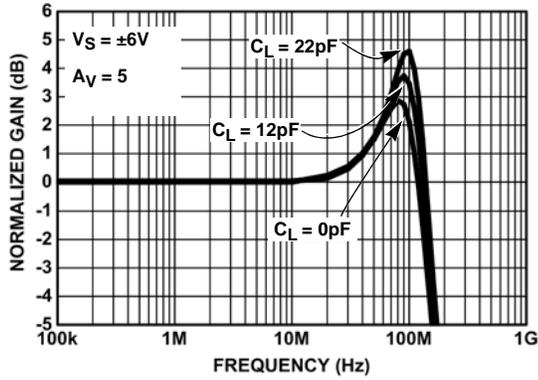
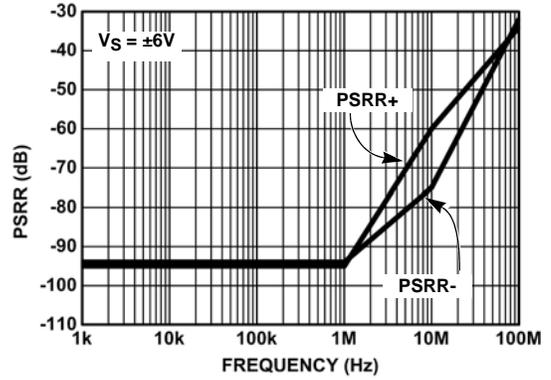


FIGURE 18. FREQUENCY RESPONSE vs VARIOUS  $C_L$  (MEDIUM BIAS MODE)

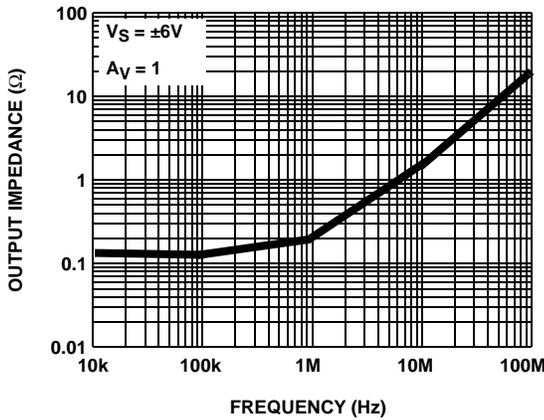
**Typical Performance Curves (Continued)**



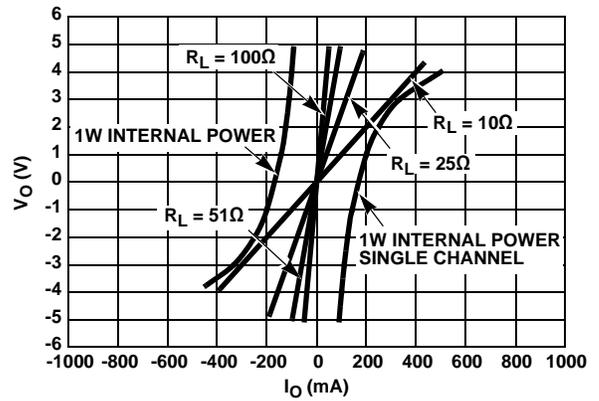
**FIGURE 19. FREQUENCY RESPONSE WITH VARIOUS  $C_L$  (LOW BIAS MODE)**



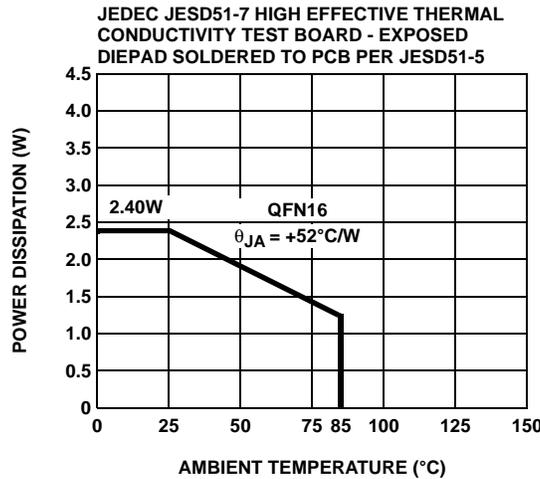
**FIGURE 20. PSRR vs FREQUENCY**



**FIGURE 21. OUTPUT IMPEDANCE vs FREQUENCY**



**FIGURE 22. OUTPUT VOLTAGE AND CURRENT LIMITATIONS**



**FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE**

## Applications Information

### Product Description

The ISL1557A is a dual operational amplifier designed for line driving in DMT ADSL2+ and VDSL solutions. It is a dual current mode feedback amplifier with low distortion that draws a moderately low supply current. It is built using proprietary Renesas complimentary bipolar process and is offered in industry standard pinouts. Due to the current feedback architecture, the ISL1557A closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First, select the desired bandwidth by choosing the feedback resistor,  $R_F$ , then set the gain by choosing the gain resistor,  $R_G$ . The curves at the beginning of the “Typical Performance Curves” on page 5 show the effect of varying both  $R_F$  and  $R_G$ . The 3dB bandwidth is somewhat dependent on the power supply voltage.

### Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible (below 0.25”). The power supply pins must be well bypassed to reduce the risk of oscillation. A 4.7 $\mu$ F tantalum capacitor in parallel with a 0.1 $\mu$ F ceramic capacitor is adequate for each supply pin. During power-up, it is necessary to limit the slew rate of the rising power supply to within 1V/ $\mu$ s. If the power supply rising time is undetermined, a series 10 $\Omega$  resistor on the power supply line can be used to ensure the proper power supply rise time.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, but avoid using wire-wound resistors because of their parasitic inductance. Similarly, capacitors should be low inductance for the best performance.

### Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will effect the AC and transient performance of the ISL1557A when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect because this point is at a virtual ground and stray capacitance is therefore not detected by the amplifier.

### Feedback Resistor Values

The ISL1557A has been designed and specified with  $R_F = 750\Omega$  for  $A_V = +5$ . This value of feedback resistor yields extremely flat frequency response with 1dB peaking out to 250MHz. As with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. See the curves in the “Typical Performance Curves” section starting on page 5, which show 3dB bandwidth and peaking vs frequency for various feedback resistors and various supply voltages.

### Bandwidth vs Temperature

Although many amplifiers' supply current and consequently 3dB bandwidth drop off at high temperatures, the ISL1557A is designed to have little supply current variations with temperature. An immediate benefit is that the 3dB bandwidth does not drop off drastically with temperature.

### Supply Voltage Range

The ISL1557A is designed to operate with supply voltages from  $\pm 2.25V$  to  $\pm 6V$  nominal. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages.

### Single Supply Operation

If a single supply is desired, values from +4.5V to +12V nominal can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either:

- DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or:
- Ensure the driving signal is within the common mode range of the ISL1557A.

### ADSL CPE Applications

The ISL1557A is designed as a line driver for ADSL CPE modems. It is capable of outputting 450mA of output current with a typical supply voltage headroom of 1.3V. It can achieve -85dBc of distortion at low 7.1mA of supply current per amplifier.

The average line power requirement for the ADSL CPE application is 14.5dBm (28mW) into a 100 $\Omega$  line. The average line voltage is 1.67V<sub>RMS</sub>. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 7.5V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. The circuit configuration is shown in Figure 24.

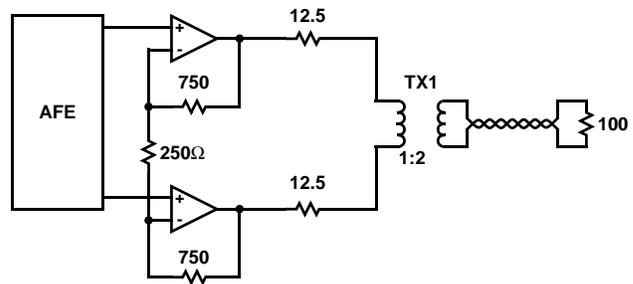


FIGURE 24. CIRCUIT CONFIGURATION

## Revision History

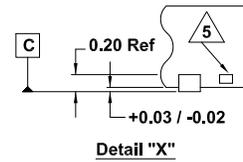
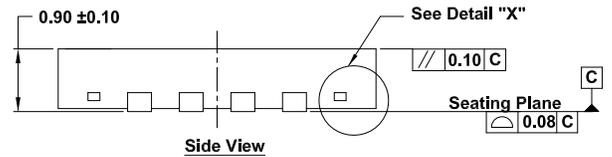
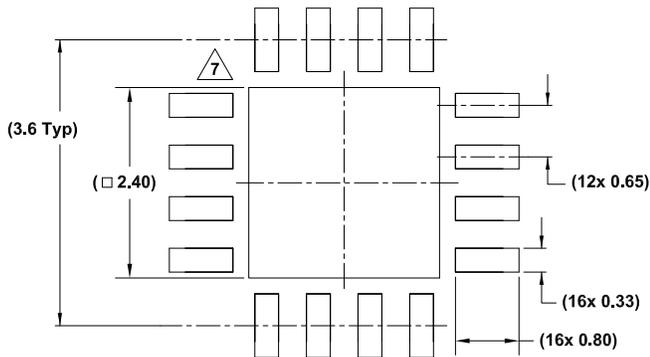
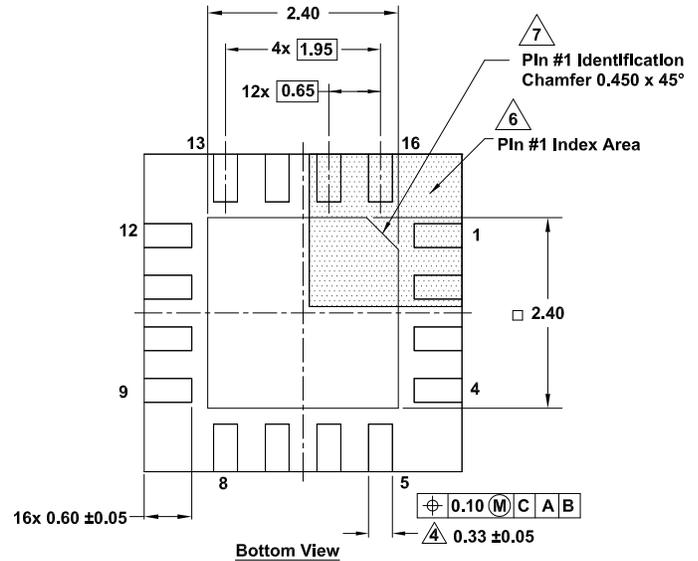
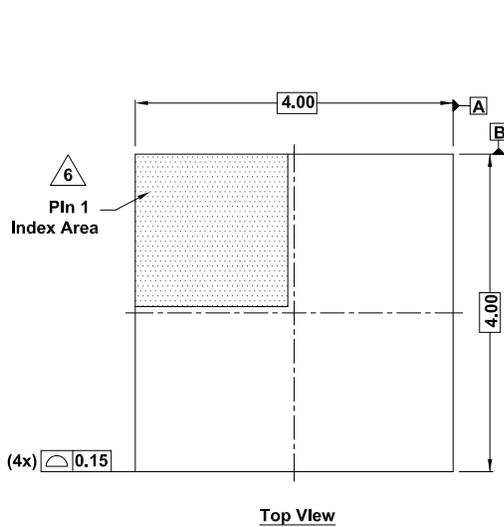
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 3, 2020	4.00	Updated links throughout. Removed ISL1557AIUEZ information throughout document. Updated POD L16.4x4H to the latest revision, changes are as follows: -Added note 7 and the Note 7 references to bottom view and Typ Pattern view -Removed "base plane" from side view -Updated the lead width dimension from $0.33 \pm 0.02$ to $0.33 \pm 0.05$
Mar 2, 2018	3.00	-Added Related Literature section on page 1. -Added Notes 1, 2, and 3 on page 2. -Updated package outline drawing on page 10. -Removed About Intersil section and added Renesas disclaimer.
Dec 9, 2015	2.00	- Updated Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage.

# Package Outline Drawing

For the most recent package outline drawing, see [L16.4x4H](#).

L16.4x4H  
 16 Lead Quad Flat No-Lead Plastic Package  
 Rev 1, 7/20



**Notes:**

1. Dimensions are in millimeters.  
 Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.
7. Pin 1 corner chamfer not required.

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(Rev.1.0 Mar 2020)

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