

# CA-IS376x High-Speed Six-Channel Digital Isolators

## 1. Features

- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: >40 years
  - Up to 3750 V<sub>RMS</sub> isolation rating
  - ±50 kV/μs typical CMTI
  - Schmitt trigger inputs
- **Interfaces Directly with Most MCUs and FPGAs**
  - Data rate: DC to 150Mbps
  - Accepts 2.5V to 5.5V supplies
  - Default output *High* (CA-IS376xH) and *Low* (CA-IS376xL) Options
- **Low Power Consumption**
  - 1.5mA per channel at 1Mbps with V<sub>DD</sub> = 5.0V
  - 6.6mA per channel at 100Mbps with V<sub>DD</sub> = 5.0V
- **Best in class propagation delay and skew**
  - 12ns typical propagation delay
  - 1ns pulse width distortion
  - 2ns propagation delay skew (chip -to-chip)
  - 5ns minimum pulse width
- **No Start-Up Initialization Required**
- **Wide operating temperature range: -40°C to 125°C**
- **Narrow-body SSOP16(B) package**
- **Safety Regulatory Approvals**
  - VDE 0884-11 isolation certification
  - UL According to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

## 2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated SPI etc. Digital Interfaces

## 3. General Description

The CA-IS376x devices are high-performance six-channel, unidirectional digital isolators with up to 3.75kV<sub>RMS</sub> isolation rating and ultra-fast data rate. The CA-IS376x devices offer high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity.

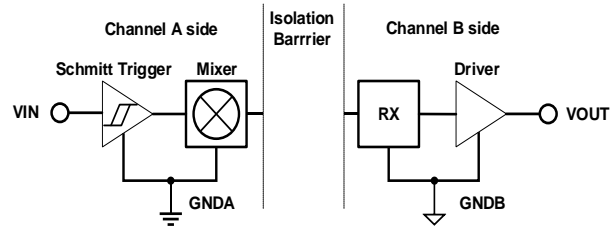
The CA-IS376x family offers all possible unidirectional channel configurations to accommodate any 6-channel design digital I/O applications, especial for the multiple SPI devices isolation. The CA-IS3760 features six channels transferring digital signals in one direction; The CA-IS3761 device has five forward and one reverse-direction channels; The CA-IS3762 device offers four forward and two reverse-direction channels; The CA-IS3763 provides further design flexibility with three channels in each direction. All devices of this family feature default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the Ordering Information for suffixes associated with each option.

The CA-IS376x series devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin SSOP narrow body package.

### Device information

Part number	Package	Package size (NOM)
CA-IS3760 CA-IS3761 CA-IS3762 CA-IS3763	SSOP16(B)	4.90 mm × 3.90 mm

Simplified Channel Structure



GND A and GND B are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3760LB	6	0	Low	3.75	No	SSOP16-NB
CA-IS3760HB	6	0	High	3.75	No	SSOP16-NB
CA-IS3761LB	5	1	Low	3.75	No	SSOP16-NB
CA-IS3761HB	5	1	High	3.75	No	SSOP16-NB
CA-IS3762LB	4	2	Low	3.75	No	SSOP16-NB
CA-IS3762HB	4	2	High	3.75	No	SSOP16-NB
CA-IS3763LB	3	3	Low	3.75	No	SSOP16-NB
CA-IS3763HB	3	3	High	3.75	No	SSOP16-NB

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### 5. Revision History

Revision Number	Description	Page Changed
Version 1.0	N/A	N/A
Version 1.01	Changed $V_{IORM}$ to 1414V, changed $V_{IOWM}$ AC RMS value to 1000V and DC value to 1414V. Updated Power Ratings table.	7, 11, 12, 13
Version 1.02	Added CA-IS3760HB, CA-IS3761LB, CA-IS3761HB, CA-IS3763HB part number. Revised pin descriptions. Updated 7.5, 7.9	1,2 4 6,10,11,12

## 6. Pin Configuration and Description

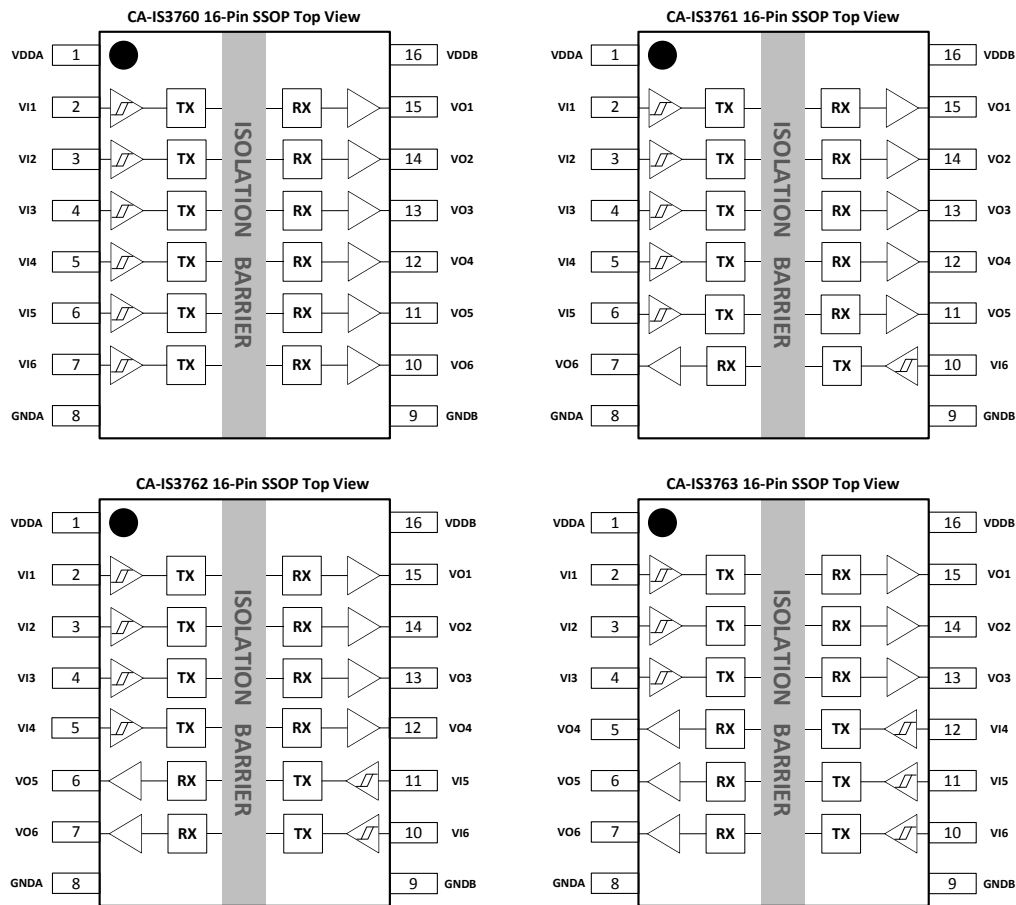


Figure 6-1. CA-IS376x pin configuration

Table 6-1. CA-IS376x pin description

16-SOIC & 16-SSOP Pin#				Name	Type	Description
CA-IS3760	CA-IS3761	CA-IS3762	CA-IS3763			
1	1	1	1	VDDA	Supply	Power supply for side A.
2	2	2	2	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
3	3	3	3	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
4	4	4	4	VI3	Digital I/O	Digital input 3 on side A, corresponds to logic output 3 on side B.
5	5	5	12	VI4	Digital I/O	Digital input 4 on side A/B, corresponds to logic output 4 on side B/A.
6	6	11	11	VI5	Digital I/O	Digital input 5 on side A/B, corresponds to logic output 5 on side B/A.
7	10	10	10	VI6	Digital I/O	Digital input 6 on side A/B, corresponds to logic output 6 on side B/A.
8	8	8	8	GNDA	Ground	Ground reference for side A.
9	9	9	9	GNDB	Ground	Ground reference for side B.
10	7	7	7	VO6	Digital I/O	Digital output 6 on side B/A, VO6 is the logic output for the VI6 input on side A/B.
11	11	6	6	VO5	Digital I/O	Digital output 5 on side B/A, VO5 is the logic output for the VI5 input on side A/B.
12	12	12	5	VO4	Digital I/O	Digital output 4 on side B/A, VO4 is the logic output for the VI4 input on side A/B.
13	13	13	13	VO3	Digital I/O	Digital output 3 on side B, VO3 is the logic output for the VI3 input on side A.
14	14	14	14	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
15	15	15	15	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	16	16	16	VDDB	Supply	Power supply for side B.

**7. Specifications**
**7.1. Absolute Maximum Ratings<sup>1</sup>**

Parameters		Minimum value	Maximum value	Unit
$V_{DDA}, V_{DDB}$	Power supply voltage <sup>2</sup>	-0.5	7.0	V
$V_{IN}$	Voltage at $VI_x, VO_x, EN_x$	-0.5	$V_{DD} + 0.5$ <sup>3</sup>	V
$I_O$	Output current	-20	20	mA
$T_J$	Junction temperature		150	°C
$T_{STG}$	Storage temperature range	-65	150	°C

**Notes:**

- The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 7 V.

**7.2. ESD Ratings**

			Numerical value	Unit
$V_{ESD}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>1</sup>		±6000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins <sup>2</sup>		±2000	V

**Notes:**

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

**7.3. Recommended Operating Conditions**

PARAMETER		MIN	TYPE	MAX	UNIT
$V_{DDA}, V_{DDB}$	Supply voltage on side A, B	2.375	3.3/5.0	5.50	V
$V_{DD(UVLO+)}$	$V_{DD}$ Undervoltage-Lockout Threshold When Supply Voltage is Rising	1.95	2.24	2.375	V
$V_{DD(UVLO-)}$	$V_{DD}$ Undervoltage-Lockout Threshold When Supply Voltage is Falling	1.88	2.10	2.325	V
$V_{HYS(UVLO)}$	$V_{DD}$ Undervoltage-Lockout Threshold Hysteresis	70	140	250	mV
$I_{OH}$	High-level Output Current	$V_{DDO}^1 = 5V$		-4	mA
		$V_{DDO} = 3.3V$		-2	
		$V_{DDO} = 2.5V$		-1	
$I_{OL}$	Low-level Output Current	$V_{DDO} = 5V$		4	mA
		$V_{DDO} = 3.3V$		2	
		$V_{DDO} = 2.5V$		1	
$V_{IH}$	High-level Input Voltage	2.0			V
$V_{IL}$	Low-level Input Voltage			0.8	V
DR	Data Rate	0		150	Mbps
$T_A$	Ambient Temperature	-40	27	125	°C

**Note:**

- $V_{DDO}$  = Output-side supply  $V_{DD}$ .

**7.4. Thermal Information**

Thermal Metric	CA-IS376x	Unit
	SSOP16-NB(B)	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	110	°C/W

**7.5. Power Rating**

Parameters	Test conditions	MIN	TYPE	MAX	Unit
<b>CA-IS3760</b>					
$P_D$ Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5\text{ V}$ , $C_L = 15\text{ pF}$ , $T_J = 150^\circ\text{C}$ , Input a 75-MHz 50% duty cycle square wave.			494	mW
$P_{DA}$ Maximum Power Dissipation on Side-A				49	mW
$P_{DB}$ Maximum Power Dissipation on Side-B				445	mW
<b>CA-IS3761</b>					
$P_D$ Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5\text{ V}$ , $C_L = 15\text{ pF}$ , $T_J = 150^\circ\text{C}$ , Input a 75-MHz 50% duty cycle square wave.			494	mW
$P_{DA}$ Maximum Power Dissipation on Side-A				113	mW
$P_{DB}$ Maximum Power Dissipation on Side-B				381	mW
<b>CA-IS3762</b>					
$P_D$ Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5\text{ V}$ , $C_L = 15\text{ pF}$ , $T_J = 150^\circ\text{C}$ , Input a 75-MHz 50% duty cycle square wave.			494	mW
$P_{DA}$ Maximum Power Dissipation on Side-A				180	mW
$P_{DB}$ Maximum Power Dissipation on Side-B				314	mW
<b>CA-IS3763</b>					
$P_D$ Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5\text{ V}$ , $C_L = 15\text{ pF}$ , $T_J = 150^\circ\text{C}$ , Input a 75-MHz 50% duty cycle square wave.			494	mW
$P_{DA}$ Maximum Power Dissipation on Side-A				247	mW
$P_{DB}$ Maximum Power Dissipation on Side-B				247	mW

**7.6. Insulation Specifications**

Parameters		Test conditions	Value	Unit
			B	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	4	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 300 V_{RMS}$	I-III	
		Rated mains voltage $\leq 400 V_{RMS}$	I-III	
		Rated mains voltage $\leq 600 V_{RMS}$	N/A	
<b>DIN V VDE V 0884-11:2017-01<sup>1</sup></b>				
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	$V_{PK}$
$V_{IOWM}$	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	$V_{RMS}$
		DC voltage	566	$V_{DC}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$ , t=1 s (100% product test)	5300	$V_{PK}$
$V_{IOSM}$	Maximum surge isolation voltage <sup>2</sup>	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	5000	$V_{PK}$
$q_{pd}$	Apparent charge <sup>3</sup>	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10$ s	$\leq 5$	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10$ s	$\leq 5$	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1$ s; $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1$ s	$\leq 5$	
$C_{IO}$	Barrier capacitance, input to output <sup>4</sup>	$V_{IO} = 0.4 \times \sin(2\pi ft)$ , f = 1 MHz	~0.5	pF
$R_{IO}$	Isolation resistance <sup>4</sup>	$V_{IO} = 500$ V, $T_A = 25^\circ\text{C}$	$>10^{12}$	$\Omega$
		$V_{IO} = 500$ V, $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$>10^{11}$	
		$V_{IO} = 500$ V at $T_S = 150^\circ\text{C}$	$>10^9$	
	Pollution degree		2	
<b>UL 1577</b>				
$V_{ISO}$	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1 s (100% production test)	3750	$V_{RMS}$
<b>Notes:</b>				
1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. 2. Devices are immersed in oil during surge characterization test. 3. The characterization charge is discharging charge (pd) caused by partial discharge. 4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

**7.7. Safety-Related Certifications (pending)**

VDE	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017

**7.8. Electrical Characteristics**
 **$V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
$V_{OH}$	High-level Output Voltage	$I_{OH} = -4\text{mA}$ ; See Figure 8-2	$V_{DDO}^{1-0.4}$	4.8		V
$V_{OL}$	Low-level Output Voltage	$I_{OL} = 4\text{mA}$ ; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
$I_{IH}$	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	$\mu\text{A}$
$I_{IL}$	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			$\mu\text{A}$
$Z_O$	Output Impedance <sup>2</sup>			50		$\Omega$
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}^{1}$ or 0 V, $V_{CM} = 1200\text{V}$ ; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
$C_I$	Input Capacitance <sup>3</sup>	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{DD} = 5\text{ V}$		2		pF

**Notes:**

- $V_{DDI}$  = Input-side supply  $V_{DD}$ ,  $V_{DDO}$  = Output-side supply  $V_{DD}$ .
- The nominal output impedance of each isolator driver is  $50\ \Omega \pm 40\%$ .
- Measured from pin to Ground.

 **$V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
$V_{OH}$	High-level Output Voltage	$I_{OH} = -4\text{mA}$ ; See Figure 8-2	$V_{DDO}^{1-0.4}$	3.1		V
$V_{OL}$	Low-level Output Voltage	$I_{OL} = 4\text{mA}$ ; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.5	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
$I_{IH}$	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	$\mu\text{A}$
$I_{IL}$	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			$\mu\text{A}$
$Z_O$	Output Impedance <sup>2</sup>			50		$\Omega$
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}^{1}$ or 0 V, $V_{CM} = 1200\text{V}$ ; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
$C_I$	Input Capacitance <sup>3</sup>	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{DD} = 3.3\text{ V}$		2		pF

**Notes:**

- $V_{DDI}$  = Input-side supply  $V_{DD}$ ,  $V_{DDO}$  = Output-side supply  $V_{DD}$ .
- The nominal output impedance of each isolator driver is  $50\ \Omega \pm 40\%$ .
- Measured from pin to Ground.

 **$V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
$V_{OH}$	High-level Output Voltage	$I_{OH} = -4\text{mA}$ ; See Figure 8-2	$V_{DDO}^{1-0.4}$	2.3		V
$V_{OL}$	Low-level Output Voltage	$I_{OL} = 4\text{mA}$ ; See Figure 8-2		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
$I_{IH}$	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	$\mu\text{A}$
$I_{IL}$	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-20			$\mu\text{A}$
$Z_O$	Output Impedance <sup>2</sup>			50		$\Omega$
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}^{1}$ or 0 V, $V_{CM} = 1200\text{V}$ ; See Figure 8-3		50		$\text{kV}/\mu\text{s}$
$C_I$	Input Capacitance <sup>3</sup>	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{DD} = 2.5\text{ V}$		2		pF

**Notes:**

- $V_{DDI}$  = Input-side supply  $V_{DD}$ ,  $V_{DDO}$  = Output-side supply  $V_{DD}$ .
- The nominal output impedance of each isolator driver is  $50\ \Omega \pm 40\%$ .
- Measured from pin to Ground.



**7.9. Supply Current Characteristics**
 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>CA-IS3760</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)	$I_{DDA}$		2.0	2.9	mA	
		$I_{DDB}$		3.9	5.7		
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0\text{V}$ (CA-IS3760H)	$I_{DDA}$		7.0	10.7		
		$I_{DDB}$		4.1	6.1		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.5		6.8
			$I_{DDB}$		6.3		9.3
		10Mbps (5MHz)	$I_{DDA}$		4.8		7.2
			$I_{DDB}$		26.9		40.6
		100Mbps (50MHz)	$I_{DDA}$		6.4	9.5	
			$I_{DDB}$		59.0	80	
<b>CA-IS3761</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)	$I_{DDA}$		2.3	3.4	mA	
		$I_{DDB}$		3.6	5.3		
	$V_{IN} = V_{DDI}^1$ (CA-IS3761L); $V_{IN} = 0\text{V}$ (CA-IS3761H)	$I_{DDA}$		6.5	9.9		
		$I_{DDB}$		4.6	6.9		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.5		6.7
			$I_{DDB}$		5.7		8.4
		10Mbps (5MHz)	$I_{DDA}$		5.1		7.6
			$I_{DDB}$		19.8		29.9
		100Mbps (50MHz)	$I_{DDA}$		10.6	16.3	
			$I_{DDB}$		45.6	62.1	
<b>CA-IS3762</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L); $V_{IN} = V_{DDI}^1$ (CA-IS3762H)	$I_{DDA}$		2.8	4.5	mA	
		$I_{DDB}$		3.8	5.8		
	$V_{IN} = V_{DDI}^1$ (CA-IS3762L); $V_{IN} = 0\text{V}$ (CA-IS3762H)	$I_{DDA}$		6.2	9.9		
		$I_{DDB}$		5.6	8.7		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		5.4		8.3
			$I_{DDB}$		6.3		9.5
		10Mbps (5MHz)	$I_{DDA}$		13.1		18.3
			$I_{DDB}$		21.0		31.5
		100Mbps (50MHz)	$I_{DDA}$		26.0	36.9	
			$I_{DDB}$		44.7	72.2	
<b>CA-IS3763</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L); $V_{IN} = V_{DDI}^1$ (CA-IS3763H)	$I_{DDA}$		2.9	4.4	mA	
		$I_{DDB}$		2.9	4.4		
	$V_{IN} = V_{DDI}^1$ (CA-IS3763L); $V_{IN} = 0\text{V}$ (CA-IS3763H)	$I_{DDA}$		5.5	8.4		
		$I_{DDB}$		5.5	8.4		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.3		6.5
			$I_{DDB}$		4.3		6.5
		10Mbps (5MHz)	$I_{DDA}$		5.7		8.4
			$I_{DDB}$		5.7		8.4
		100Mbps (50MHz)	$I_{DDA}$		19.9	30.0	
			$I_{DDB}$		19.9	30.0	
<b>Note:</b>							
1. $V_{DDI}^1$ = Input-side supply $V_{DD}$ .							

$V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>CA-IS3760</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)	$I_{DDA}$		1.9	2.8	mA	
		$I_{DDB}$		3.6	5.4		
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0\text{V}$ (CA-IS3760H)	$I_{DDA}$		6.8	10.5		
		$I_{DDB}$		3.9	5.7		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.4		6.7
			$I_{DDB}$		5.2		7.5
		10Mbps (5MHz)	$I_{DDA}$		4.6		7.0
			$I_{DDB}$		18.3		24.6
		100Mbps (50MHz)	$I_{DDA}$		6.1	9.0	
			$I_{DDB}$		38.3	51.8	
<b>CA-IS3761</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)	$I_{DDA}$		2.2	3.2	mA	
		$I_{DDB}$		3.4	5.0		
	$V_{IN} = V_{DDI}^1$ (CA-IS3761L); $V_{IN} = 0\text{V}$ (CA-IS3761H)	$I_{DDA}$		6.3	9.7		
		$I_{DDB}$		4.4	6.5		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.3		6.5
			$I_{DDB}$		4.8		7.1
		10Mbps (5MHz)	$I_{DDA}$		4.8		7.1
			$I_{DDB}$		13.9		18.9
		100Mbps (50MHz)	$I_{DDA}$		8.6	12.2	
			$I_{DDB}$		30.1	40.8	
<b>CA-IS3762</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L); $V_{IN} = V_{DDI}^1$ (CA-IS3762H)	$I_{DDA}$		2.7	4.3	mA	
		$I_{DDB}$		3.6	5.6		
	$V_{IN} = V_{DDI}^1$ (CA-IS3762L); $V_{IN} = 0\text{V}$ (CA-IS3762H)	$I_{DDA}$		6.0	9.7		
		$I_{DDB}$		5.4	8.4		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.9		7.7
			$I_{DDB}$		5.6		8.5
		10Mbps (5MHz)	$I_{DDA}$		10.0		14.3
			$I_{DDB}$		15.2		22.7
		100Mbps (50MHz)	$I_{DDA}$		18.5	26.2	
			$I_{DDB}$		30.4	48.1	
<b>CA-IS3763</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L); $V_{IN} = V_{DDI}^1$ (CA-IS3763H)	$I_{DDA}$		2.7	4.1	mA	
		$I_{DDB}$		2.7	4.1		
	$V_{IN} = V_{DDI}^1$ (CA-IS3763L); $V_{IN} = 0\text{V}$ (CA-IS3763H)	$I_{DDA}$		5.3	8.1		
		$I_{DDB}$		5.3	8.1		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.1		6.2
			$I_{DDB}$		4.1		6.2
		10Mbps (5MHz)	$I_{DDA}$		5.1		7.4
			$I_{DDB}$		5.1		7.4
		100Mbps (50MHz)	$I_{DDA}$		13.6	18.7	
			$I_{DDB}$		13.6	18.7	
<b>Note:</b>							
1. $V_{DDI} = \text{Input-side supply } V_{DD}$ .							

$V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>CA-IS3760</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)	$I_{DDA}$		1.9	2.7	mA	
		$I_{DDB}$		3.6	5.2		
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0\text{V}$ (CA-IS3760H)	$I_{DDA}$		6.8	10.4		
		$I_{DDB}$		3.8	5.5		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.3		6.6
			$I_{DDB}$		4.8		6.9
		10Mbps (5MHz)	$I_{DDA}$		4.6		6.9
			$I_{DDB}$		14.7		19.8
		100Mbps (50MHz)	$I_{DDA}$		5.7	8.5	
			$I_{DDB}$		28.9	39.0	
<b>CA-IS3761</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)	$I_{DDA}$		2.1	3.2	mA	
		$I_{DDB}$		3.3	4.8		
	$V_{IN} = V_{DDI}^1$ (CA-IS3761L); $V_{IN} = 0\text{V}$ (CA-IS3761H)	$I_{DDA}$		6.3	9.6		
		$I_{DDB}$		4.3	6.4		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.3		6.4
			$I_{DDB}$		4.5		6.6
		10Mbps (5MHz)	$I_{DDA}$		4.6		6.9
			$I_{DDB}$		11.4		15.5
		100Mbps (50MHz)	$I_{DDA}$		7.6	10.8	
			$I_{DDB}$		23.1	31.2	
<b>CA-IS3762</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L); $V_{IN} = V_{DDI}^1$ (CA-IS3762H)	$I_{DDA}$		2.6	4.2	mA	
		$I_{DDB}$		3.5	5.5		
	$V_{IN} = V_{DDI}^1$ (CA-IS3762L); $V_{IN} = 0\text{V}$ (CA-IS3762H)	$I_{DDA}$		6.0	9.6		
		$I_{DDB}$		5.3	8.3		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.8		7.4
			$I_{DDB}$		5.2		8.0
		10Mbps (5MHz)	$I_{DDA}$		8.6		12.4
			$I_{DDB}$		12.6		18.6
		100Mbps (50MHz)	$I_{DDA}$		14.8	21.2	
			$I_{DDB}$		23.3	36.3	
<b>CA-IS3763</b>							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L); $V_{IN} = V_{DDI}^1$ (CA-IS3763H)	$I_{DDA}$		2.7	4.0	mA	
		$I_{DDB}$		2.7	4.0		
	$V_{IN} = V_{DDI}^1$ (CA-IS3763L); $V_{IN} = 0\text{V}$ (CA-IS3763H)	$I_{DDA}$		5.2	8.0		
		$I_{DDB}$		5.2	8.0		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel.	1Mbps (500kHz)	$I_{DDA}$		4.0		6.1
			$I_{DDB}$		4.0		6.1
		10Mbps (5MHz)	$I_{DDA}$		4.8		7.0
			$I_{DDB}$		4.8		7.0
		100Mbps (50MHz)	$I_{DDA}$		11.3	16.0	
			$I_{DDB}$		11.3	16.0	
<b>Note:</b>							
1. $V_{DDI}^1 = \text{Input-side supply } V_{DD}$ .							

**7.10. Timing Characteristics**
 **$V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
$PW_{\min}$	Minimum Pulse Width				5.0	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $ t_{PLH} - t_{PHL} $					
$t_{sk(o)}$	Channel-to-Channel Output Skew Time <sup>1</sup>	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time <sup>2</sup>			2.0	4.5	ns
$t_r$	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
$t_f$	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
$t_{DO}$	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
$t_{SU}$	Start-up Time			15	40	$\mu\text{s}$

**Notes:**

1.  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2.  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

 **$V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
$PW_{\min}$	Minimum Pulse Width				5.0	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $ t_{PLH} - t_{PHL} $					
$t_{sk(o)}$	Channel-to-Channel Output Skew Time <sup>1</sup>	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time <sup>2</sup>			2.0	4.5	ns
$t_r$	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
$t_f$	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
$t_{DO}$	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
$t_{SU}$	Start-up Time			15	40	$\mu\text{s}$

**Notes:**

1.  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2.  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

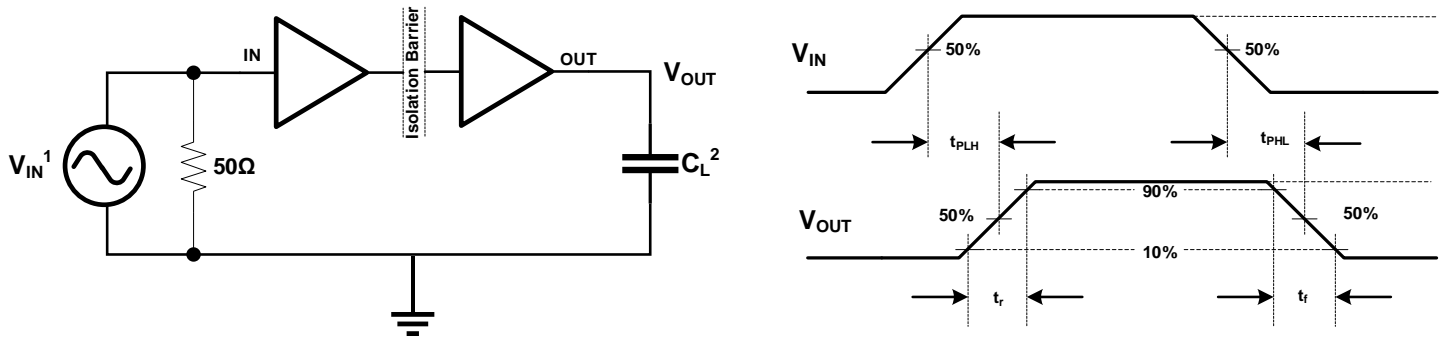
 **$V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125^\circ\text{C}$  (over recommended operating conditions, unless otherwise specified)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
$PW_{\min}$	Minimum Pulse Width				5.0	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $ t_{PLH} - t_{PHL} $					
$t_{sk(o)}$	Channel-to-Channel Output Skew Time <sup>1</sup>	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to Part Output Skew Time <sup>2</sup>			1.0	5.0	ns
$t_r$	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
$t_f$	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
$t_{DO}$	Default Output Delay Time from Input Power Loss	See Figure 8-2		8	12	ns
$t_{SU}$	Start-up Time			15	40	$\mu\text{s}$

**Notes:**

1.  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2.  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

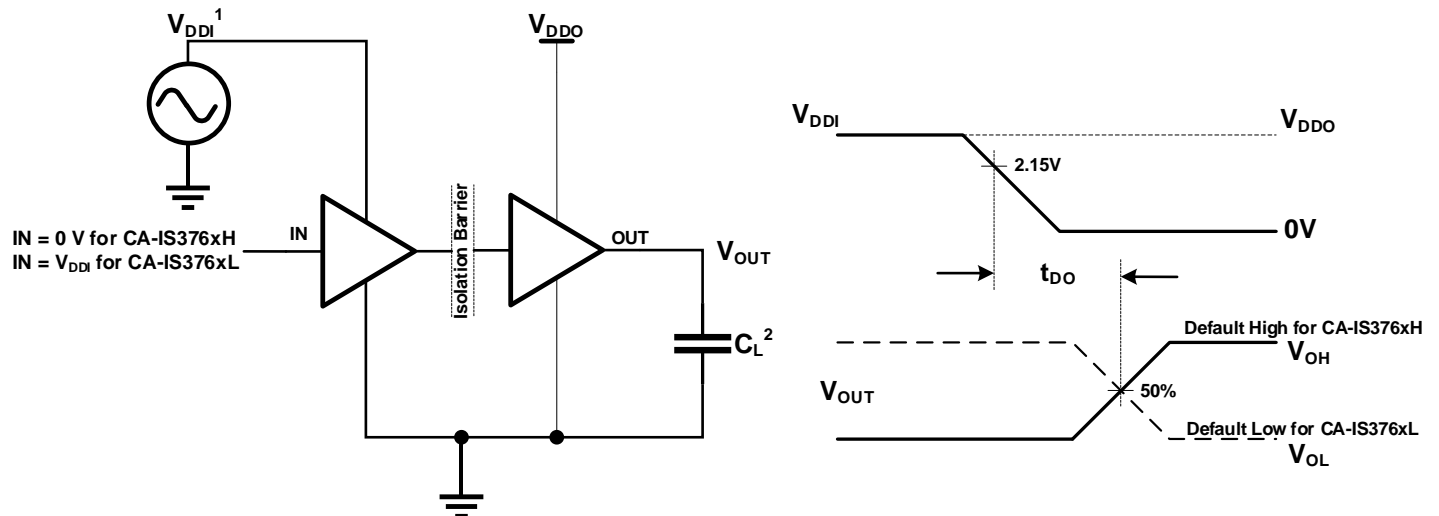
**8. Parameter Measurement Information**



**Notes:**

1. A square wave generator provide  $V_{IN}$  input signal with the following characteristics: frequency  $\leq 100\text{kHz}$ , 50% duty cycle,  $t_r \leq 3\text{ns}$ ,  $t_f \leq 3\text{ns}$ ,  $Z_{out} = 50\Omega$ . At the input,  $50\Omega$  resistor is required to terminate input generator signal. It is not needed in actual application.
2.  $C_L = 15\text{pF}$  and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

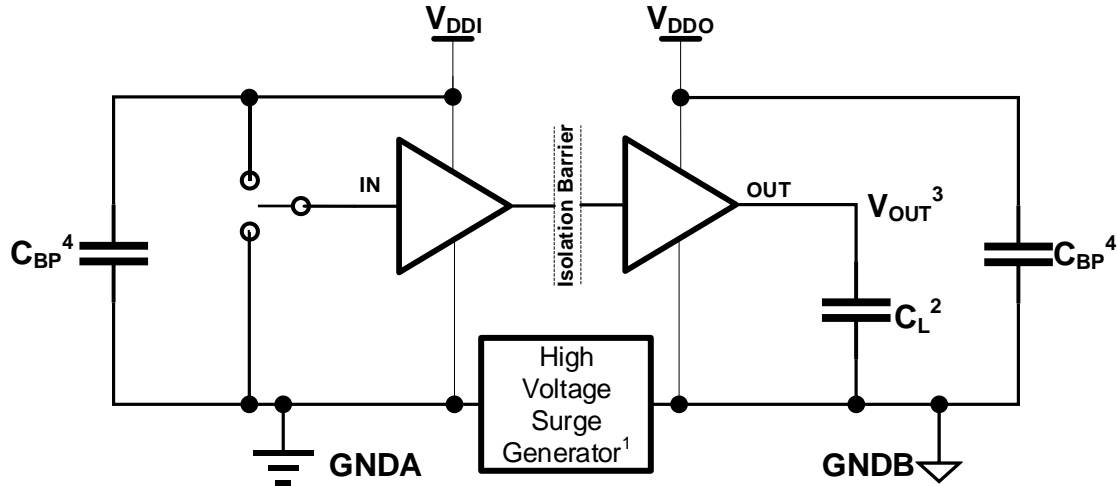
**Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms**



**Notes:**

1. Power Supply Ramp Rate =  $10\text{ mV/ns}$ .  $V_{DDI}$  should ramp over  $2.375\text{V}$ , and less than  $5.5\text{V}$ .
2.  $C_L = 15\text{pF}$  and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

**Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms**



**Notes:**

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 50kV/ $\mu$ s slew rate.
2.  $C_L = 15\text{pF}$  and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4.  $C_{BP}$  (0.1 ~ 1 $\mu$ F) is bypass capacitance.

**Figure 8-3. Common-Mode Transient Immunity Test Circuit**

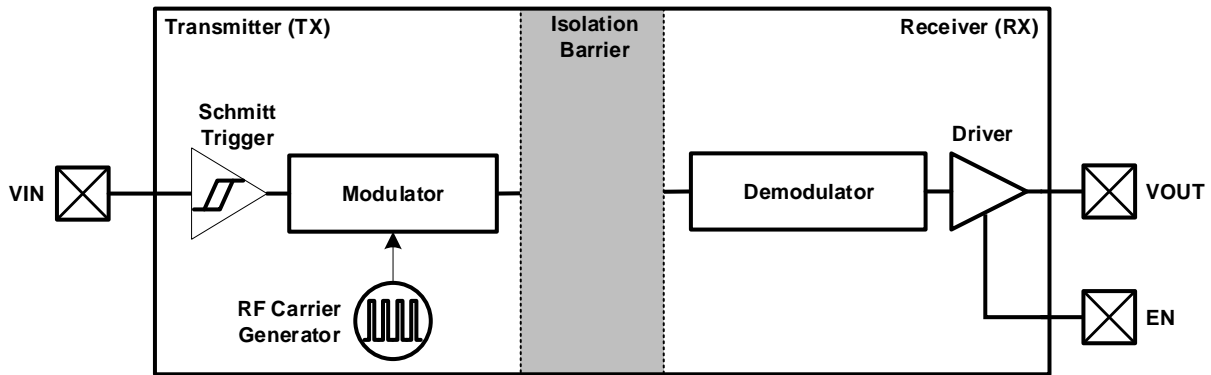
**9. Detailed Description**

**9.1. Overview**

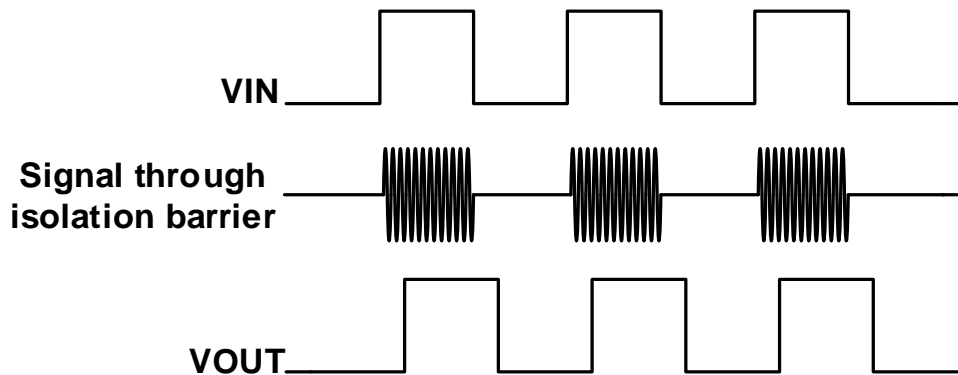
The CA-IS376x are a family of six-channel digital galvanic isolators using Chipanalog’s full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO<sub>2</sub> based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS376x family of devices build a robust data transmission path between different power domains without any special start-up initialization requirements. These devices also incorporate advanced full differential techniques to minimize the radiated emissions due the high frequency carrier and IO buffer switching.

**9.2. Functional Block Diagram**

The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel. Each channel of the CA-IS376x is unidirectional, only passes data in one direction as indicated in the functional diagram. Each device of this family features six unidirectional channels that operate independently with guaranteed data rates from DC up to 150Mbps.



**Figure 9-1. Functional Block Diagram of a Single Channel**



**Figure 9-2. Conceptual Operation Waveforms of a Single Channel**

### 9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS376x devices.

**Table 9-1. Operation Mode**

$V_{DDI}^1$	$V_{DDO}^1$	INPUT (V <sub>Ix</sub> ) <sup>2</sup>	OUTPUT (V <sub>Ox</sub> )	OPERATION
PU	PU	H	H	Normal operation mode: Each channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input V <sub>Ix</sub> is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for CA-IS376xH and Low for CA-IS376xL.
PD	PU	X	Default	Default output mode: When V <sub>DDI</sub> is unpowered, a channel output assumes the logic state based on its default option. Default is <i>High</i> for CA-IS376xH and Low for CA-IS376xL.
X	PD	X	Undetermined	If the output side V <sub>DDO</sub> is unpowered, a channel output is undetermined. <sup>4</sup>
<b>Notes:</b> 1. $V_{DDI}$ = Input-side supply V <sub>DD</sub> ; $V_{DDO}$ = Output-side supply V <sub>DD</sub> ; PU = Powered up ( $V_{DD} \geq V_{DD(UVLO+)}$ ); PD = Powered down ( $V_{DD} \leq V_{DD(UVLO-)}$ ); X = Irrelevant; H = High level; L = Low level; Z = High Impedance. 2. A strongly driven input signal can weakly power the floating V <sub>DD</sub> through an internal protection diode and cause undetermined output.				

## 10. Application and Implementation

The CA-IS376x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The CA-IS376x devices are the high-performance, six-channel digital isolators. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS376x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass V<sub>DDA</sub> and V<sub>ddb</sub> pins with 0.1μF to 1μF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 shows typical operating circuit of the CA-IS37xx series products.

The CA-IS376x family devices do not require special power supply sequencing. The logic levels are set independently on either side by V<sub>DDA</sub> and V<sub>ddb</sub> supply voltage. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance from the design. For the high-speed digital signal circuit boards, we recommend to use the standard FR4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Layer order from top-to-bottom is: high-speed signal layer, ground plane, power plane, and low-frequency signal layer. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.



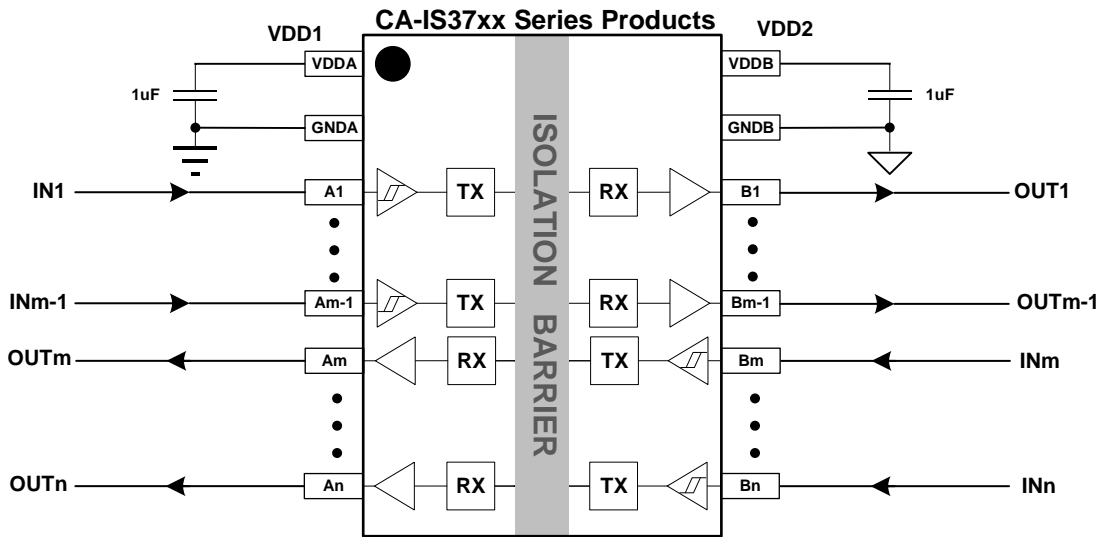
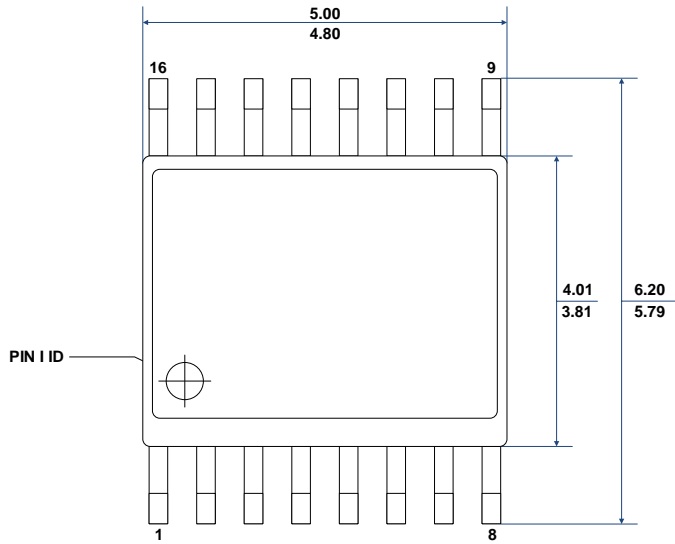


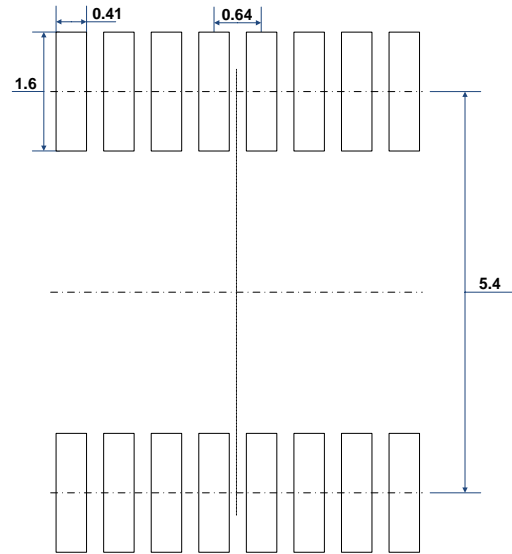
Figure 10-1. Typical Applications for the CA-IS37xx Series Digital Isolators

11. Package Information

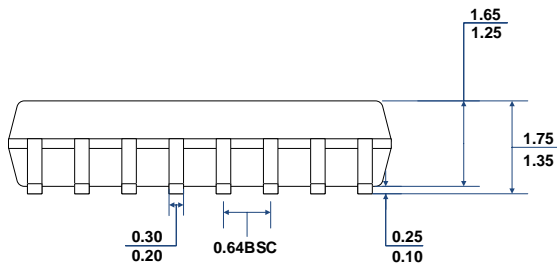
16-Pin Narrow Body SSOP Package Outline



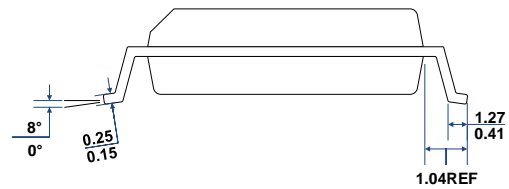
**TOP VIEW**



**RECOMMENDED LAND PATTERN**



**FRONT VIEW**

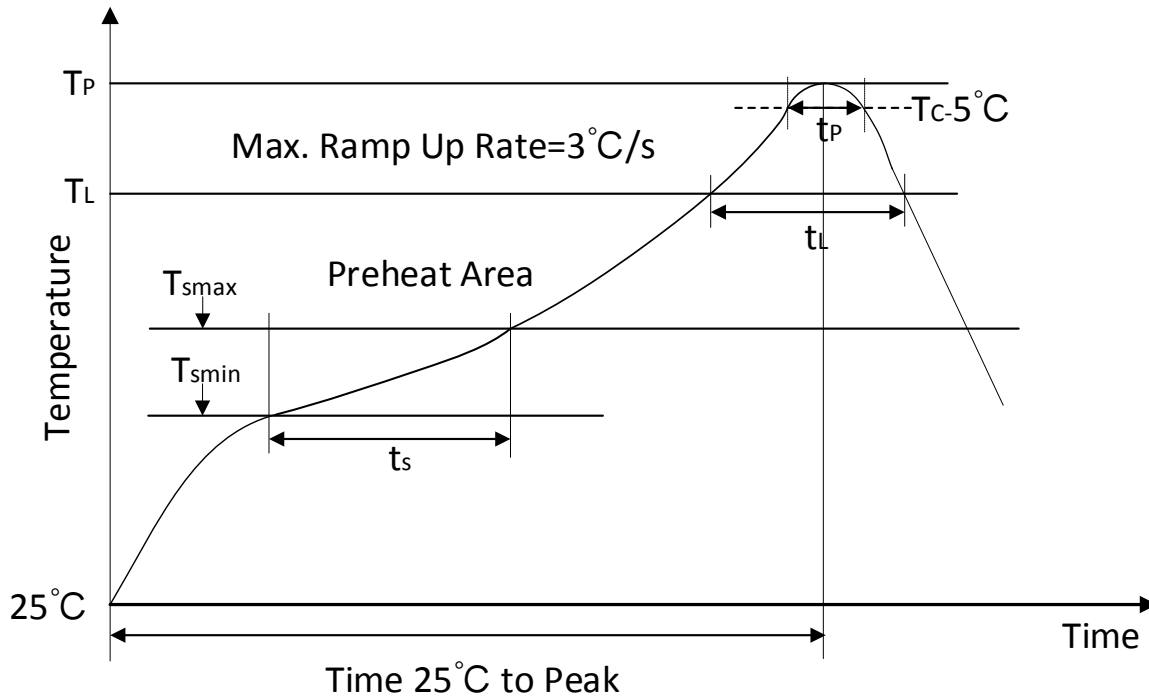


**LEFT-SIDE VIEW**

**Note:**

1. All dimensions are in millimeters, angles are in degrees.

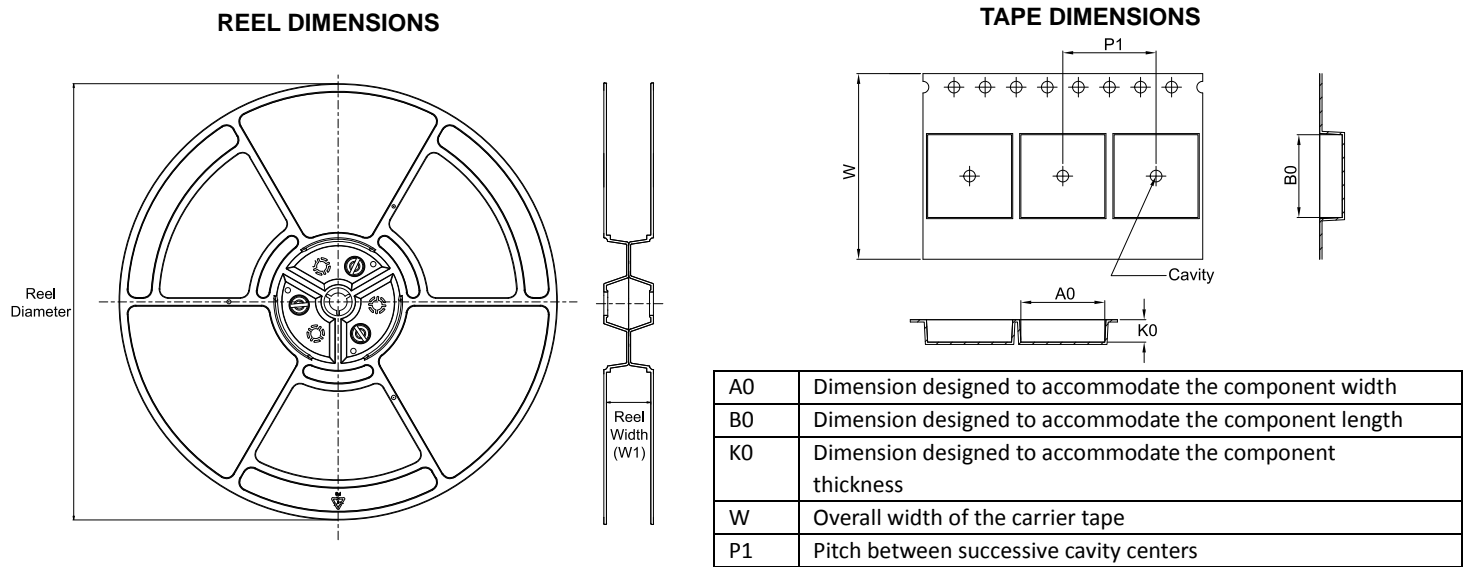
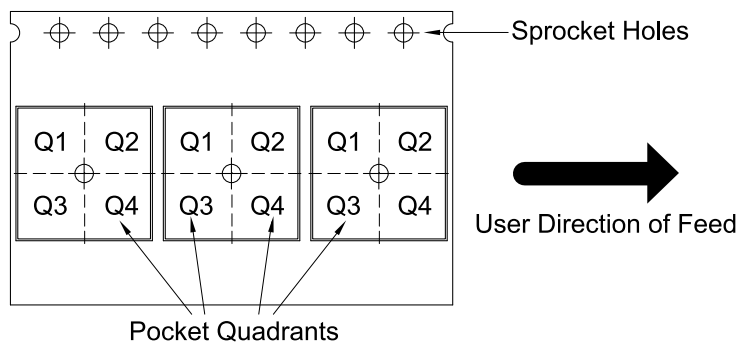
**12. Soldering Temperature (reflow) Profile**



**Figure. 12-1 Soldering Temperature (reflow) Profile**

**Table 12-1 Soldering Temperature Parameter**

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 °C to Peak)	3°C/second max
Time of Preheat temp(from 150 °C to 200 °C)	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5 °C of actual peak temp	30 second
Ramp-down rate	6 °C/second max.
Time from 25°C to peak temp	8 minutes max

**13. Tape and Reel Information**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3760LB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3760HB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3761LB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3761HB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3762LB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3762HB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3763LB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1
CA-IS3763HB	SSOP	B	16	2500	330	12.4	6.55	5.4	1.9	8.0	12.0	Q1

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