

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# SSM3J374R

## 1. Applications

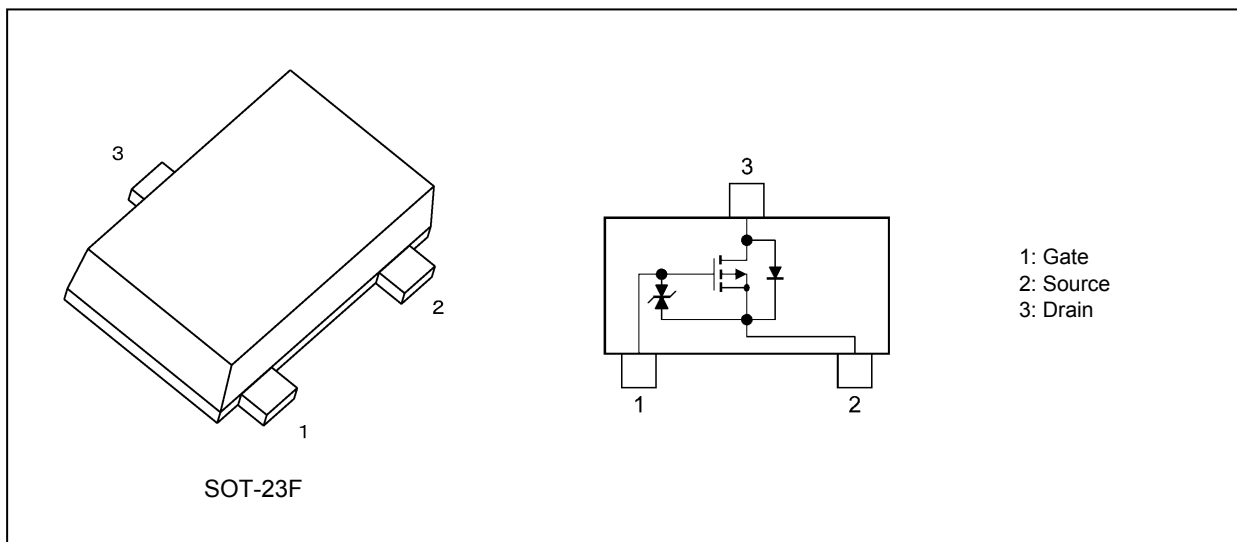
- Power Management Switches

## 2. Features

- (1) AEC-Q101 qualified (Note 1)
- (2) 4.0-V gate drive voltage.
- (3) Low drain-source on-resistance
  - $R_{DS(ON)} = 71 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )
  - $R_{DS(ON)} = 105 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )
  - $R_{DS(ON)} = 136 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.0 \text{ V}$ )

Note 1: For detail information, please contact to our sales.

## 3. Packaging and Pin Assignment



### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-30	V
Gate-source voltage	$V_{GSS}$	-20/+10	
Drain current (DC) (Note 1)	$I_D$	-4	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	-16	
Power dissipation (Note 3)	$P_D$	1	W
Power dissipation ( $t < 10\text{ s}$ ) (Note 3)	$P_D$	2	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Pulse width (PW)  $\leq 1\text{ ms}$ , duty  $\leq 1\%$

Note 3: Device mounted on an FR4 board. (25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu pad: 645 mm<sup>2</sup>)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = -16/+10\text{ V}$ , $V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -30\text{ V}$ , $V_{GS} = 0\text{ V}$	—	—	-1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10\text{ mA}$ , $V_{GS} = 0\text{ V}$	-30	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = -10\text{ mA}$ , $V_{GS} = 10\text{ V}$	-21	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = -10\text{ V}$ , $I_D = -100\text{ }\mu\text{A}$	-0.8	—	-2.0	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = -3.0\text{ A}$ , $V_{GS} = -10\text{ V}$	—	54	71	$\text{m}\Omega$
		$I_D = -2.0\text{ A}$ , $V_{GS} = -4.5\text{ V}$	—	80	105	
		$I_D = -1.0\text{ A}$ , $V_{GS} = -4.0\text{ V}$	—	89	136	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = -10\text{ V}$ , $I_D = -1.0\text{ A}$	2.3	4.6	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	—	280	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	40	—	
Output capacitance	$C_{oss}$		—	55	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = -15\text{ V}$ , $I_D = -1.0\text{ A}$ $V_{GS} = 0\text{ to }-4.5\text{ V}$ , $R_G = 10\text{ }\Omega$ Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ Common source, See Chapter 5.3	—	13	—	ns
Switching time (turn-off time)	$t_{off}$		—	22	—	

#### 5.3. Switching Time Test Circuit

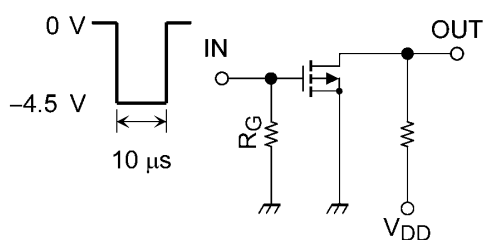


Fig. 5.3.1 Switching Time Test Circuit

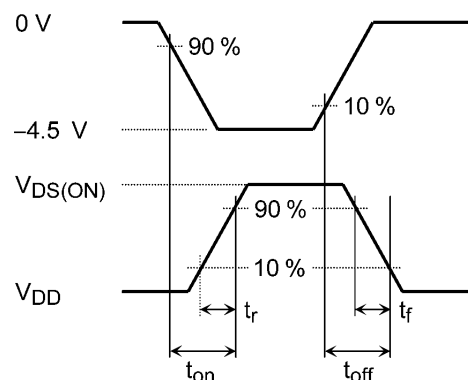


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = -15\text{ V}$ , $V_{GS} = -10\text{ V}$ , $I_D = -4.0\text{ A}$	—	5.9	—	nC
Gate-source charge 1	$Q_{gs1}$		—	0.8	—	
Gate-drain charge	$Q_{gd}$		—	1.2	—	

## 5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = 4.0\text{ A}$ , $V_{GS} = 0\text{ V}$	—	0.9	1.2	V

Note 1: Pulse measurement.

## 6. Marking

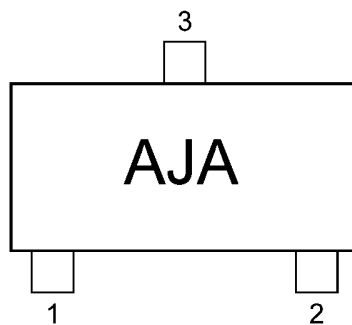


Fig. 6.1 Marking

## 7. Characteristics Curves (Note)

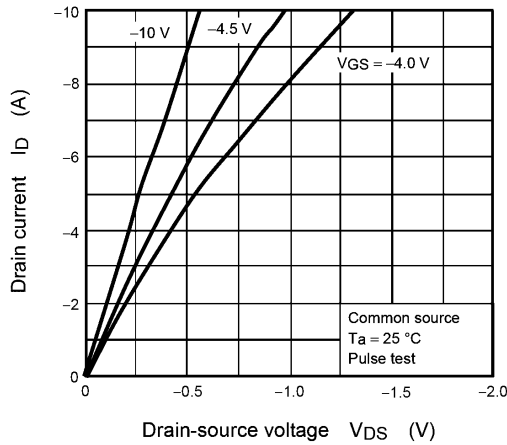


Fig. 7.1  $I_D - V_{DS}$

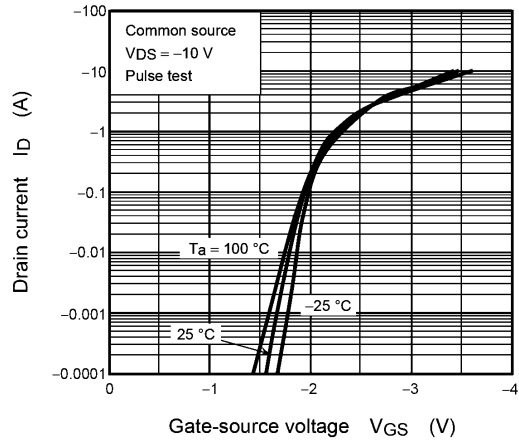


Fig. 7.2  $I_D - V_{GS}$

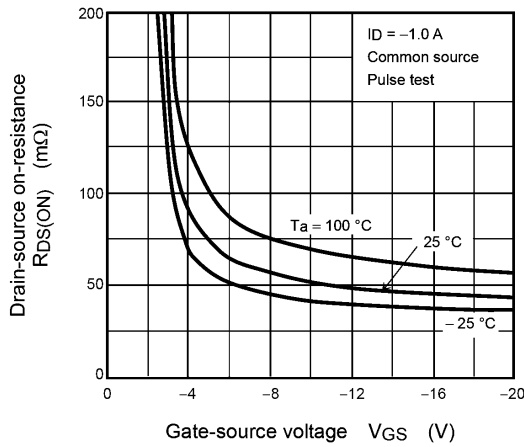


Fig. 7.3  $R_{DS(ON)} - V_{GS}$

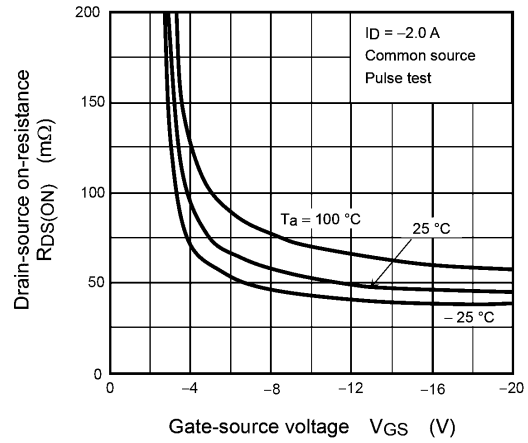


Fig. 7.4  $R_{DS(ON)} - V_{GS}$

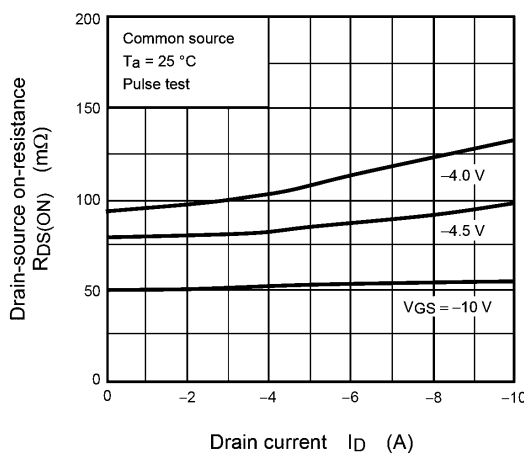


Fig. 7.5  $R_{DS(ON)} - I_D$

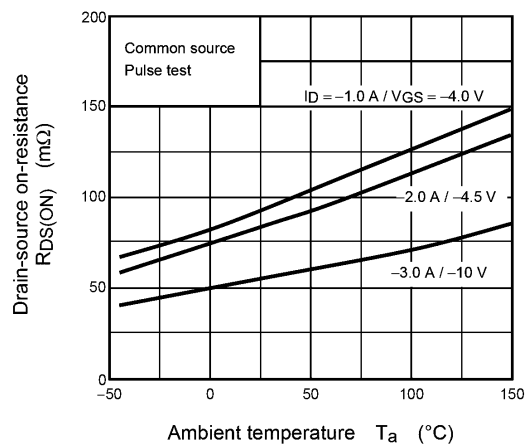
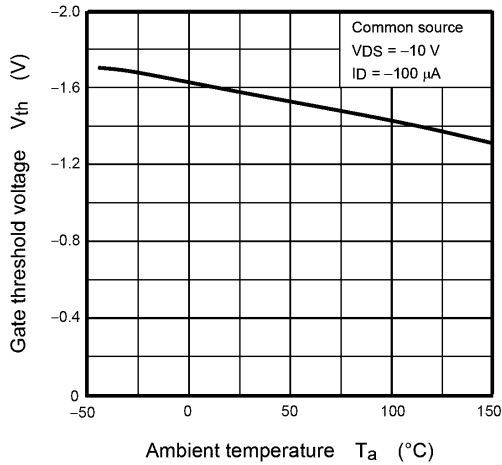
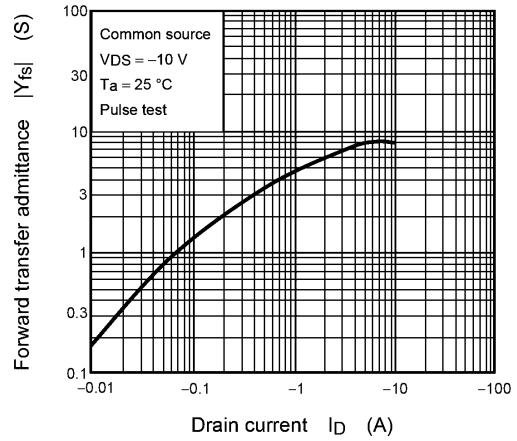


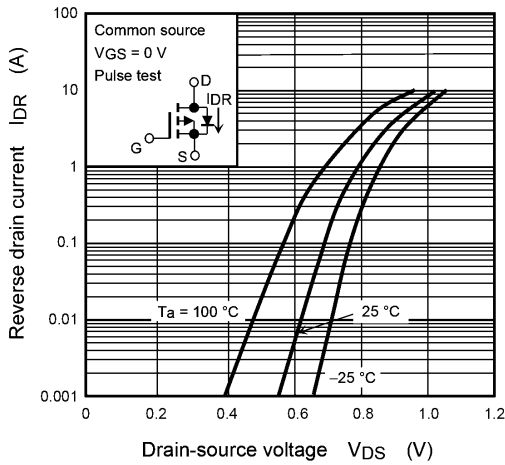
Fig. 7.6  $R_{DS(ON)} - T_a$



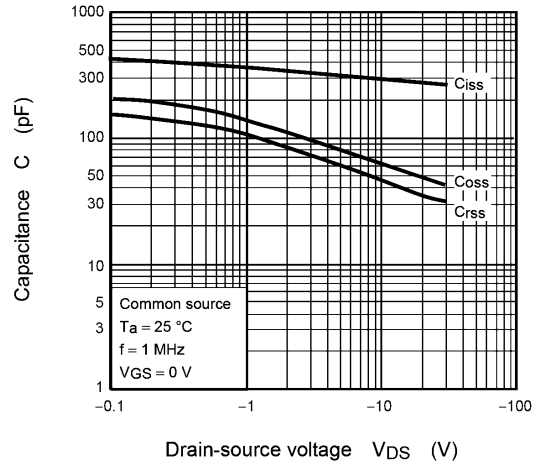
**Fig. 7.7  $V_{th} - T_a$**



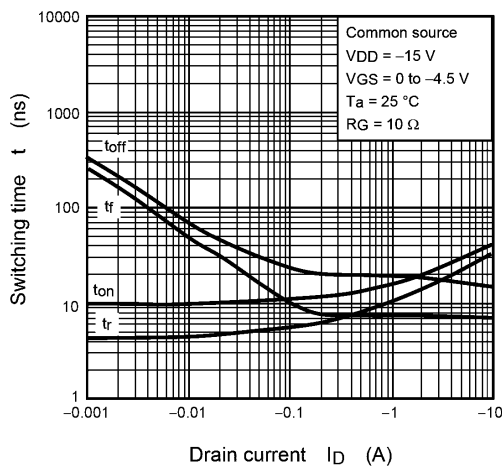
**Fig. 7.8  $|Y_{fs}| - I_D$**



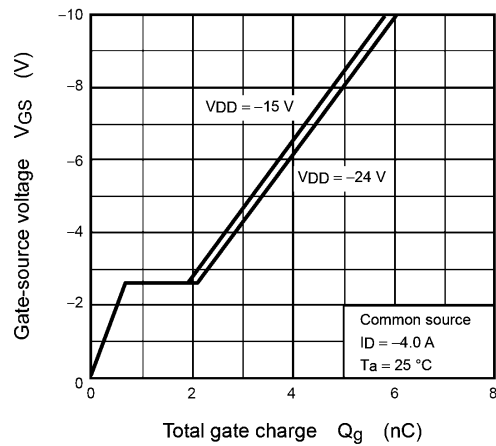
**Fig. 7.9  $I_{DR} - V_{DS}$**



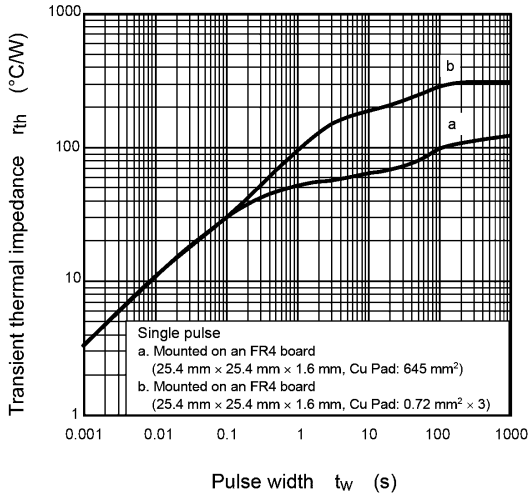
**Fig. 7.10  $C - V_{DS}$**



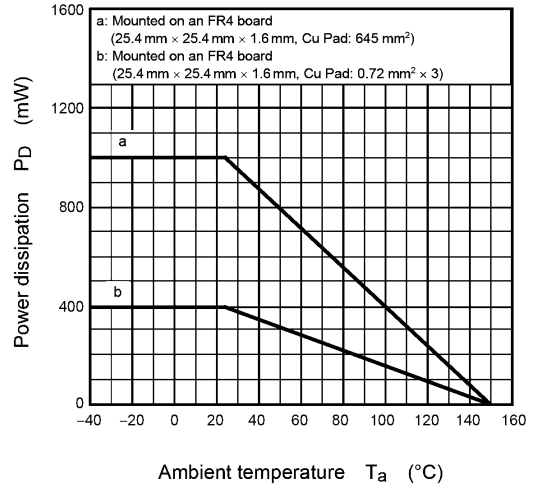
**Fig. 7.11  $t - I_D$**



**Fig. 7.12 Dynamic Input Characteristic**



**Fig. 7.13**  $r_{th} - t_w$



**Fig. 7.14**  $P_D - T_a$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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