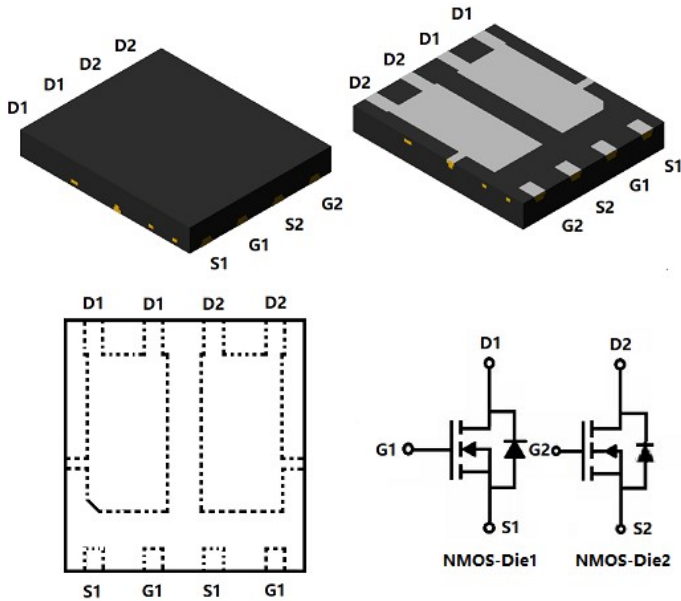


N-Channel Enhancement Mode Field Effect Transistor

DFN5060-8L



Product Summary

NMOS(Die1)

• V_{DS}	100V
• I_D	20A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<22 mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<27 mohm

NMOS(Die2)

• V_{DS}	100V
• I_D	20A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<22 mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<27 mohm

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	N-Die1	N-Die2	Unit
Drain-source Voltage		V_{DS}	100	100	V
Gate-source Voltage		V_{GS}	± 20	± 20	V
Drain Current	$T_C=25^{\circ}C$	I_D	20	20	A
	$T_C=70^{\circ}C$		12.5	12.5	
Pulsed Drain Current ^A		I_{DM}	80	80	A
Avalanche energy ^B		E_{AS}	64	64	mJ
Total Power Dissipation	$T_C=25^{\circ}C$	P_D	17	17	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	-55~+150	$^{\circ}C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	30	40	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		60	75	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	6.2	7.5	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD20G10A	F1	YJGD20G10A	5000	10000	100000	13" reel



YJGD20G10A

■ NMOS(Die1/Die2) Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =15A		17	22	mΩ
		V _{GS} = 4.5V, I _D =7A		21	27	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.96	1.3	V
Maximum Body-Diode Continuous Current	I _S				20	A
Gate Resistance	R _g	f=1MHz		1.2		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		1051		pF
Output Capacitance	C _{oss}			399		
Reverse Transfer Capacitance	C _{rss}			18		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =25A		16		nC
Gate-Source Charge	Q _{gs}			5.6		
Gate-Drain Charge	Q _{gd}			2.4		
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=100A/us		42		
Reverse Recovery Time	t _{rr}			39.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =4.0A R _{GEN} =3.0Ω		39.2		ns
Turn-on Rise Time	t _r			11		
Turn-off Delay Time	t _{D(off)}			53.2		
Turn-off fall Time	t _f			15.8		
Peak reverse recovery corrent	I _{rm}	I _F =4A, di/dt=100A/us		3		A

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=0.5mH, I_D=16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



■ NMOS(Die1/Die2) Typical Performance Characteristics

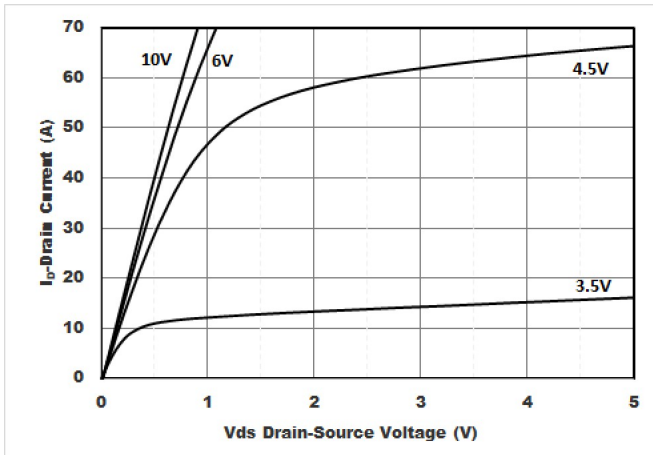


Figure1. Output Characteristics

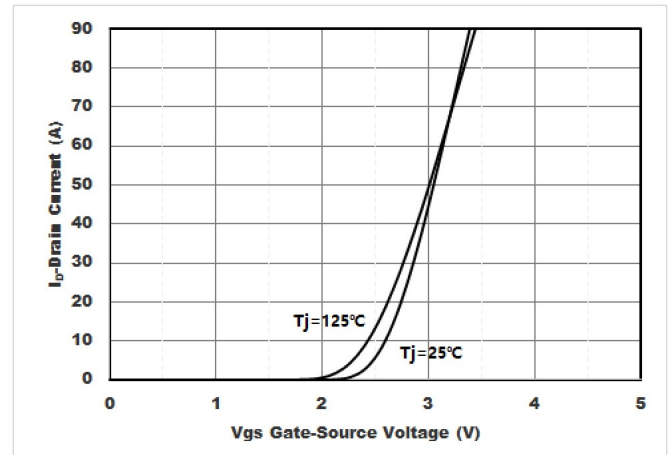


Figure2. Transfer Characteristics

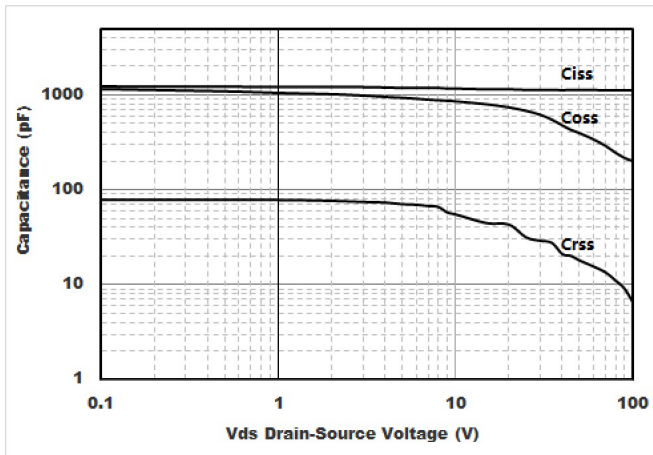


Figure3. Capacitance Characteristics

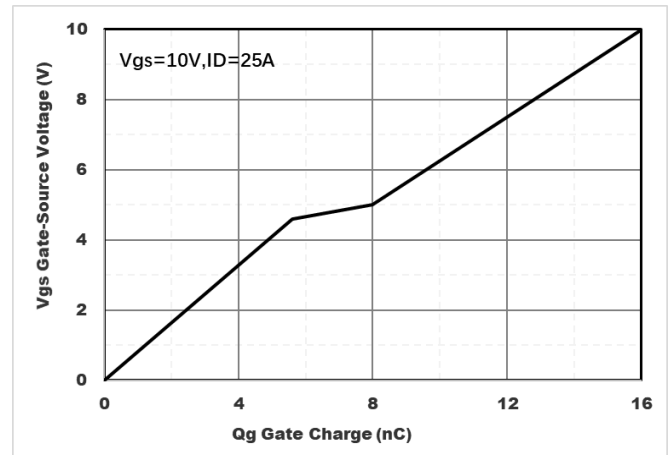


Figure4. Gate Charge

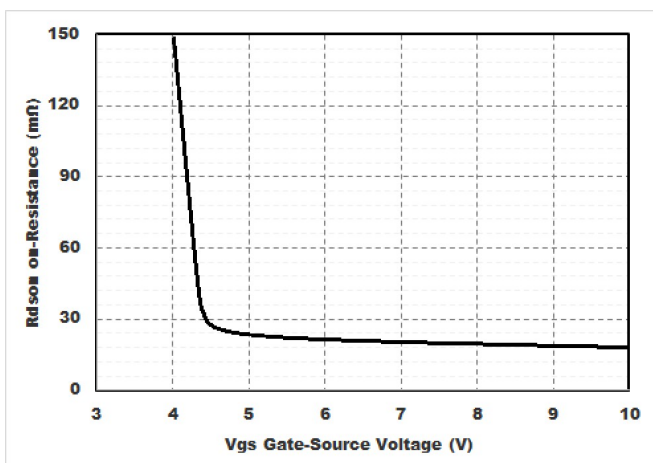


Figure5. : On-Resistance vs. Gate to Source Voltage

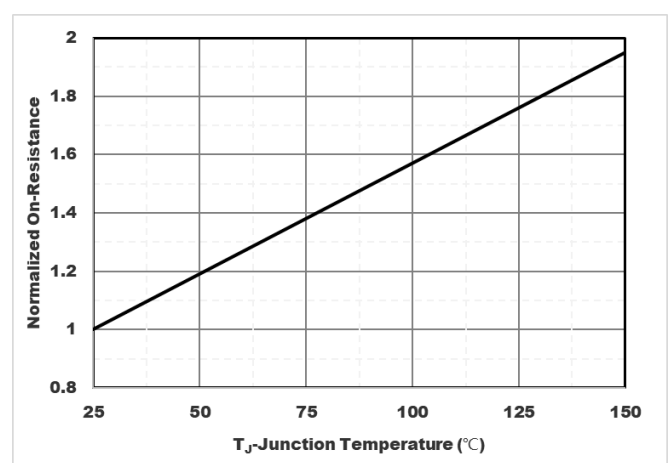


Figure6. Normalized On-Resistance



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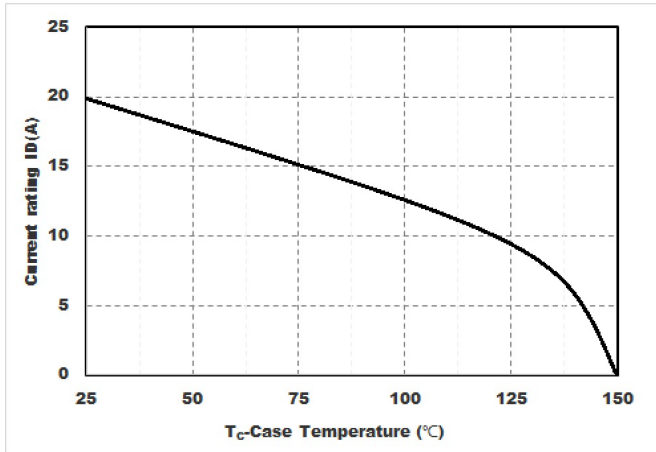


Figure7. Drain current

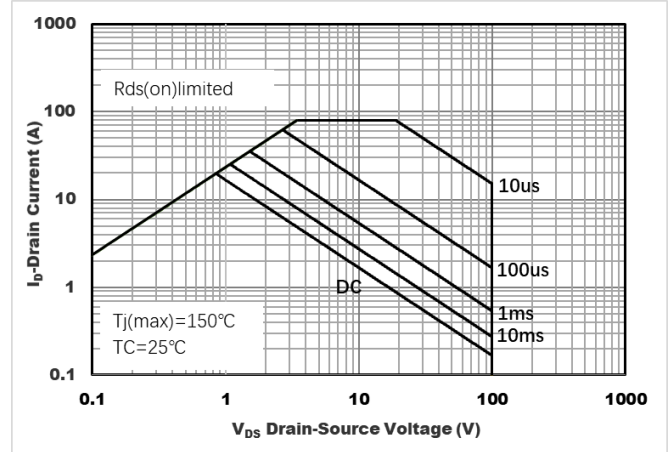


Figure8.Safe Operation Area

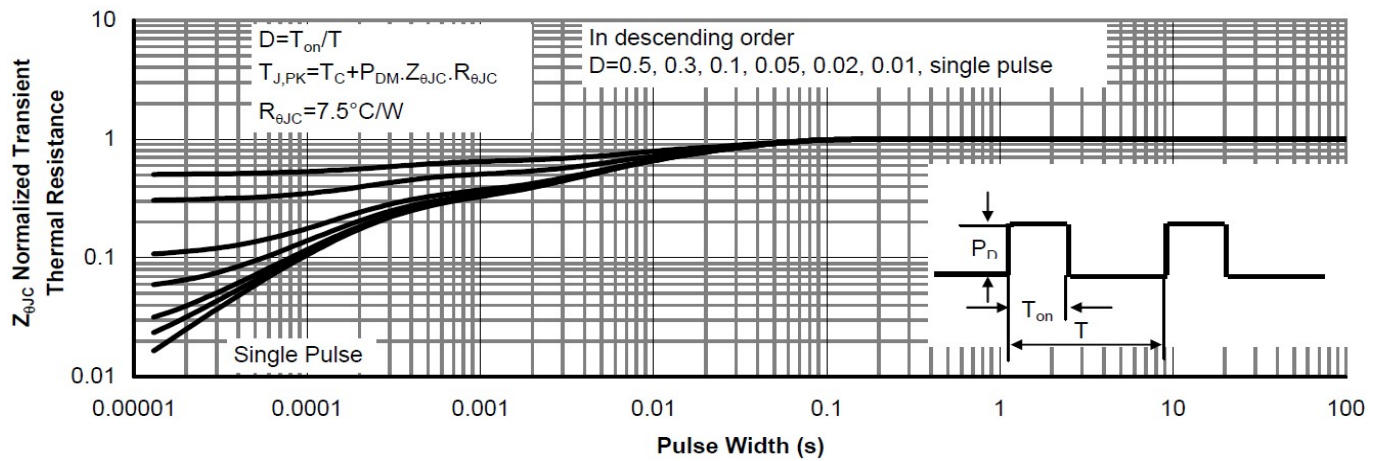
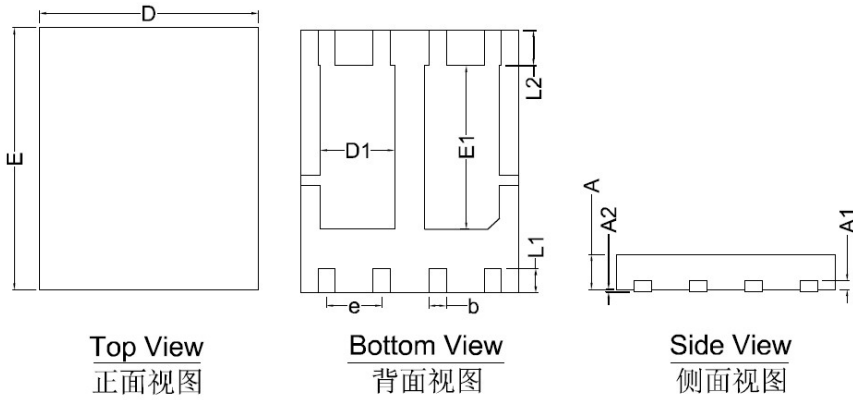


Figure9.Normalized Maximum Transient thermal impedance



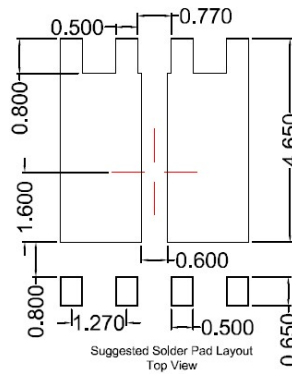
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■ DFN5060-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2	080 BSC		
b	0.30	0.40	0.50
e	1.27 BSC		

Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.





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