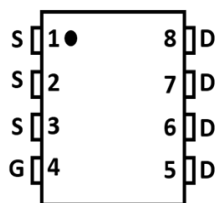
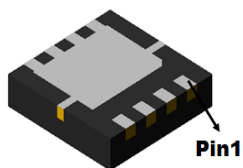
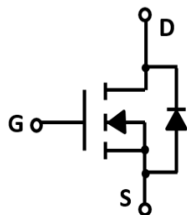


## N-Channel Enhancement Mode Field Effect Transistor



**DFN3.3X3.3**



### Product Summary

- $V_{DS}$  40 V
- $I_D$  35 A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $<8.0m\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $<13m\Omega$
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| Parameter                                  |                         | Symbol          | Limit           | Unit               |
|--------------------------------------------|-------------------------|-----------------|-----------------|--------------------|
| Drain-source Voltage                       |                         | $V_{DS}$        | 40              | V                  |
| Gate-source Voltage                        |                         | $V_{GS}$        | $\pm 20$        | V                  |
| Drain Current                              | $T_A=25^\circ\text{C}$  | $I_D$           | 35              | A                  |
|                                            | $T_A=100^\circ\text{C}$ |                 | 22              |                    |
| Pulsed Drain Current <sup>A</sup>          |                         | $I_{DM}$        | 160             | A                  |
| Single Pulse Avalanche Energy <sup>B</sup> |                         | $E_{AS}$        | 120             | mJ                 |
| Total Power Dissipation                    | $T_C=25^\circ\text{C}$  | $P_D$           | 40              | W                  |
|                                            | $T_A=25^\circ\text{C}$  |                 | 4.1             |                    |
| Thermal Resistance Junction-to-Case        |                         | $R_{\theta JC}$ | 3.1             | $^\circ\text{C/W}$ |
|                                            |                         | $R_{\theta JA}$ | 30              |                    |
| Junction and Storage Temperature Range     |                         | $T_J, T_{STG}$  | $-55 \sim +150$ | $^\circ\text{C}$   |

### ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|--------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| YJQ35N04A    | F1           | Q35N04  | 5000                 | 10000                   | 100000                     | 13" reel      |



# YJQ35N04A

## ■ Electrical Characteristics (T<sub>J</sub>=25℃ unless otherwise noted)

| Parameter                             | Symbol              | Conditions                                                                                                 | Min | Typ  | Max  | Units |
|---------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------|-----|------|------|-------|
| <b>Static Parameter</b>               |                     |                                                                                                            |     |      |      |       |
| Drain-Source Breakdown Voltage        | BV <sub>DSS</sub>   | V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA                                                                | 40  |      |      | V     |
| Zero Gate Voltage Drain Current       | I <sub>DSS</sub>    | V <sub>DS</sub> =40V, V <sub>GS</sub> =0V                                                                  |     |      | 1    | μA    |
| Gate-Body Leakage Current             | I <sub>GSS</sub>    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V                                                                |     |      | ±100 | nA    |
| Gate Threshold Voltage                | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA                                                  | 1.0 | 1.5  | 2.5  | V     |
| Static Drain-Source On-Resistance     | R <sub>DS(on)</sub> | V <sub>GS</sub> = 10V, I <sub>D</sub> =20A                                                                 |     | 6.5  | 8.0  | mΩ    |
|                                       |                     | V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A                                                                |     | 8.7  | 13   |       |
| Diode Forward Voltage                 | V <sub>SD</sub>     | I <sub>S</sub> =20A, V <sub>GS</sub> =0V                                                                   |     | 0.7  | 1.2  | V     |
| Maximum Body-Diode Continuous Current | I <sub>S</sub>      |                                                                                                            |     |      | 35   | A     |
| <b>Dynamic Parameters</b>             |                     |                                                                                                            |     |      |      |       |
| Input Capacitance                     | C <sub>iss</sub>    | V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHZ                                                          |     | 1860 |      | pF    |
| Output Capacitance                    | C <sub>oss</sub>    |                                                                                                            |     | 256  |      |       |
| Reverse Transfer Capacitance          | C <sub>rss</sub>    |                                                                                                            |     | 205  |      |       |
| Gate Resistance                       | R <sub>g</sub>      | f= 1MHZ                                                                                                    |     | 1.5  | 2    | Ω     |
| <b>Switching Parameters</b>           |                     |                                                                                                            |     |      |      |       |
| Total Gate Charge                     | Q <sub>g</sub>      | V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A                                            |     | 46.7 |      | nC    |
| Gate-Source Charge                    | Q <sub>gs</sub>     |                                                                                                            |     | 8    |      |       |
| Gate-Drain Charge                     | Q <sub>gd</sub>     |                                                                                                            |     | 11.6 |      |       |
| Reverse Recovery Charge               | Q <sub>rr</sub>     | I <sub>F</sub> =20A, di/dt=100A/us                                                                         |     | 2.3  |      | ns    |
| Reverse Recovery Time                 | t <sub>rr</sub>     |                                                                                                            |     | 15   |      |       |
| Turn-on Delay Time                    | t <sub>D(on)</sub>  | V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =2A, R <sub>L</sub> =1Ω<br>R <sub>GEN</sub> =3Ω |     | 10   |      |       |
| Turn-on Rise Time                     | t <sub>r</sub>      |                                                                                                            |     | 21   |      |       |
| Turn-off Delay Time                   | t <sub>D(off)</sub> |                                                                                                            |     | 36   |      |       |
| Turn-off fall Time                    | t <sub>f</sub>      |                                                                                                            |     | 25   |      |       |

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

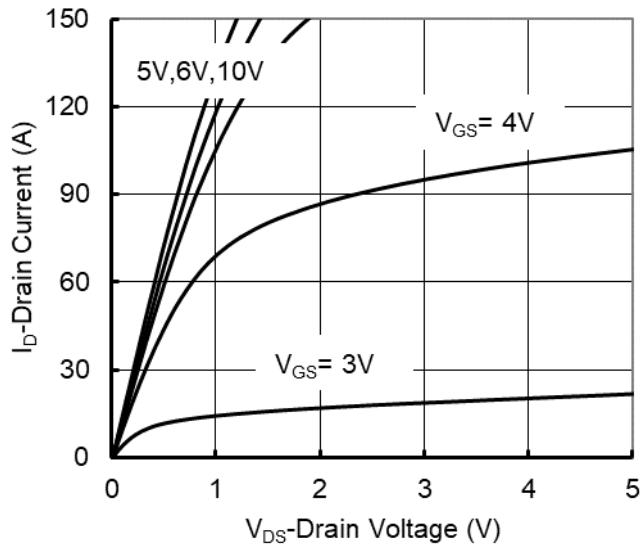


Figure 1. Output Characteristics

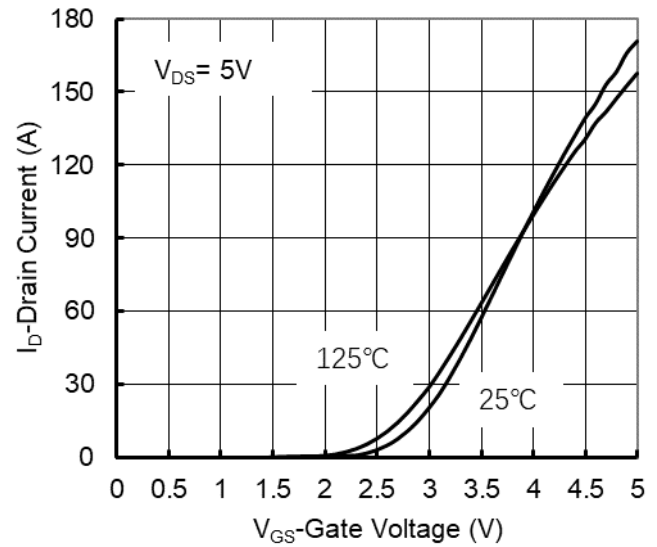


Figure 2. Transfer Characteristics

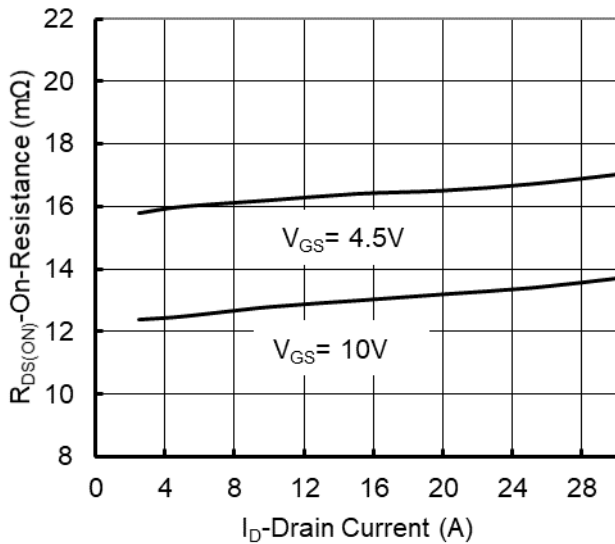


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

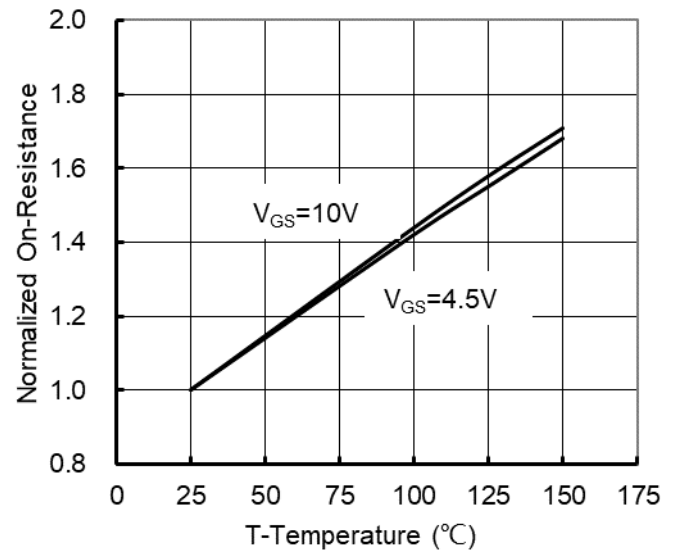


Figure 4. On-Resistance vs. Junction Temperature

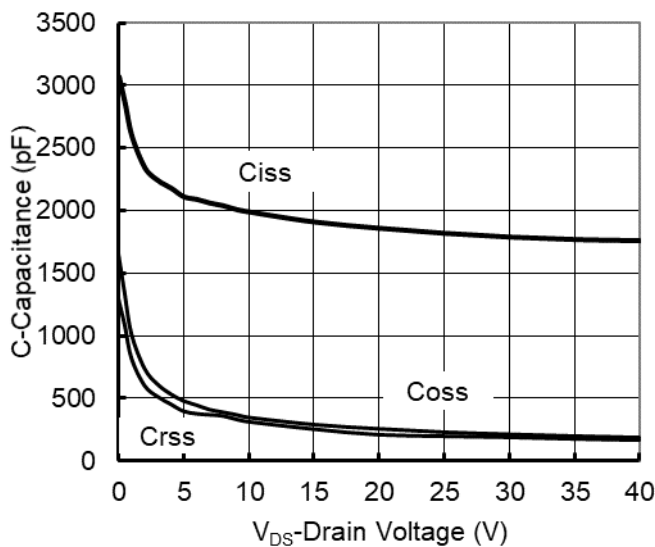


Figure 5. Capacitance Characteristics

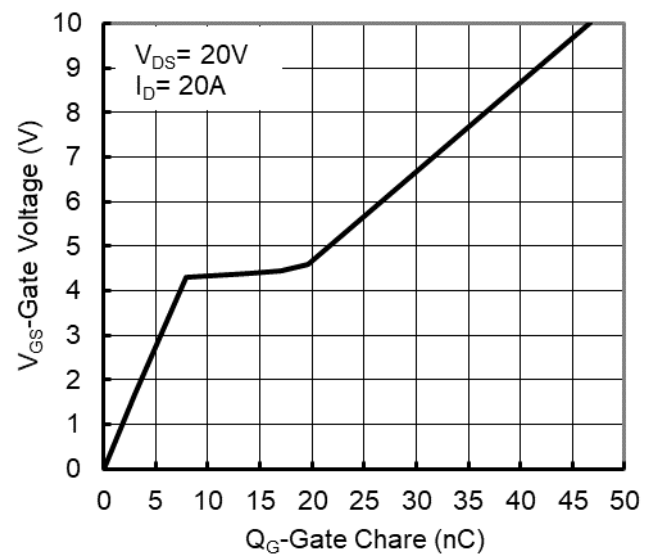


Figure 6. Gate Charge

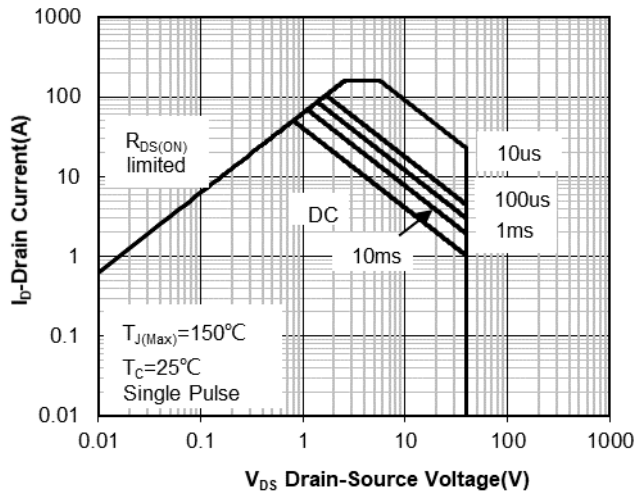


Figure 7. Safe Operation Area

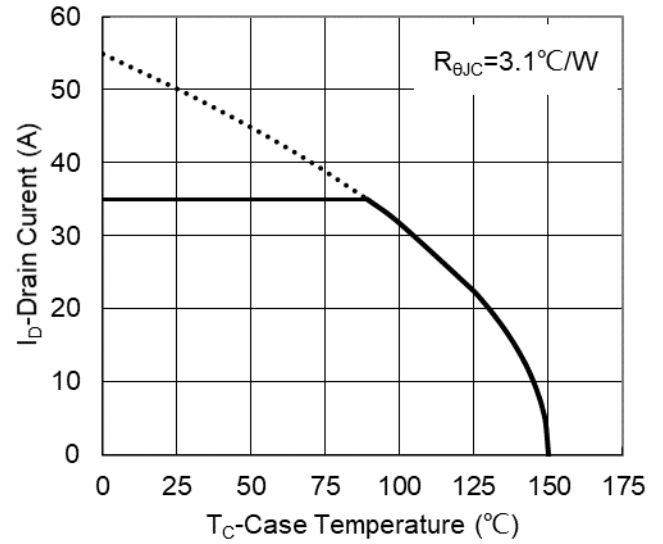


Figure 8. Maximum Continuous Drain Current vs. Ambient Temperature

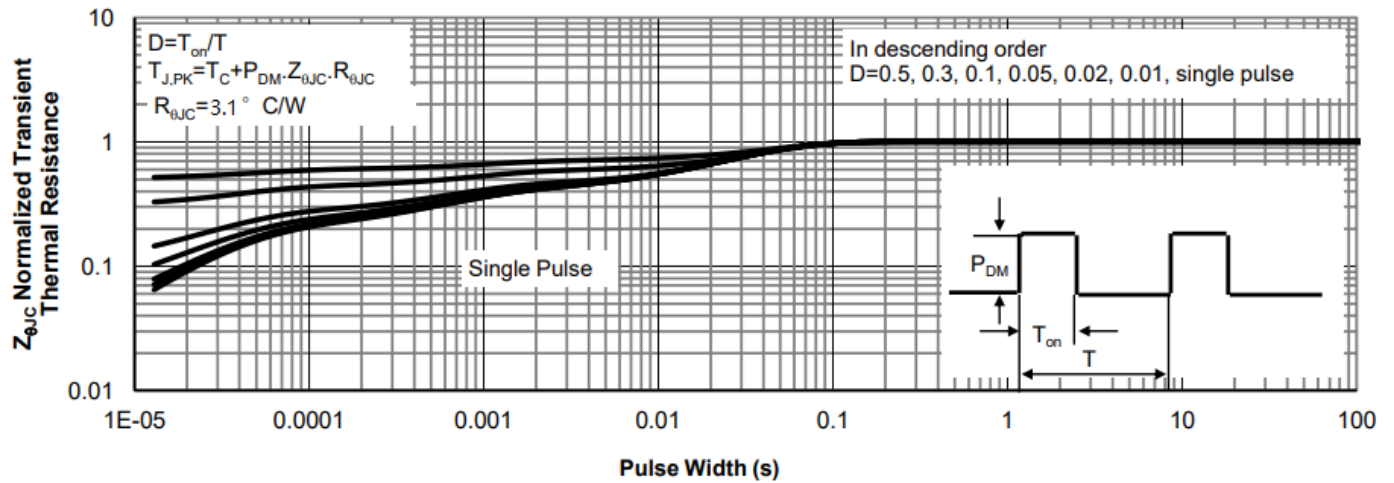
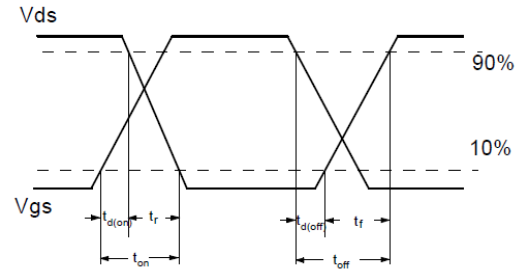
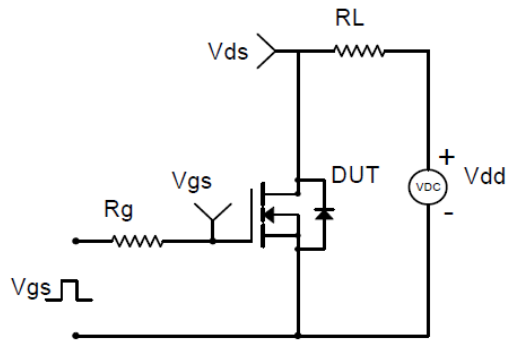
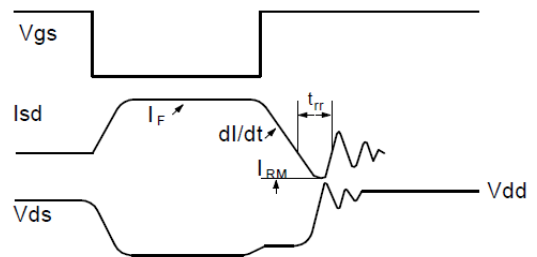
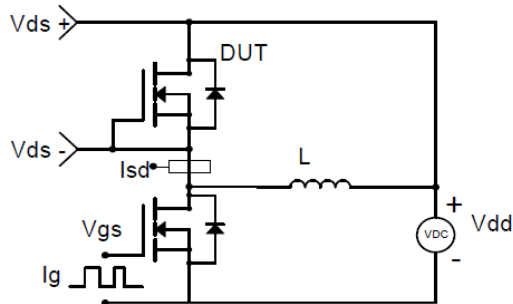


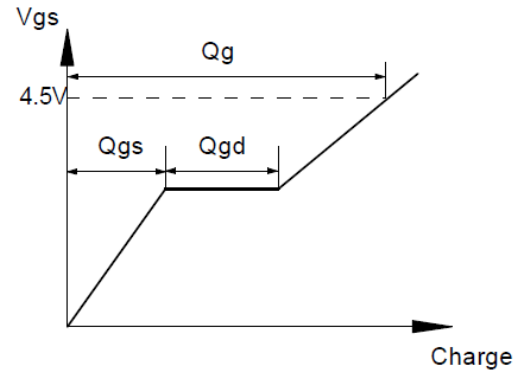
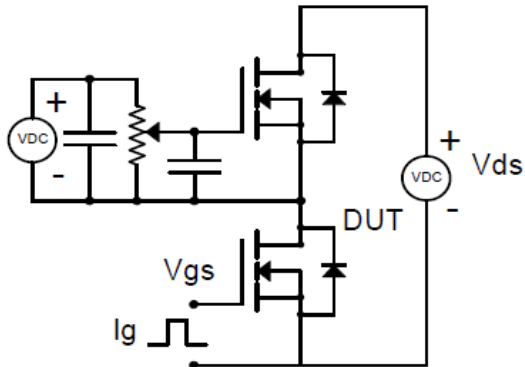
Figure 9. Normalized Maximum Transient Thermal Impedance



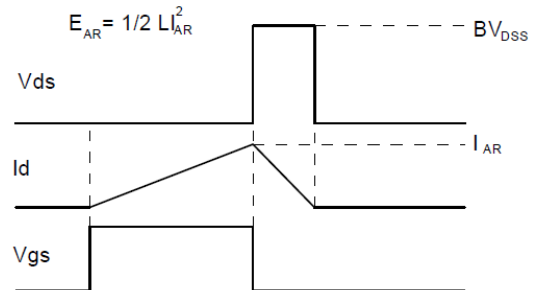
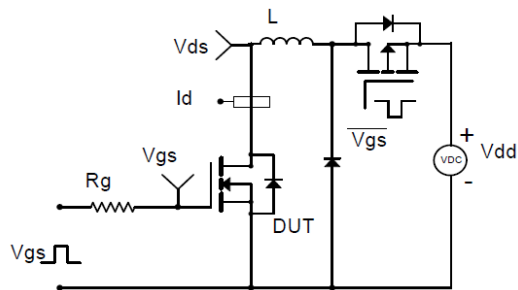
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



A diagram of a square. The top horizontal side is labeled with a dimension line and the letter  $D$ . The left vertical side is labeled with a dimension line and the letter  $W$ .

Technical drawing of a mechanical part with dimensions. The drawing shows a cross-section of a part with a central vertical axis. The dimensions are as follows:

- Overall width: 2.450
- Overall height: 2.000
- Top width: 0.650
- Top height: 0.350
- Bottom width: 0.400
- Bottom height: 0.450
- Central width: 0.000
- Central height: 0.000
- Left side height: 0.675
- Right side height: 0.550
- Left side width: 0.125
- Right side width: 0.400

Suggested Solder Pad Layout  
Top View

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