GENERAL DESCRIPTION

The XRT86VL30 is a single channel T1/E1/J1 BITS clock recovery element and framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL30 provides protection from power failures and hot swapping.

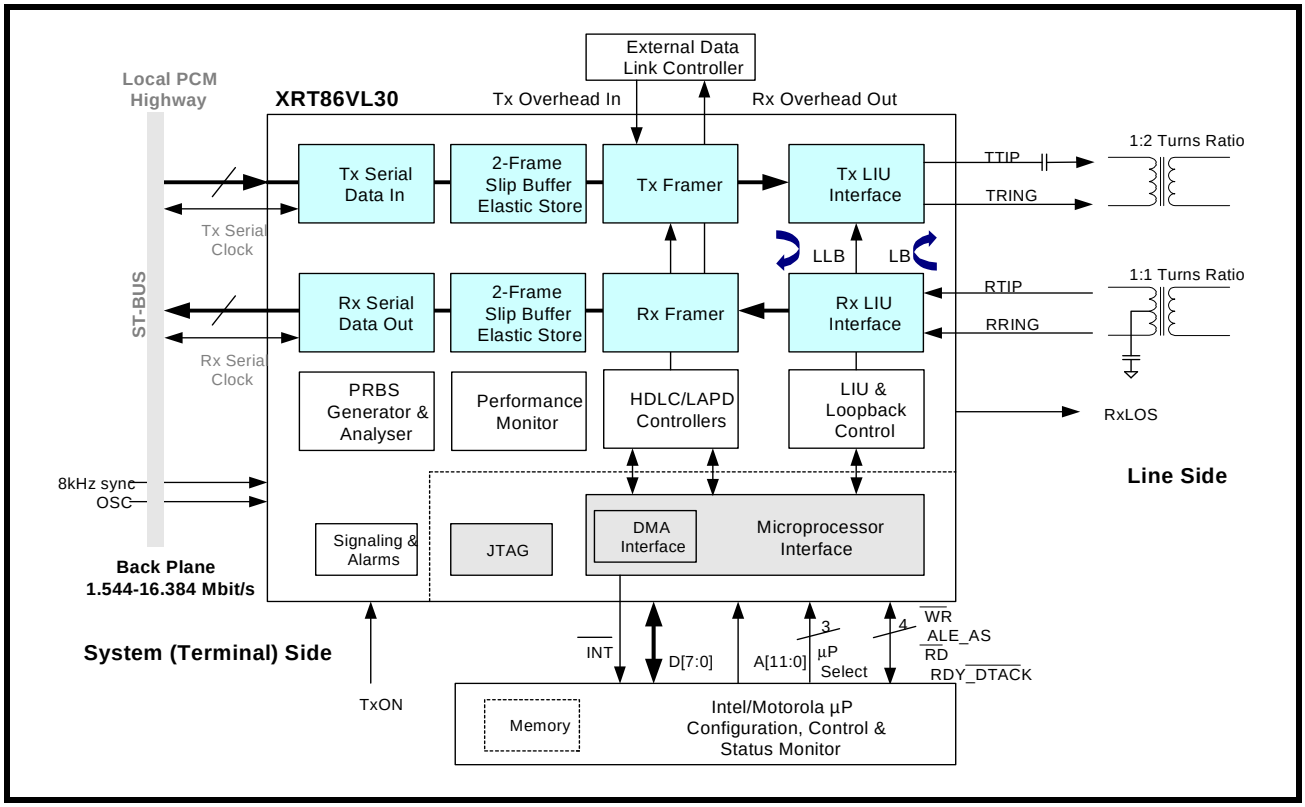
The XRT86VL30 contains an integrated DS1/E1/J1 framer and LIU which provides DS1/E1/J1 framing and error accumulation in accordance with ANSI/ ITU_T specifications. The framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

The Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. The framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL30 fully meets all of the latest T1/E1/J1 specifications: ANSI T1.101-1999, ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703 (Including Section 13 - Synchronization), G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

APPLICATIONS AND FEATURES (NEXT PAGE)

FIGURE 1. XRT86VL30 SINGLE CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- BITS Timing
- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Supports Section 13 - Synchronization Interface in ITU G.703 for both Transmit and Receive Paths
- Supports SSM Synchronous Messaging Generation (BOC for T1, National Bits for E1) on the Transmit Path
- Supports SSM Synchronous Messaging Extraction (BOC for T1, National Bits for E1) on the Receive Path
- Supports BITS timing generation on the Transmit Outputs
- Supports BITS timing extraction from NRZ data on the Analog Receive Path
- Parallel Microcontroller Interface
- Independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 2-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7

- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Supports SPRM and NPRM
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola or Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- Full BERT Controller for generation and detection on system and line side of the chip.
- PRBS, QRSS, and Network Loop Code generation and detection
- Three Independent, simultaneous Loop Code Detectors per Channel
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- The framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs
- 80-pin LQFP and 128-pin LQFP package options with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL30IV	128 Pin LQFP(14x20x1.4mm)	-40°C to +85°C
XRT86VL30IV80	80 Pin LQFP(12x12x1.4mm)	-40°C to +85°C

LIST OF FIGURES

LIST OF TABLES

1.0 128-PIN LIST

TABLE 1: 128-PIN LIST BY PIN NUMBER

PIN	PIN NAME
1	LOP
2	DVDD3v3
3	NC
4	DVDD1v8
5	DGND
6	TRING
7	TVDD3v3
8	TTIP
9	TGND
10	JTAG_RING
11	JTAG_TIP
12	RGND
13	RRING
14	RTIP
15	RVDD3v3
16	AVDD1v8
17	AGND
18	SENSE
19	ANALOG
20	VDDPLL1v8
21	VDDPLL1v8
22	PLLGND
23	PLLGND
24	MCLKIN
25	MCLKnOUT
26	RxOH
27	RxCHN4
28	RxCHN3
29	DGND
30	RxCASYNC
31	RxOHCLK
32	RxCHN2
33	RxSYNC
34	NC
35	NC
36	RxCH1
37	DVDD3v3
38	RxCHCLK
39	RxCRCSYNC
40	RxCHN0
41	DVDD1v8
42	RxSERCLK
43	RxLOS
44	RxSER
45	TxCHN4
46	TxCHN3
47	TxCHN2
48	DGND
49	TxCHCLK
50	TxCHN1
51	TxOH
52	DVDD3v3
53	TxCHN0
54	TxSERCLK
55	TxSER
56	DVDD1v8
57	TxOHCLK
58	TxMSYNC
59	TxSYNC
60	DGND
61	$\overline{\text{REQ1}}$
62	$\overline{\text{ACK0}}$
63	DVDD1v8
64	$\overline{\text{REQ0}}$
65	$\overline{\text{ACK1}}$
66	NC
67	NC
68	PCLK
69	DATA0
70	DATA1
71	$\overline{\text{RD}}$
72	DGND
73	$\overline{\text{DBEN}}$
74	$\overline{\text{RDY}}$
75	ADDR0
76	ADDR1
77	ADDR2
78	DVDD1v8
79	ADDR3
80	ADDR4
81	ADDR5
82	ADDR6
83	DGND
84	ADDR7
85	$\overline{\text{RESET}}$
86	OSCCLK
87	DGND
88	8KSYNC
89	ADDR8
90	DATA2
91	DATA3
92	DVDD3v3
93	ALE
94	ADDR9
95	ADDR10
96	$\overline{\text{INT}}$
97	ADDR11
98	NC
99	NC
100	BLAST
101	DATA4
102	DGND
103	DATA5
104	DATA6
105	DVDD1v8
106	DATA7
107	$\overline{\text{WR}}$
108	$\overline{\text{CS}}$
109	DGND
110	DGND
111	TCK
112	$\overline{\text{TRST}}$
113	TDI
114	TMS
115	TDO
116	GPIO1
117	GPIO0
118	GPIO2
119	GPIO3
120	aTEST
121	TEST
122	8KEXTOSC
123	fADDR
124	iADDR
125	PTYPE2
126	PTYPE1
127	PTYPE0
128	TxON

2.0 80-PIN LIST

TABLE 2: 80-PIN LIST BY PIN NUMBER

PIN	PIN NAME
1	DVDD1v8
2	DGND
3	TRING
4	TVDD3v3
5	TTIP
6	TGND
7	RGND
8	RRING
9	RTIP
10	RVDD3v3
11	AVDD1v8
12	AGND
13	VDDPLL1v8
14	VDDPLL1v8
15	PLLGND
16	PLLGND
17	MCLKIN
18	RxCHN4
19	RxCASYNC
20	RxSYNC
21	DVDD3v3
22	RxCRCSYNC
23	DVDD1v8
24	RxSERCLK
25	RxLOS
26	RxSER
27	DGND
28	DVDD3v3
29	TxSERCLK
30	TxSER
31	TxMSYNC
32	TxSYNC
33	DGND
34	$\overline{\text{REQ1}}$
35	$\overline{\text{ACK0}}$
36	DVDD1v8
37	$\overline{\text{REQ0}}$
38	$\overline{\text{ACK1}}$
39	PCLK
40	DATA0
41	DATA1
42	$\overline{\text{RD}}$
43	$\overline{\text{RDY}}$
44	ADDR0
45	ADDR1
46	ADDR2
47	ADDR3
48	ADDR4
49	ADDR5
50	ADDR6
51	ADDR7
52	$\overline{\text{RESET}}$
53	ADDR8
54	DATA2
55	DATA3
56	ALE
57	ADDR9
58	ADDR10
59	$\overline{\text{INT}}$
60	ADDR11
61	DATA4
62	DGND
63	DATA5
64	DATA6
65	DVDD1v8
66	DATA7
67	$\overline{\text{WR}}$
68	$\overline{\text{CS}}$
69	DGND
70	DGND
71	DGND
72	GPIO1
73	GPIO0
74	GPIO2
75	GPIO3
76	PTYPE2
77	PTYPE1
78	PTYPE0
79	TxON
80	DVDD3v3

3.0 PIN DESCRIPTIONS

There are six types of pins defined throughout this pin description and the corresponding symbol is presented in table below. All output pins are "tri-stated" upon hardware RESET.

TABLE 3: PIN TYPES

SYMBOL	PIN TYPE
I	Input
O	Output
I/O	Bidirectional
GND	Ground
PWR	Power
NC	No Connect

The structure of the pin description is divided into thirteen groups, as presented in the table below

TABLE 4: PIN DESCRIPTION STRUCTURE

SECTION	PAGE NUMBER
Transmit System Side Interface	page 7
Transmit Overhead Interface	page 15
Receive Overhead Interface	page 17
Receive System Side Interface	page 18
Receive Line Interface	page 26
Transmit Line Interface	page 27
Timing Interface	page 27
JTAG Interface	page 28
Microprocessor Interface	page 29
Power Pins (3.3V)	page 37
Power Pins (1.8V)	page 37
Ground Pins	page 37
No Connect Pins	page 37

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSER/ TxPOS	55	30	I	-	**Transmit Serial Data Input (TxSER)/Transmit Positive Digital Input (TxPOS):** The exact function of this pin depends on the mode of operation selected, as described below. **DS1/E1 Mode - TxSER** This pin functions as the transmit serial data input on the system side interface, which are latched on the rising edge of the TxSERCLk pin. Any payload data applied to this pin will be inserted into an outbound DS1/E1 frame and output to the line. In DS1 mode, the framing alignment bits, facility data link bits, CRC-6 bits, and signaling information can also be inserted from this input pin if configured appropriately. In E1 mode, all data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. Data intended for Time Slots 0 and 16 can also be applied to this input pin If configured accordingly. **DS1 or E1 High-Speed Multiplexed Mode* - TxSER** In this mode, this pin is used as the high-speed multiplexed data input pin on the system side. High-speed multiplexed data must be applied to TxSER in a byte or bit-interleaved way. The three unused channels are ignored for the single channel device. The framer latches in the multiplexed data on TxSER using TxMSYNC/TxINCLK and demultiplexes this data into 1 serial stream and 3 unused serial streams. The LIU block will then output the data to the line interface using TxSERCLK. **DS1 or E1 Framer Bypass Mode - TxPOS** In this mode, TxSER is used for the positive digital input pin (TxPOS) to the LIU. ***NOTE:*** *1. *High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* *2. In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* *3. This pin is internally pulled "High".*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSERCLK/ TxLINECLK	54	29	I/O	12	**Transmit Serial Clock (TxSERCLK)/Transmit Line Clock (TxSERCLK):** The exact function of this pin depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - TxSERCLK:** This clock signal is used by the transmit serial interface to latch the contents on the TxSER pin into the T1/E1 framer on the rising edge of TxSERCLK. This pin can be configured as input or output as described below. **When TxSERCLK is configured as Input:** This pin will be an input if the TxSERCLK is chosen as the timing source for the transmit framer. Users must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When TxSERCLK is configured as Output:** This pin will be an output if either the recovered line clock or the MCLK PLL is chosen as the timing source for the T1/E1 transmit framer. The transmit framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - TxSERCLK as INPUT ONLY** In this mode, TxSERCLK is an optional clock signal input which is used as the timing source for the transmit line interface, and is only required if TxSERCLK is chosen as the timing source for the transmit framer. If TxSERCLK is chosen as the timing source, system equipment should provide 1.544MHz (For T1 mode) or 2.048MHz (For E1 mode) to the TxSERCLK pin. TxSERCLK is not required if either the recovered clock or MCLK PLL is chosen as the timing source of the device. High speed or multiplexed data is latched into the device using the TxMSYNC/TxINCLK high-speed clock signal. **DS1 or E1 Framer Bypass Mode - TxLINECLK** In this mode, TxSERCLK is used as the transmit line clock (TxLINECLK) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *This pin is internally pulled "High".*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSYNC/ TxNEG	59	32	I/O	12	**Transmit Single Frame Sync Pulse (TxSYNC) / Transmit Negative Digital Input (TxNEG):** The exact function of this pin depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxSYNC:** These TxSYNC pin is used to indicate the single frame boundary within an outbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, TxSYNC can be configured as either input or output as described below. **When TxSYNC is configured as an Input**: Users must provide a signal which must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal. **When TxSYNC is configured as an Output:** The transmit T1/E1 framer will output a signal which pulses "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - TxSYNC as INPUT ONLY:** In this mode, TxSYNC must be an input regardless of the clock source that is chosen to be the timing source for the transmit framer. In 2.048MVIP/4.096/8.192MHz high-speed modes, the TxSYNC pin must be pulsed 'High' for one period of TxSERCLK during the first bit of the outbound T1/E1 frame. In HMVIP mode, TxSYNC0 must be pulsed 'High' for 4 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, TxSYNC0 must be pulsed 'High' for 2 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - TxNEGn** In this mode, TxSYNC is used as the negative digital input pin (TxNEG) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *This pin is internally pulled "Low".*

TRANSMIT SYSTEM SIDE INTERFACE

<table>
<tr><th>SIGNAL NAME</th><th>128-PIN#</th><th>80-PIN#</th><th>TYPE</th><th>OUTPUT DRIVE(MA)</th><th>DESCRIPTION</th></tr>
<tr><td>TxMSYNC/
TxINCLK</td><td>58</td><td>31</td><td>I/O</td><td>12</td><td>
Multiframe Sync Pulse (TxMSYNC) / Transmit Input Clock (TxINCLK)
The exact function of this pin depends on the mode of operation selected, as described below.
DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxMSYNC
In this mode, this pin is used to indicate the multi-frame boundary within an outbound DS1/E1 frame.
In DS1 ESF mode, TxMSYNC repeats every 3ms.
In DS1 SF mode, TxMSYNC repeats every 1.5ms.
In E1 mode, TxMSYNC repeats every 2ms.
If TxMSYNC is configured as an input, TxMSYNC must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 multi-frame. It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal.
If TxMSYNC is configured as an output, the transmit section of the T1/E1 framer will output and pulse TxMSYNC "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame.
DS1/E1 High-Speed Backplane Modes* - (TxINCLK as INPUT ONLY)
In this mode, TxINCLK0 must be used as the high-speed input clock pin for the backplane interface to latch in high-speed or multiplexed data on the TxSER pin. The frequency of TxINCLK0 is presented in the table below.
<table>
<tr><th>OPERATION MODE</th><th>FREQUENCY OF TXINCLK0(MHZ)</th></tr>
<tr><td>2.048MVIP non-multiplexed</td><td>2.048</td></tr>
<tr><td>4.096MHz non-multiplexed</td><td>4.096</td></tr>
<tr><td>8.192MHz non-multiplexed</td><td>8.192</td></tr>
<tr><td>12.352MHz Bit-multiplexed (DS1 ONLY)</td><td>12.352</td></tr>
<tr><td>16.384MHz Bit-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 HMVIP Byte-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 H.100 Byte-multiplexed</td><td>16.384</td></tr>
</table>
NOTES:
1. *High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.
2. In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).
3. This pin is internally pulled "Low".
</td></tr>
</table>

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHCLK	49	n/a	O	8	**Transmit Channel Clock Output Signal (TxCHCLK):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface to input fractional data, as described below. **If transmit fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. In T1 mode, this output pin is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, this output pin is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. The Terminal Equipment can use this clock signal to sample the TxCHN0 through TxCHN4 time slot identifier pins to determine which time slot is being processed. **If transmit fractional/signaling interface is enabled:** TxCHCLK is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to input fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked into the device using the TxSERCLK pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0x0120 to '1'.* *This pin is internally pulled "Low"*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0/ TxSIG	53	n/a	I/O	8	**Transmit Time Slot Octet Identifier Output 0 (TxCHN0) / Transmit Serial Signaling Input (TxSIG):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHN0:** These output pins (TxCHN4 through TxCHN0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of in order to identify the time slot being processed. This pin indicates the Least Significant Bit (LSB) of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxSIG:** This pin can be used to input robbed-bit signaling data to be inserted within an outbound DS1 frame or to input Channel Associated Signaling (CAS) data within an outbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) must be provided on bit 4,5,6,7 of each time slot on the TxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) must be provided on bit 4, 5 of each time slot on the TxSIG pin. If 2-code signaling is selected, signaling data (A) must be provided on bit 4 of each time slot on the TxSIG pin. **E1 Mode:** Signaling data in E1 mode can be provided on the TxSIG pin on a time-slot-basis as in T1 mode, or it can be provided on time slot 16 only via the TxSIG input pin. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxSIG pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxSIG pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxSIG pin during time slot 16 of frame 0. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0x0120 to '1'.* ***NOTE:*** *This pin is internally pulled "Low".*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN1/ TxFrTD	50	n/a	I/O	8	**Transmit Time Slot Octet Identifier Output 1 (TxCHN1) / Transmit Serial Fractional Input (TxFrTD):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHN1** These output signals (TxCHN4 through TxCHN0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins in order to identify the time slot being processed. This pin indicates Bit 1 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxFrTDn** This pin is used as the fractional data input pin to input fractional DS1/E1 payload data which will be inserted within an outbound DS1/E1 frame. In this mode, terminal equipment can use either TxCHCLK or TxSERCLK to clock in fractional DS1/E1 payload data depending on the framer configuration. ***NOTES:*** *1. Transmit fractional/Signaling interface can be enabled by programming to bit 4 - TxFr1544/ TxFr2048 bit from register 0x0120 to '1'.* *2. This pin is internally pulled "Low".*
TxCHN2/ Tx32MHz	47	n/a	O	8	**Transmit Time Slot Octet Identifier Output 2 (TxCHN2) / Transmit 32.678MHz Clock Output (Tx32MHZ):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHN2** These output signals (TxCHN4 through TxCHN0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins in order to identify the time slot being processed. This pin indicates Bit 2 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - Tx32MHz** This pin is used to output a 32.678MHz clock reference which is derived from the MCLKIN input pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0x0120 to '1'.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN3/ TxOHSYNC	46	n/a	O	8	**Transmit Time Slot Octet Identifier Output 3 (TxCHN3) / Transmit Overhead Synchronization Pulse (TxOHSYNC):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHN3** These output signals (TxCHN4 through TxCHN0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins in order to identify the time slot being processed. This pin indicates Bit 3 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxOHSYNC** This pin is used to output an Overhead Synchronization Pulse which indicates the first bit of each multi-frame. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0x0120 to '1'.*
TxCHN4	45	n/a	O	8	**Transmit Time Slot Octet Identifier Output-Bit 4 (TxCHN4):** These output signals (TxCHN4 through TxCHN0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins in order to identify the time slot being processed. This pin indicates the Most Significant Bit (MSB) of the time slot channel being processed.

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxOH	51	n/a	I	-	**Transmit Overhead Input (TxOH):** The exact function of this pin depends on the mode of operation selected, as described below. **DS1 Mode** This pin operate as the source of Datalink bits which will be inserted into the Datalink bits within an outbound DS1 frame if the framer is configured accordingly. Datalink Equipment can provide data to this input pin using the TxOHCLK clock at either 2kHz or 4kHz depending on the transmit datalink bandwidth selected. ***NOTE:*** *This input pin will be disabled if the framer is using the Transmit HDLC Controller, or the TxSER input as the source for the Data Link Bits.* **E1 Mode** This pin operates as the source of Datalink bits or Signaling bits depending on the framer configuration, as described below. **Sourcing Datalink bits from TxOH:** The E1 transmit framer will output a clock edge on TxOHCLK for each Sa bit that has been configured to carry datalink information. Terminal equipment can then use TxOHCLK to provide datalink bits on TxOH to be inserted into the Sa bits within an outbound E1 frame. **Sourcing Signaling bits from TxOH:** Users must provide signaling data on the TxOH pin on time slot 16 only. Signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxOH pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxOH pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxOH pin during time slot 16 of frame 0. ***NOTE:*** *This pin is internally pulled "Low".*

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxOHCLK	57	n/a	O	8	**Transmit OH Serial Clock Output Signal(TxOHCLK)** This pin functions as an overhead output clock signal for the transmit overhead interface, and its function is explained below. **DS1 Mode** If the TxOH pin has been configured to be the source for Datalink bits, the DS1 transmit framer will provide a clock edge for each Data Link Bit. In DS1 ESF mode, the TxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0x010A). Data Link Equipment can provide data to the TxOH pin on the rising edge of TxOHCLK. The framer latches the data on the falling edge of this clock signal. **E1 Mode** If the TxOH pin has been configured to be the source for Data Link bits, the E1 transmit framer will provide a clock edge for each National Bit (Sa bits) that has been configured to carry data link information. (Register 0x010A)

RECEIVE OVERHEAD INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
RxOH	26	n/a	O	8	**Receive Overhead Output (RxOH):** This pin functions as the Receive Overhead output, or Receive Signaling Output depending on the receive framer configuration, as described below. **DS1 Mode** If the RxOH pin has been configured as the destination for the Data Link bits within an inbound DS1 frame, datalink bits will be output to the RxOH pin at either 2kHz or 4kHz depending on the Receive datalink bandwidth selected. (Register 0x010C). If configured appropriately, signaling information in the receive signaling array registers (Registers 0x0500-0x051F) can also be output to the RxOH output pin. **E1 Mode** This output pin will always output the contents of the National Bits (Sa4 through Sa8) if these Sa bits have been configured to carry Data Link information (Register 0x010C). The Receive Overhead Output Interface will provide a clock edge on RxOHCLK for each Sa bit carrying Data Link information. If configured appropriately, signaling information in the receive signaling array registers (Registers 0x0500-0x051F) can also be output to the RxOH output pin.
RxOHCLK	31	n/a	O	8	**Receive Overhead Clock Output (RxOHCLK):** This pin functions as an overhead output clock signal for the receive overhead interface, and its function is explained below. **DS1 Mode** If the RxOH pin has been configured to be the destination for Datalink bits, the DS1 transmit framer will output a clock edge for each Data Link Bit. In DS1 ESF mode, the RxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0x010C). Data Link Equipment can clock out datalink bits on the RxOH pin using this clock signal. **E1 Mode** The E1 receive framer provides a clock edge for each National Bit (Sa bits) that is configured to carry data link information. Data Link Equipment can clock out datalink bits on the RxOH pin using this clock signal.

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSYNC/ RxNEG	33	20	I/O	12	**Receive Single Frame Sync Pulse (RxSYNC):** The exact function of this pin depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - RxSYNC:** This RxSYNC pin is used to indicate the single frame boundary within an inbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, RxSYNC can be configured as either input or output depending on the slip buffer configuration as described below. **When RxSYNC is configured as an Input**: Users must provide a signal which must pulse "High" for one period of RxSERCLK and repeats every 125µS. The receive serial Interface will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with the RxSERCLK input signal.* **When RxSYNC is configured as an Output:** The receive T1/E1 framer will output a signal which pulses "High" for one period of RxSERCLK during the first bit of an inbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - RxSYNC as INPUT ONLY:** In this mode, RxSYNC must be an input regardless of the slip buffer configuration. In 2.048MVIP/4.096/8.192MHz high-speed modes, the RxSYNC pin must be pulsed 'High' for one period of RxSERCLK during the first bit of the inbound T1/E1 frame. In HMVIP mode, RxSYNC0 must be pulsed 'High' for 4 clock cycles of the RxSERCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, RxSYNC0 must be pulsed 'High' for 2 clock cycles of the RxSERCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - RxNEGn** In this mode, RxSYNC is used as the Receive negative digital output pin (RxNEG) from the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *This pin is internally pulled "Low".*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCRCSYNC	39	22	O	12	**Receive Multiframe Sync Pulse (RxCRCSYNC):** The RxCRCSYNC pin is used to indicate the receive multi-frame boundary. This pin pulse "High" for one period of RxSERCLK when the first bit of an inbound DS1/E1 Multi-frame is being output on the RxCRCSYNC pin. • In DS1 ESF mode, RxCRCSYNC repeats every 3ms • In DS1 SF mode, RxCRCSYNC repeats every 1.5ms • In E1 mode, RxCRCSYNC repeats every 2ms.
RxCASYNC	30	19	O	12	**Receive CAS Multiframe Sync Pulse (RxCASYNC):** **- E1 Mode Only** The RxCASYNC pin is used to indicate the E1 CAS Multif-frame boundary. This pin pulses "High" for one period of RxSERCLK when the first bit of an E1 CAS Multi-frame is being output on the RxCASYNC pin.

RECEIVE SYSTEM SIDE INTERFACE

<table>
<tr><th>SIGNAL NAME</th><th>128-PIN#</th><th>80-PIN#</th><th>TYPE</th><th>OUTPUT DRIVE (MA)</th><th>DESCRIPTION</th></tr>
<tr><td>RxSERCLK/
RxLINECLK</td><td>42</td><td>24</td><td>I/O</td><td>12</td><td>
Receive Serial Clock Signal (RxSERCLK) / Receive Line Clock (RxLINECLK):
The exact function of this pin depends on the mode of operation selected, as described below.
In Base-Rate Mode (1.544MHz/2.048MHz) - RxSERCLK:
This pin is used as the receive serial clock on the system side interface which can be configured as either input or output. The receive serial interface outputs data on RxSER on the rising edge of RxSERCLK.
When RxSERCLK is configured as Input:
This pin will be an input if the slip buffer on the Receive path is enabled. System side equipment must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode.
When RxSERCLK is configured as Output:
This pin will be an output if slip buffer is bypassed. The receive framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode.
DS1/E1 High-Speed Backplane Modes* - (RxSERCLK as INPUT ONLY)
In this mode, this pin must be used as the high-speed input clock for the backplane interface to output high-speed or multiplexed data on the RxSER pin. The frequency of RxSERCLK is presented in the table below.
<table>
<tr><th>OPERATION MODE</th><th>FREQUENCY OF RXSERCLK(MHZ)</th></tr>
<tr><td>2.048MVIP non-multiplexed</td><td>2.048</td></tr>
<tr><td>4.096MHz non-multiplexed</td><td>4.096</td></tr>
<tr><td>8.192MHz non-multiplexed</td><td>8.192</td></tr>
<tr><td>12.352MHz Bit-multiplexed (DS1 ONLY)</td><td>12.352</td></tr>
<tr><td>16.384MHz Bit-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 HMVIP Byte-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 H.100 Byte-multiplexed</td><td>16.384</td></tr>
</table>
NOTES:
1. *High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.
2. For DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).
</td></tr>
</table>

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK/ RxLINECLK	42	24	I/O	12	**(Continued)** **DS1 or E1 Framer Bypass Mode - RxLINECLK** In this mode, RxSERCLK is used as the Receive Line Clock output pin (RxLineClk) from the LIU. ***NOTE:*** *This pin is internally pulled "High".*
RxSER/ RxPOS	44	26	O	12	**Receive Serial Data Output (RxSER):** The exact function of this pin depends on the mode of operation selected, as described below. **DS1/E1 Mode - RxSER** This pin functions as the receive serial data output on the system side interface, which updates on the rising edge of the RxSERCLK pin. All the framing alignment bits, facility data link bits, CRC bits, and signaling information will also be extracted to this output pin. **DS1 or E1 High-Speed Multiplexed Mode* - RxSER** In this mode, this pin is used as the high-speed multiplexed data output pin on the system side. High-speed multiplexed data will output on RxSER in a byte or bit-interleaved way. The framer outputs the multiplexed data on RxSER using the high-speed input clock (RxSERCLK). **DS1 or E1 Framer Bypass Mode** In this mode, RxSER is used as the positive digital output pin (RxPOS) from the LIU. ***NOTE:*** **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN0/ RxSig	40	n/a	O	8	**Receive Time Slot Octet Identifier Output (RxCHN0) / Receive Serial Signaling Output (RxSIG):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHN0:** These output pins (RxCHN4 through RxCHN0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLK to sample the five output pins to identify the time slot being output on this pin. RxCHN0 indicates the Least Significant Bit (LSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxSIG:** This pin can be used to output robbed-bit signaling data within an inbound DS1 frame or to output Channel Associated Signaling (CAS) data within an inbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) will be output on bit 4,5,6,7 of each time slot on the RxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) will be output on bit 4, 5 of each time slot on the RxSIG pin. If 2-code signaling is selected, signaling data (A) will be output on bit 4 of each time slot on the RxSIG pin. **E1 Mode:** Signaling data in E1 mode will be output on the RxSIG pin on a time-slot-basis as in T1 mode, or it can be output on time slot 16 only via the RxSIG output pin. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 will be output on the RxSIG pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 will be output on the RxSIG pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) will be output on the RxSIG pin during time slot 16 of frame 0. ***NOTE:*** *Receive Fractional/signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN1/ RxFrTD	36	n/a	O	8	**Receive Time Slot Octet Identifier Output Bit 1 (RxCHN1) / Receive Serial Fractional Output (RxFrTD):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHN1:** These output pins (RxCHN4 through RxCHN0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLK to sample the five output pins to identify the time slot being output on this pin. RxCHN1 indicates Bit 1 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxFrTD:** This pin is used as the fractional data output pin to output fractional DS1/E1 payload data within an inbound DS1/E1 frame. In this mode, system equipment can use either RxCHCLK or RxSERCLK to clock out fractional DS1/E1 payload data depending on the framer configuration. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*
RxCHN2/ RxCHN	32	n/a	O	8	**Receive Time Slot Octet Identifier Output-Bit 2 (RxCHN2) / Receive Time Slot Identifier Serial Output (RxCHN):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHN2:** These output pins (RxCHN4 through RxCHN0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLK to sample the five output pin to identify the time slot being output on this pin. RxCHN2 indicates Bit 2 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxCHNn** This pin serially outputs the five-bit binary value of the time slot being output by the receive serial interface. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN3/ Rx8KHZ	28	n/a	O	8	**Receive Time Slot Octet Identifier Output-Bit 3 (RxCHN3) / Receive 8KHz Clock Output (Rx8KHZ):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHN3:** These output pins (RxCHN4 through RxCHN0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLK to sample the five output pin to identify the time slot being output on this pin. RxCHN3 indicates Bit 3 of the time slot channel being output. **If receive fractional/signaling interface is enabled - Rx8KHZ:** This pin outputs a reference 8KHz clock signal derived from the MCLKIN input. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*
RxCHN4/ RxSCLK	27	18	O	8	**Receive Time Slot Octet Identifier Output-Bit 4 (RxCHN4) / Receive Recovered Line Clock Output (RxSCLK):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHN4:** These output pins (RxCHN4 through RxCHN0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLK to sample the five output pin to identify the time slot being output on this pin. RxCHN4 indicates the Most Significant Bit (MSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - Receive Recovered Line Clock Output (RxSCLK):** This pin outputs the recovered T1/E1 line clock (1.544MHz in T1 mode and 2.048MHz in E1 mode). ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHCLK	38	n/a	O	8	**Receive Channel Clock Output (RxCHCLK):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface to output fractional data, as described below. **If receive fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an inbound DS1/E1 frame. In T1 mode, this output pin is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, this output pin is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. System Equipment can use this clock signal to sample the RxCHN0 through RxCHN4 time slot identifier pins to determine which time slot is being output. **If receive fractional/signaling interface is enabled:** RxCHCLK is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to output fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked out of the device using the RxSERCLK pin. ***NOTE:*** *Receive fractional interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0x0122 to '1'.*

RECEIVE LINE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RTIP	14	9	I	-	**Receive Positive Analog Input (RTIP):** RTIP is the positive differential input from the line interface. This input pin, along with the RRING input pin, functions as the “Receive DS1/E1 Line Signal” input for the XRT86VL30 device. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RRING	13	8	I	-	**Receive Negative Analog Input (RRING):** RRING is the negative differential input from the line interface. This input pin, along with the RTIP input pin, functions as the “Receive DS1/E1 Line Signal” input for the XRT86VL30 device. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RxLOS	43	25	O	4	**Receive Loss of Signal Output Indicator (RLOS):** The XRT86VL30 device will assert this output pin (i.e., toggle it “high”) anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block declares the LOS defect condition. Conversely, the XRT86VL30 device will tri-state this output pin anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block is NOT declaring the LOS defect condition. ***NOTES:***. 1. *This output pin will toggle "high" (to denote that LOS is being declared) whenever either the Receive DS1/E1 Framer or the Receive DS1/E1 LIU block declares the LOS defect condition. In other words, the state of this output pin is a logic OR of the Framer LOS and the LIU LOS condition.* 2. *Since the XRT86VL30 device tri-states this output pin (anytime the channel is NOT declaring the LOS defect condition). Therefore, the user MUST connect a "pull-down" resistor (ranging from 1K to 10K) to the RxLOS output pin, in order to pull this output pin to the logic "LOW" condition, whenever the Channel is NOT declaring the LOS defect condition.*

TRANSMIT LINE INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
TTIP	8	5	O	**Transmit Positive Analog Output (TTIP):** TTIP is the positive differential output to the line interface. This output pin, along with the corresponding TRING output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL30 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. This output pin will be tri-stated whenever the user sets the "TxON" input pin or register bit (0x0F02, bit 3) to "0". ***NOTE:*** *This pin should have a series line capacitor of 0.68μF for DC blocking purposes.*
TRING	6	3	O	**Transmit Negative Analog Output (TRING):** TRING is the negative differential output to the line interface. This output pin, along with the corresponding TTIP output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL30 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the "TxON" input pin or register bit (0x0F02, bit 3) to "0".*
TxON	128	79	I	**Transmitter On** This input pin permits the user to either enable or disable the Transmit Output Driver within the Transmit DS1/E1 LIU Block. If the TxON pin is pulled "Low", the output driver is tri-stated. When this pin is pulled 'High', turning on or off the transmitter will be determined by the appropriate channel register (address 0x0F02, bit 3) **LOW** = Disables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the TTIP and TRING output pins will be tri-stated. **HIGH** = Enables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the corresponding TTIP and TRING output pins will be enabled or disabled by programming the appropriate channel register. (address 0x0F02, bit 3) ***NOTE:*** *Whenever the transmitters are turned off, the TTIP and TRING output pins will be tri-stated.*

TIMING INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
MCLKIN	24	17	I	**Master Clock Input:** This pin is used to provide the timing reference for the internal master clock of the device. The frequency of this clock is programmable from 1.544Mhz to 16.384MHz in register 0x0FE9. ***NOTE:*** *For HMVIP mode, this pin should be set to 1.544MHz or 2.048MHz.*
MCLKnOUT	25	n/a	O	**LIU T1/E1 Output Clock Reference** This output clock depends on the mode of operation. In T1 mode, this output pin is defaulted to 1.544MHz, but can be programmed to output 3.088MHz, 6.176MHz, or 12.352MHz in register 0x0FE4. In E1 mode, this output pin is defaulted to 2.048MHz, but can be programmed to 4.096MHz, 8.192MHz, or 16.384MHz in register 0x0FE4.

TIMING INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
OSCCLK	86	n/a	I/O	**Framer T1/E1 Output Clock Reference** This output clock depends on the mode of operation. In T1 mode, this output pin is defaulted to 1.544MHz, but can be programmed to output 49.408MHz in register 0x011E. In E1 mode, this output pin is defaulted to 2.048MHz, but can be programmed to 65.536MHz in register 0x011E. ***NOTE:*** *This pin is internally pulled "Low"*
8KSYNC	88	n/a	I/O	**8kHz Clock Output Reference** This pin is an output reference of 8kHz based on the MCLKIN input. Therefore, the duty cycle of this output is determined by the time period of the input clock reference. ***NOTE:*** *This pin is internally pulled "Low"*
8KEXTOSC	122	n/a	I	**External Oscillator Select** For normal operation, this pin should not be used, or pulled "Low". ***NOTE:*** *This pin is internally pulled "Low"*
ANALOG	19	n/a	O	Factory Test Mode Pin **Note:** For Internal Use Only
LOP	1	n/a	I	**Loss of Power for E1 Only** This is a Loss of Power pin in the E1 application only. Upon detecting LOP in E1 mode, the device will automatically transmit the Sa5 and Sa6 bit to a different pattern, so that the Receive terminal can detect a power failure in the network. Please see register 0x0131 for the Transmit SA control.

GPIO CONTROL

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
GPIO_3 GPIO_2 GPIO_1 GPIO_0	119 118 116 117	75 74 72 73	I/O	**General Purpose Input/Output Pins** The GPIO pins can be used as either inputs or outputs selected by register 0x0102. By default, these pins are inputs. To configure a GPIO pin to be an output, the register bit must be set to "1".

JTAG

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
TCK	111	n/a	I	**Test clock: Boundary Scan Test clock input:** The TCLK signal is the clock for the TAP controller, and it generates the boundary scan data register clocking. The data on TMS and TDI is loaded on the positive edge of TCK. Data is observed at TDO on the falling edge of TCK.
TMS	114	n/a	I	**Test Mode Select:** Boundary Scan Test Mode Select input. The TMS signal controls the transitions of the TAP controller in conjunction with the rising edge of the test clock (TCK). ***NOTE:*** *1. For normal operation this pin MUST be pulled "High".* *2. This pin is internally pulled 'high'*

JTAG

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
TDI	113	n/a	I	**Test Data In:** Boundary Scan Test data input The TDI signal is the serial test data input. ***NOTE:*** *This pin is internally pulled 'high'.*
TDO	115	n/a	O	**Test Data Out:** Boundary Scan Test data output The TDO signal is the serial test data output.
$\overline{\text{TRST}}$	112	n/a	I	**Test Reset Input:** The $\overline{\text{TRST}}$ signal (Active Low) asynchronously resets the TAP controller to the Test-Logic-Reset state. ***NOTE:*** *1. This pin is internally pulled 'high'*
TEST	121	n/a	I	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
aTEST	120	n/a	I	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
SENSE	18	n/a	I	Factory Test Mode Pin Note: User should tie this pin to ground
JTAG_Ring	10	n/a	I	**ATP_Ring Test Pin** This analog test pin is used for testing the continuity between the TTIP/ TRING, RTIP/RRING and the on-board transformer.
JTAG_Tip	11	n/a	I	**ATP_Tip Test Pin** This analog test pin is used for testing the continuity between the TTIP/ TRING, RTIP/RRING and the on-board transformer.

MICROPROCESSOR INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
DATA0	69	40	I/O	**Bidirectional Microprocessor Data Bus** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT86VL30 device. When DMA interface is enabled, these 8-bit bidirectional data bus is also used by the T1/E1 Framer or the external DMA Controller for storing and retrieving information.
DATA1	70	41		
DATA2	90	54		
DATA3	91	55		
DATA4	101	61		
DATA5	103	63		
DATA6	104	64		
DATA7	106	66		

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
$\overline{\text{REQ0}}$	64	37	O	**DMA Cycle Request Output—DMA Controller 0 (Write)**: This output pin is used to indicate that DMA transfers (Write) are requested by the T1/E1 Framer. On the transmit side (i.e., To transmit data from external DMA controller to HDLC buffers within the XRT86VL30), DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA Write cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ0}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK0}}$) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the $\overline{\text{WR}}$ is configured as a Write Strobe. If $\overline{\text{WR}}$ is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal ($\overline{\text{RD}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it "High") when the HDLC buffer can no longer receive another HDLC message.
$\overline{\text{REQ1}}$	61	34	O	**DMA Cycle Request Output—DMA Controller 1 (Read):** This output pin is used to indicate that DMA transfers (Read) are requested by the T1/E1 Framer. On the receive side (i.e., To transmit data from HDLC buffers within the XRT86VL30 to external DMA Controller), DMA transfers are only requested when the receive buffer contains a complete message or cell. The DMA Read cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ1}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK1}}$) 'low' to indicate that it is ready to receive the data. The T1/E1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the $\overline{\text{RD}}$ is configured as a Read Strobe. If $\overline{\text{RD}}$ is configured as a direction signal, then the T1/E1 Framer would place new data on the Microprocessor data bus each time the Write Signal ($\overline{\text{WR}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it "High") when the Receive HDLC buffers are depleted.
$\overline{\text{INT}}$	96	59	O	**Interrupt Request Output:** This active-low output signal will be asserted when the XRT86VL30 device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the Microprocessor. The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.

MICROPROCESSOR INTERFACE

<table>
<tr><th>SIGNAL NAME</th><th>128-PIN#</th><th>80-PIN#</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>PCLK</td><td>68</td><td>39</td><td>I</td><td>Microprocessor Clock Input:
This clock input signal is only used if the Microprocessor Interface has been configured to operate in the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in this mode, then it will use this clock signal to do the following.
1. To sample the CS*, WR*/R/W*, A[11:0], D[7:0], RD*/DS* and DBEN input pins, and
2. To update the state of the D[7:0] and the RDY/DTACK output signals.
NOTES:
1. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.
When DMA interface is enabled, the PCLK input pin is also used by the T1/E1 Framer to latch in or latch out receive or output data respectively.</td></tr>
<tr><td>iADDR</td><td>124</td><td>n/a</td><td>I</td><td>This Pin Must be Tied “Low” for Normal Operation.
NOTE: This pin is internally pulled “Low”</td></tr>
<tr><td>fADDR</td><td>123</td><td>n/a</td><td>I</td><td>This Pin Must be Tied “High” for Normal Operation.
NOTE: This pin is internally pulled “High”</td></tr>
<tr><td>PTYPE0
PTYPE1
PTYPE2</td><td>127
126
125</td><td>78
77
76</td><td>I</td><td>Microprocessor Type Input:
These input pins permit the user to specify which type of Microprocessor/ Microcontroller to be interfaced to the XRT86VL30 device. The following table presents the three different microprocessor types that the XRT86VL30 supports.
<table><tr><th>° PType2</th><th>° PType1</th><th>° PType0</th><th>MICROPROCESSOR TYPE</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Intel Asynchronous</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Motorola Asynchronous</td></tr><tr><td>1</td><td>0</td><td>1</td><td>IBM POWER PC 403</td></tr></table>NOTE: These pins are internally pulled “Low”</td></tr>
</table>

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION

$\overline{\text{RDY}}$	74	43	O	**Ready/Data Transfer Acknowledge Output:**
				The exact behavior of this pin depends upon the type of Microprocessor/ Microcontroller the XRT86VL30 has been configured to operate in, as defined by the PTYPE[2:0] pins.
				Intel Asynchronous Mode - RDY* - Ready Output
				Tis output pin will function as the “active-low” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Motorola Asynchronous Mode - DTACK* - Data Transfer Acknowledge Output
				Tis output pin will function as the “active-low” DTACK output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Power PC 403 Mode - RDY Ready Output:
				This output pin will function as the “active-high” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic “high” level upon the rising edge of PCLK, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “low” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level.
				NOTE: *The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11	75 76 77 79 80 81 82 84 89 94 95 97	44 45 46 47 48 49 50 51 53 57 58 60	I	**Microprocessor Interface Address Bus Input** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations within the XRT86VL30 device whenever it performs READ and WRITE operations with the XRT86VL30 device. ***NOTE:*** *These pins are internally pulled "Low" , except ADDR [8:11].*
$\overline{\text{DBEN}}$	73	n/a	I	**Data Bus Enable Input pin.** This active-low input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. • Setting this input pin "low" enables the Bi-directional Data bus. • Setting this input pin "high" tri-states the Bi-directional Data Bus. ***NOTE:*** *This pin is internally pulled "Low"*
ALE	93	56	I	**Address Latch Enable Input Address Strobe** The exact behavior of this pin depends upon the type of Microprocessor/ Microcontroller the XRT86VL30 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - ALE** This active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[11:0]) into the XRT86VL30 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus input pins (A[11:0]). The contents of the Address Bus will be latched into the XRT86VL30 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - AS*** This active-low input pin is used to latch the data residing on the Address Bus, A[11:0] into the Microprocessor Interface circuitry of the XRT86VL30 device. Pulling this input pin "low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the falling edge of this signal. **Power PC 403 Mode - No Function -Tie to GND:** This input pin has no role nor function and should be tied to GND.
$\overline{\text{CS}}$	108	68	I	**Microprocessor Interface—Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT86VL30 on-chip registers and buffer/memory locations.

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
$\overline{RD}$	71	42	I	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/ Microcontroller the Framer has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** This input pin will function as the RD* (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT86VL30 device will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - DS* - Data Strobe:** This input pin will function as the DS* (Data Strobe) input signal. **Power PC 403 Mode - WE* - Write Enable Input:** This input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR/R/W*) also being asserted (at a logic low level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the “target” on-chip register or buffer location within the XRT86VL30 device.

MICROPROCESSOR INTERFACE

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
$\overline{WR}$	107	67	I	**Microprocessor Interface—Write Strobe Input** The exact behavior of this pin depends upon the type of Microprocessor/ Microcontroller the XRT86VL30 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - WR* - Write Strobe Input:** This input pin functions as the WR* (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT86VL30) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** This pin is functionally equivalent to the "R/W*" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **Power PC 403 Mode - R/W* - Read/Write Operation Identification Input:** This input pin will function as the "Read/Write Operation Identification Input" pin. Anytime the Microprocessor Interface samples this input signal at a logic low (while also sampling the CS* input pin "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[11:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT86VL30 device) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the CS* input pin a logic "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[11:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT86VL30).

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
$\overline{ACK0}$	62	35	I	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. **2.** When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle. *This pin is internally pulled "High"*
$\overline{ACK1}$	65	38	I	**DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. **2.** When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle. ***NOTE:*** *This pin is internally pulled "High"*
BLAST	100	n/a	I	**Last Cycle of Burst Indicator Input:** The Microprocessor asserts this pin "Low" when it is performing its last read or write cycle, within a burst operation. ***NOTE:*** *This pin is internally pulled "High"*
$\overline{RESET}$	85	52	I	**Hardware Reset Input** $\overline{Reset}$ is an active low input. If this pin is pulled "Low" for more than 10µS, the device will be reset. When this occurs, all output will be 'tri-stated', and all internal registers will be reset to their default values.

1.8V POWER SUPPLY PINS

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
DVDD1v8	4, 41, 56, 63, 78, 105	1, 23, 36, 65	PWR	Framer Block Power Supply
AVDD1v8	16	11	PWR	
VDDPLL1v8	20, 21	13, 14	PWR	Analog Power Supply for PLL

3.3V POWER SUPPLY PINS

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
DVDD3v3	2, 37, 52, 92	80, 21, 28	PWR	Framer Block Power Supply
RVDD3v3	15	10	PWR	Receiver Analog Power Supply for LIU Section
TVDD3v3	7	4	PWR	Transmitter Analog Power Supply for LIU Section

GROUND PINS

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
DGND	5, 29, 48, 60, 72, 83, 87, 102, 109, 110	2, 27, 33, 62, 69, 70, 71	GND	Framer Block Ground
AGND	17	12	GND	Analog Ground for LIU Section
RGND	12	7	GND	Receiver Analog Ground for LIU Section
TGND	9	6	GND	Transmitter Analog Ground for LIU Section
PLLGND	22, 23	15, 16	GND	Analog Ground for PLL

NO CONNECT PINS

SIGNAL NAME	128-PIN#	80-PIN#	TYPE	DESCRIPTION
NC	3, 34, 35, 66, 67, 98, 99	n/a	NC	Not Connected

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply..... VDD_{IO} .. .. -0.5V to +3.465V VDD_{CORE}.....-0.5V to +1.890V Storage Temperature .....-65℃ to 150℃ Operating Temperature Range.....-40℃ t o 85℃ Supply Voltage ..... GND-0.5V to +VDD + 0.5V Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V Input Current (Any Pin) ..... ± 100mA ESD Protection (HBM).....>2000V	Power Rating 80pin LQFP Package.....0.976W (at zero air flow) Power Rating 128pin LQFP Package.....0.760W (at zero air flow) XRT86VL30IV80 Theta ja-0 .....41.0 C/W (0 lfpm) XRT86VL30IV80 Theta ja-100 ..... 38.5 C/W (100 lfpm) XRT86VL30IV80 Theta ja-200 ..... 37.0 C/W (200 lfpm) XRT86VL30IV128 Theta ja-0 .....52.61 C/W (0 lfpm) XRT86VL30IV128 Theta ja-100 ..... 46.6 C/W (100 lfpm) XRT86VL30IV128 Theta ja-200 ..... 44.8 C/W (200 lfpm)

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25℃, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
V_{OH}	Output High Voltage	2.4		VDD	V	I_{OH} = 40µA
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current (with No Pull-Up or Pull_Down resistor)	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current (with No Pull-Up or Pull_Down resistor)	-10		10	µA	V_{IL} = GND
PU_{IL}	Input Leakage (Input with Pull-Up resistor)	-120		10	µA	V_I = VDD or GND
PD_{IL}	Input Leakage (Input with Pull-Down resistor)	-10		120	µA	V_I = VDD or GND

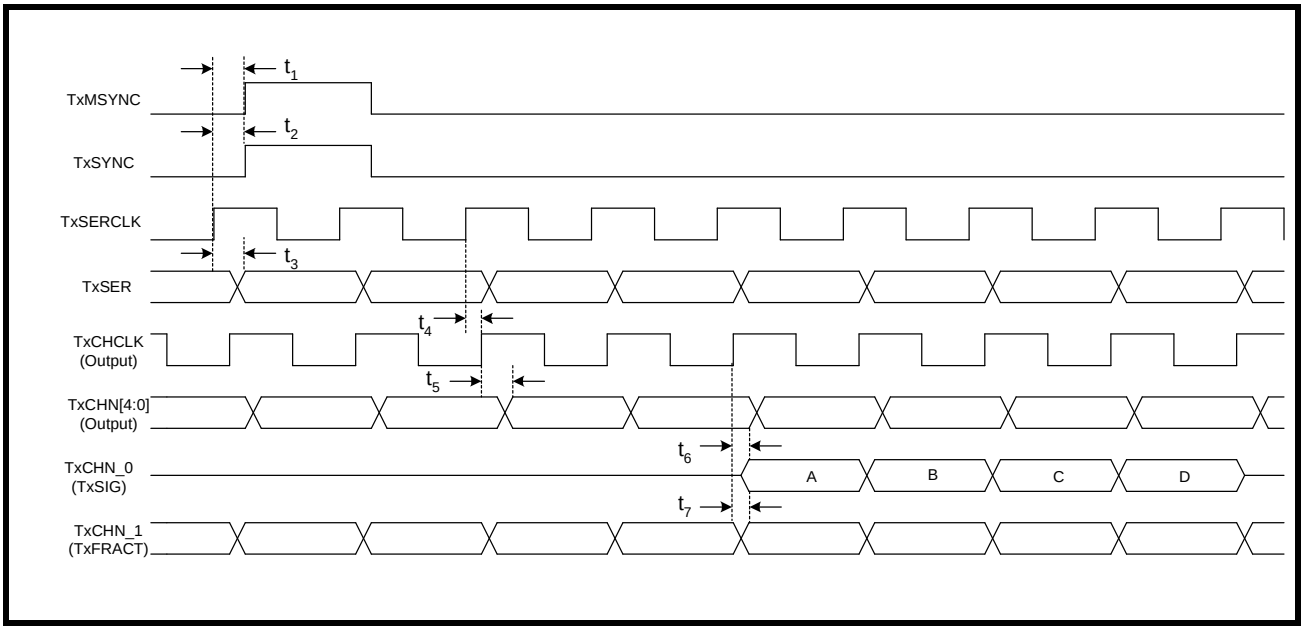
TABLE 1: XRT86VL30 POWER CONSUMPTION

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% , T_A=25°C, UNLESS OTHERWISE SPECIFIED									
MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V 3.3V 3.465V	75Ω	Internal	1:1	1:2	310 359	 446	mW	PRBS Pattern All ones All ones
E1	3.3V 3.3V 3.465V	120Ω	Internal	1:1	1:2	300 336	 418	mW	PRBS Pattern All ones All ones
T1	3.3V 3.3V 3.465V	100Ω	Internal	1:1	1:2	288 344	 425	mW	PRBS Pattern All ones All ones

AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	TxSERCLK to TxMSYNC delay			234	nS	
t_2	TxSERCLK to TxSYNC delay			230	nS	
t_3	TxSERCLK to TxSER data delay			230	nS	
t_4	Rising Edge of TxSERCLK to Rising Edge of TxCH-CLK			13	nS	
t_5	Rising Edge of TxCHCLK to Valid TxCHN[4:0] Data			6	nS	
t_6	TxSERCLK to TxSIG delay			230	nS	
t_7	TxSERCLK to TxFRACT delay			110	nS	

FIGURE 1. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (BASE RATE/NON-MUX)



AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RxSERCLK as an Output						
t_8	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			4	nS	
t_9	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			4	nS	
t_{10}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{11}	Rising Edge of RxSERCLK to Rising Edge of RxSER			6	nS	
t_{12}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			6	nS	
RxSERCLK as an Input						
t_{13}	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			8	nS	

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25℃, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{14}	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			8	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			10	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{16}	Rising Edge of RxSERCLK to Rising Edge of RxSER			10	nS	
t_{17}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			9	nS	

FIGURE 2. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

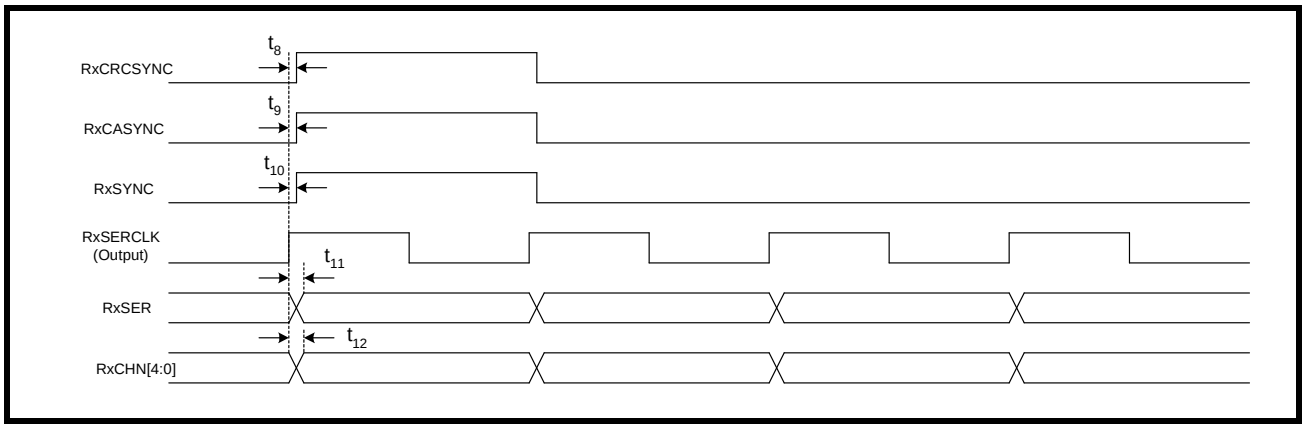
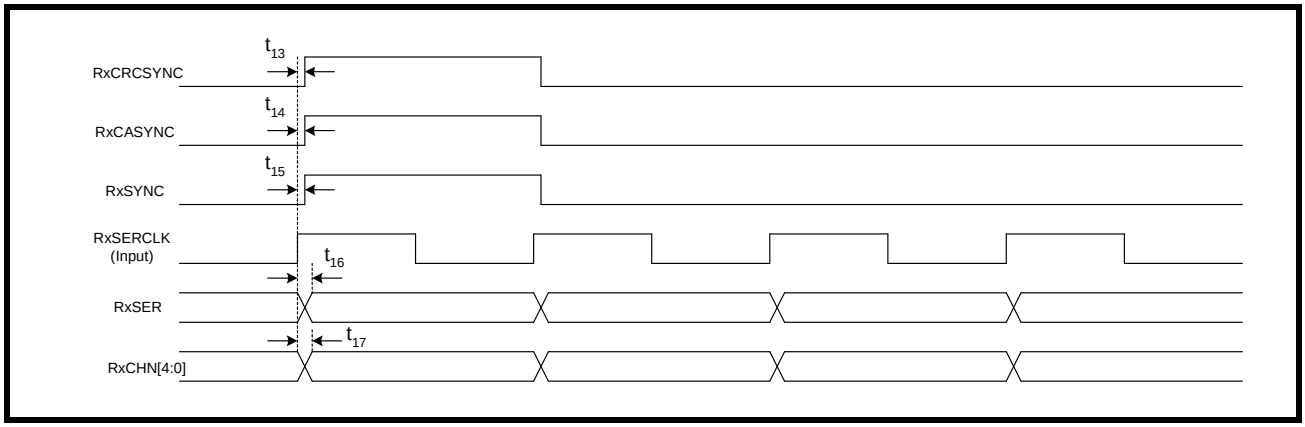


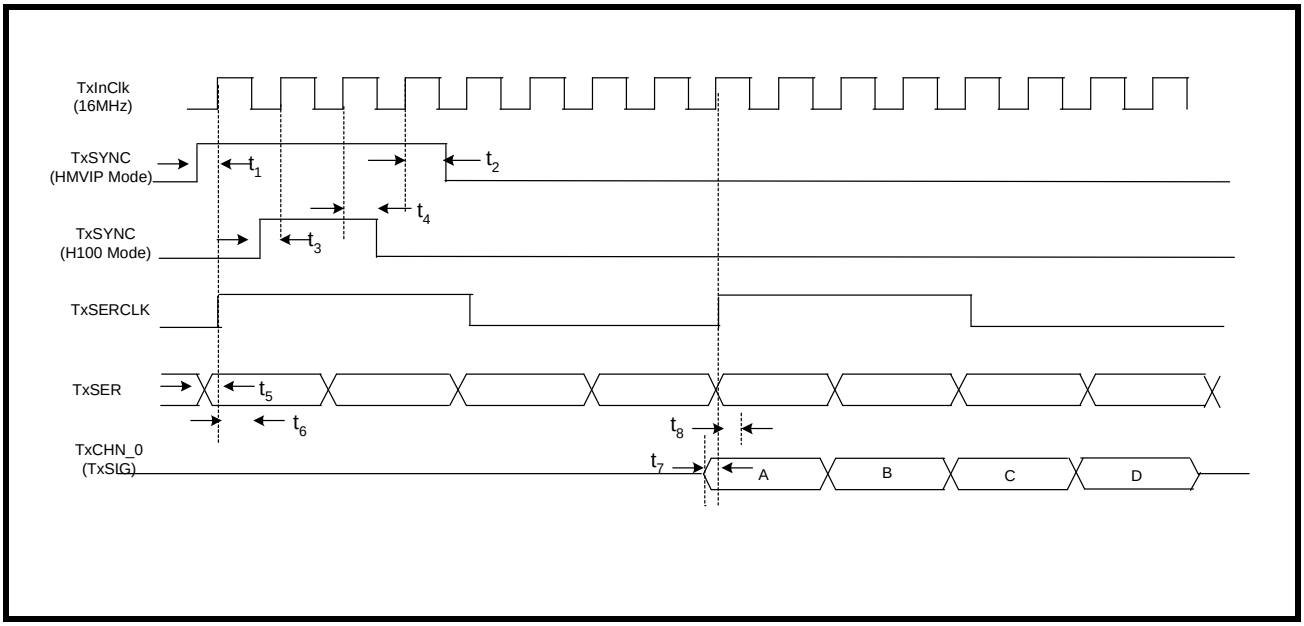
FIGURE 3. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN INPUT)



AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	TxSYNC Setup Time - HMVIP Mode	7			nS	
t_2	TxSYNC Hold Time - HMVIP Mode	4			nS	
t_3	TxSYNC Setup Time - H100 Mode	7			nS	
t_4	TxSYNC Hold Time - H100 Mode	4			nS	
t_5	TxSER Setup Time - HMVIP and H100 Mode	6			nS	
t_6	TxSER Hold Time - HMVIP and H100 Mode	3			nS	
t_7	TxSIG Setup Time - HMVIP and H100 Mode	6			nS	
t_8	TxSIG Hold Time - HMVIP and H100 Mode	3			nS	

FIGURE 4. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (HMVIP AND H100 MODE)



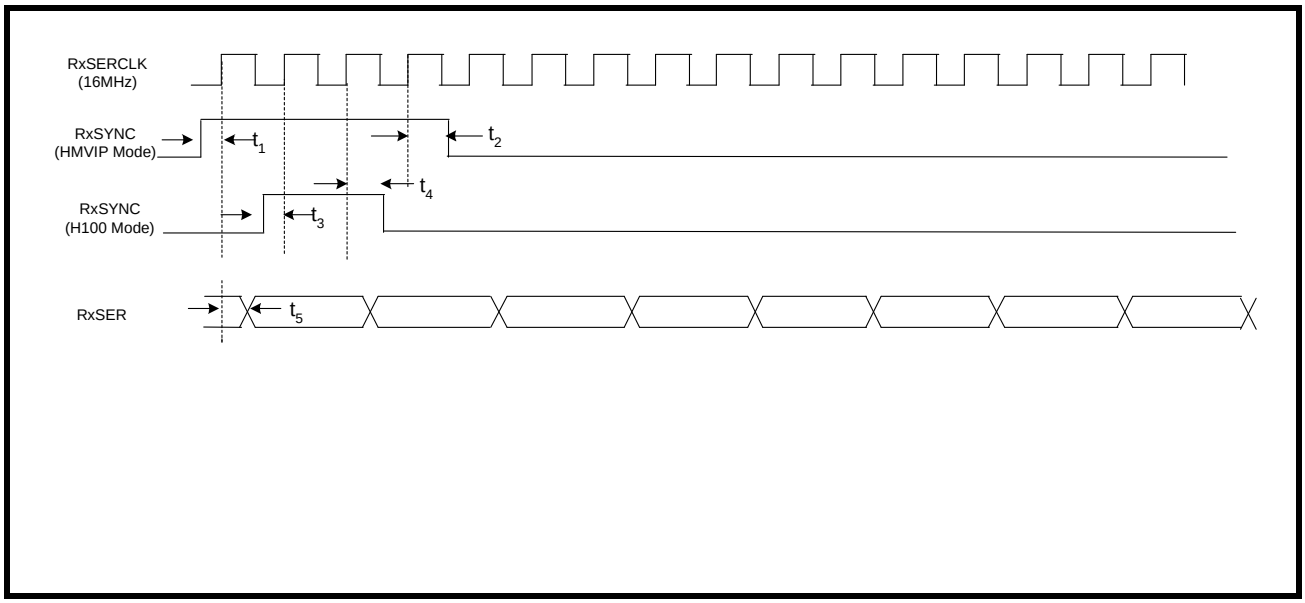
NOTE: *Setup and Hold time is not valid from TxInClk to TxSERCLK as TxInClk is used as the timing source for the back plane interface and TxSERCLK is used as the timing source on the line side.*

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	RxSYNC Setup Time - HMVIP Mode	4			nS	
t_2	RxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	RxSYNC Setup Time - H100 Mode	5			nS	
t_4	RxSYNC Hold Time - H100 Mode	3			nS	
t_5	Rising Edge of RxSERCLK to Rising Edge of RxSER delay			11	nS	

NOTE: *Both RxSERCLK and RxSYNC are inputs*

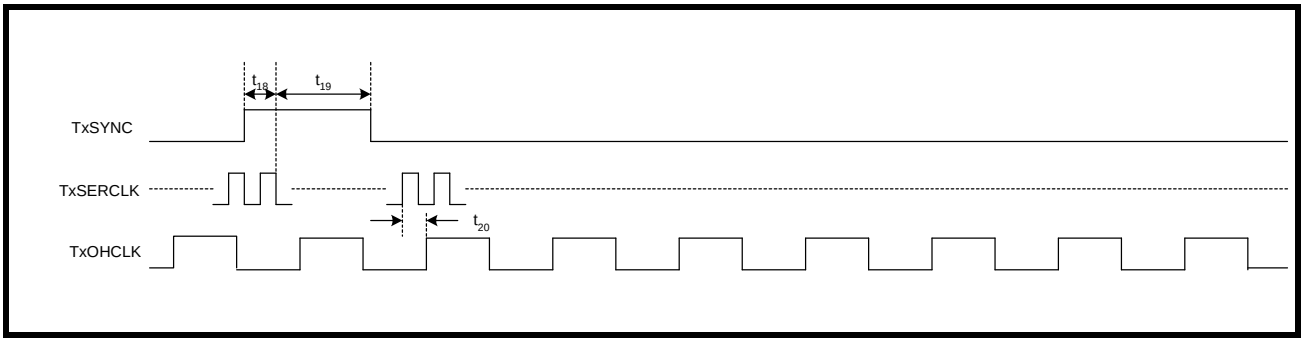
FIGURE 5. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (HMVIP/H100 MODE)



AC ELECTRICAL CHARACTERISTICS TRANSMIT OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{18}	TxSYNC Setup Time (Falling Edge TxSERCLK)	6			nS	
t_{19}	TxSYNC Hold Time (Falling Edge TxSERCLK)	4			nS	
t_{20}	Rising Edge of TxSERCLK to TxOHCLK			12	nS	

FIGURE 6. FRAMER SYSTEM TRANSMIT OVERHEAD TIMING DIAGRAM



AC ELECTRICAL CHARACTERISTICS RECEIVE OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RxSERCLK as an Output						
t_{21}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{22}	Rising Edge of RxSERCLK to Rising Edge of RxOHCLK			6	nS	
t_{23}	Rising Edge of RxSERCLK to Rising Edge of RxOH			8	nS	
RxSERCLK as an Input						
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			12	nS	
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{25}	Rising Edge of RxSERCLK to Rising Edge of RxOHCLK			12	nS	
t_{26}	Rising Edge of RxSERCLK to Rising Edge of RxOH			15	nS	

FIGURE 7. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

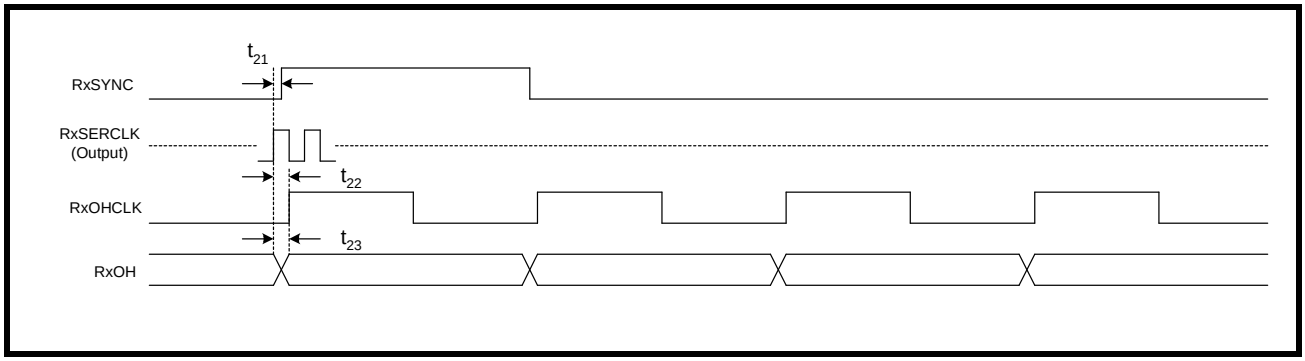


FIGURE 8. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN INPUT)

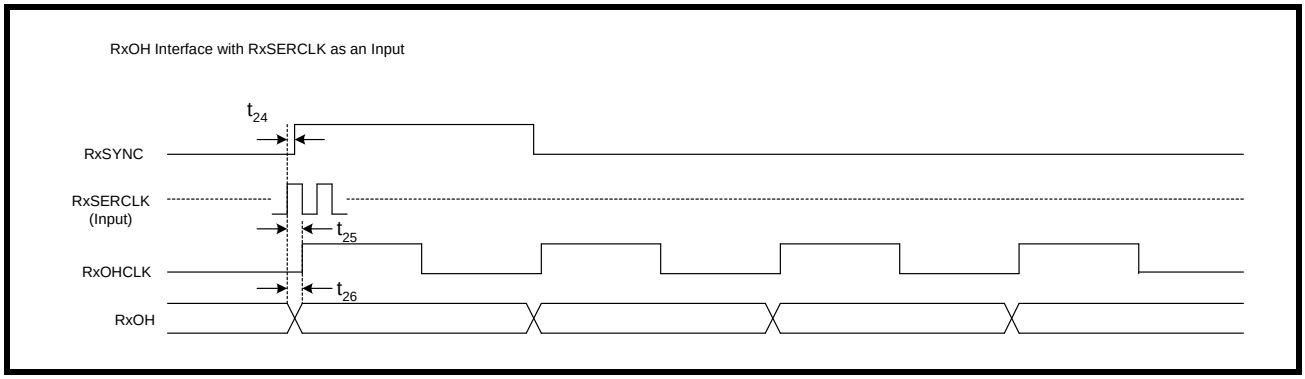


TABLE 2: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A= -40°to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal: Number of consecutive zeros before RLOS is set Input signal level at RLOS RLOS De-asserted	 15 12.5	 32 20		 dB % ones	Cable attenuation @1024kHz ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Receiver Sensitivity (Long Haul with cable loss) Normal Extended	 0 0	 43	 36 	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Input Impedance		15		kΩ	
Input Jitter Tolerance: 1 Hz 10kHz-100kHz	 37 0.3			 UIpp UIpp	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 -	 20 	 0.5	 kHz dB	ITU G.736
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0) (JABW=1)	-	10 1.5	-	Hz Hz	ITU G.736
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 12 8 8	 - 	 - 	 dB dB dB	ITU-G.703

TABLE 3: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)					With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0	45		dB	
Input Impedance		15	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	10	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	3		Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	14	-	dB	
102kHz - 2048kHz	-	20	-	dB	
2048kHz - 3072kHz	-	16	-	dB	

TABLE 4: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40°to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.13 2.70	 2.37 3.00	 2.60 3.30	 V V	1:2 Transformer
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 15 9 8	 - - -	 - - -	 dB dB dB	 ETSI 300 166

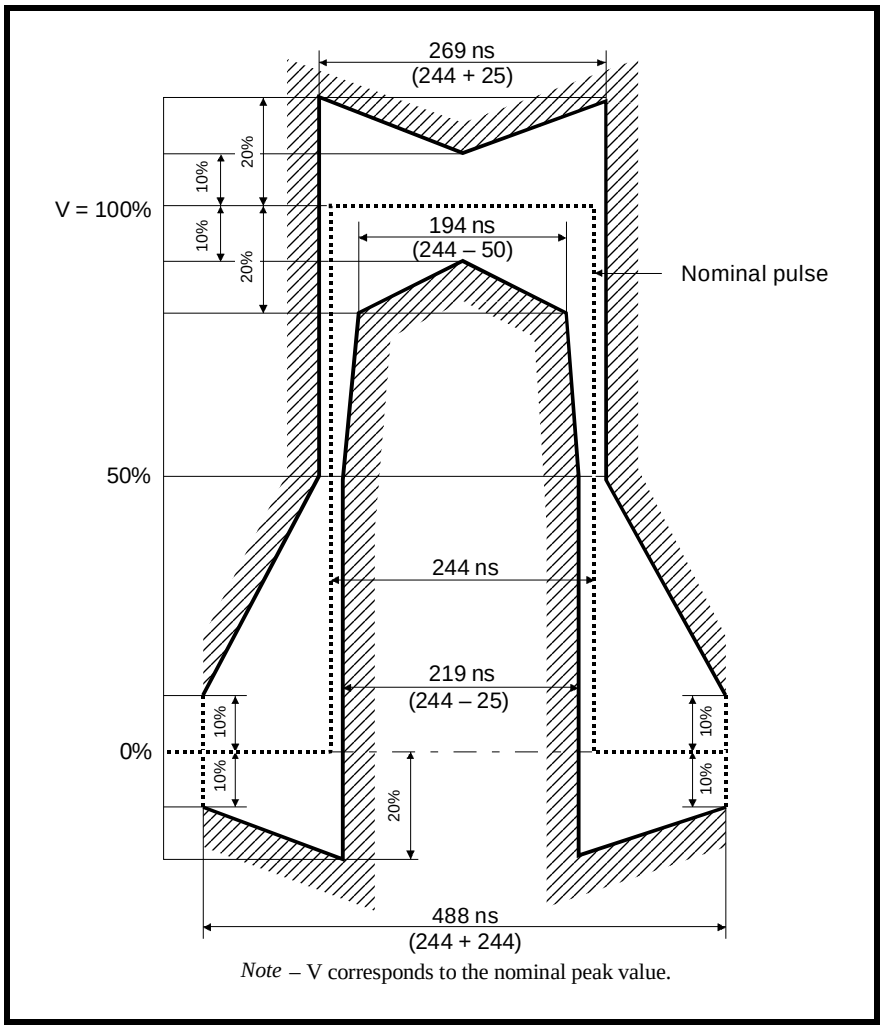
TABLE 5: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	**RETURN LOSS ETS 300166**
51-102kHz	6dB
102-2048kHz	8dB
2048-3072kHz	8dB

TABLE 6: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	1:2 Transformer measured at DSX_1.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 - - -	 17 12 10	 - - -	 dB dB dB	

FIGURE 9. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 7: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 10. ITU G.703 SECTION 13 SYNCHRONOUS INTERFACE PULSE TEMPLATE

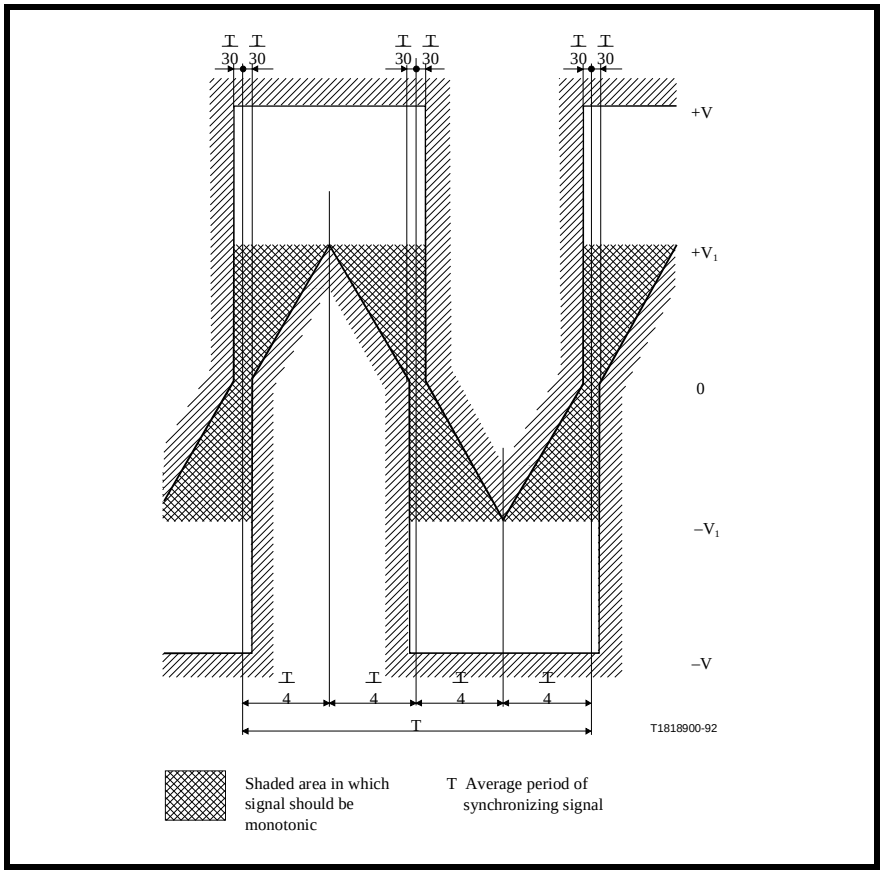


TABLE 8: E1 SYNCHRONOUS INTERFACE TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Maximum Peak Voltage of a Mark	1.5V	1.9V
Minimum Peak Voltage of a Mark	0.75V	1.0V
Nominal Pulse width	244ns	244ns

FIGURE 11. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

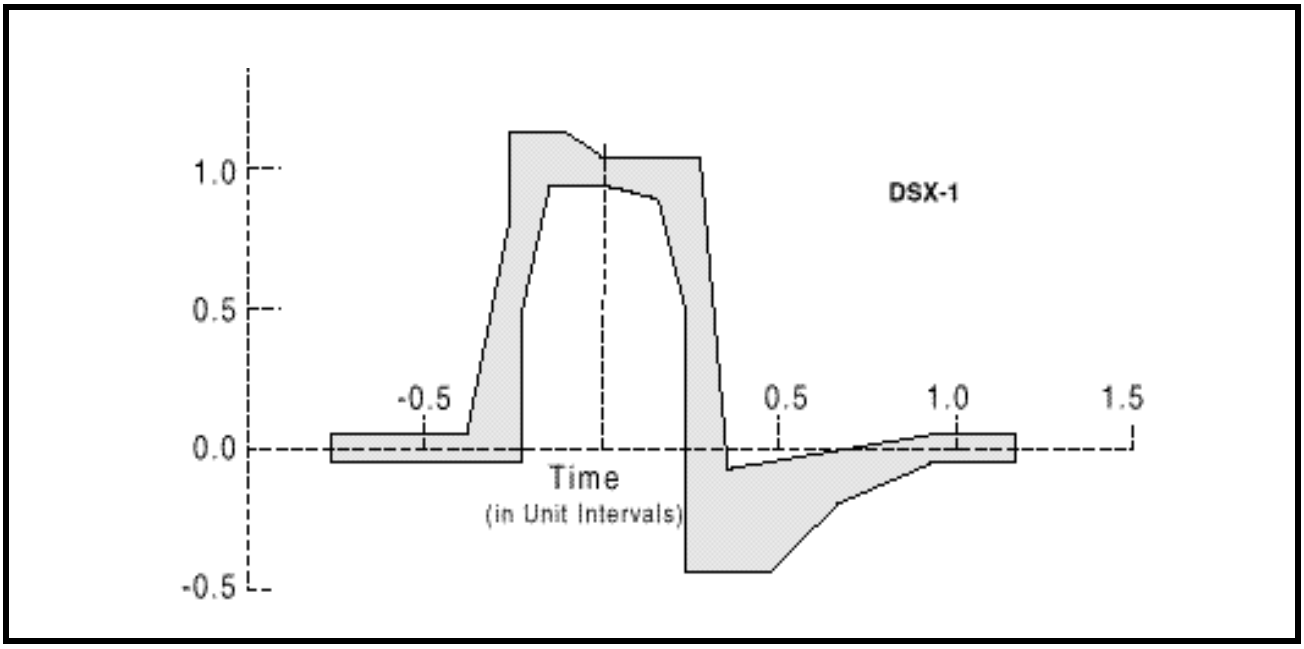


TABLE 9: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 10: AC ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
MCLKIN Clock Duty Cycle		40	-	60	%
MCLKIN Clock Tolerance		-	±50	-	ppm

MICROPROCESSOR INTERFACE I/O TIMING

INTEL INTERFACE TIMING - ASYNCHRONOUS

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80188 family of microprocessors. The ALE signal can be tied 'HIGH' if this signal is not available, and the corresponding timing interface is shown in **Figure 13** and **Table 12.**

FIGURE 12. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS NOT TIED 'HIGH'

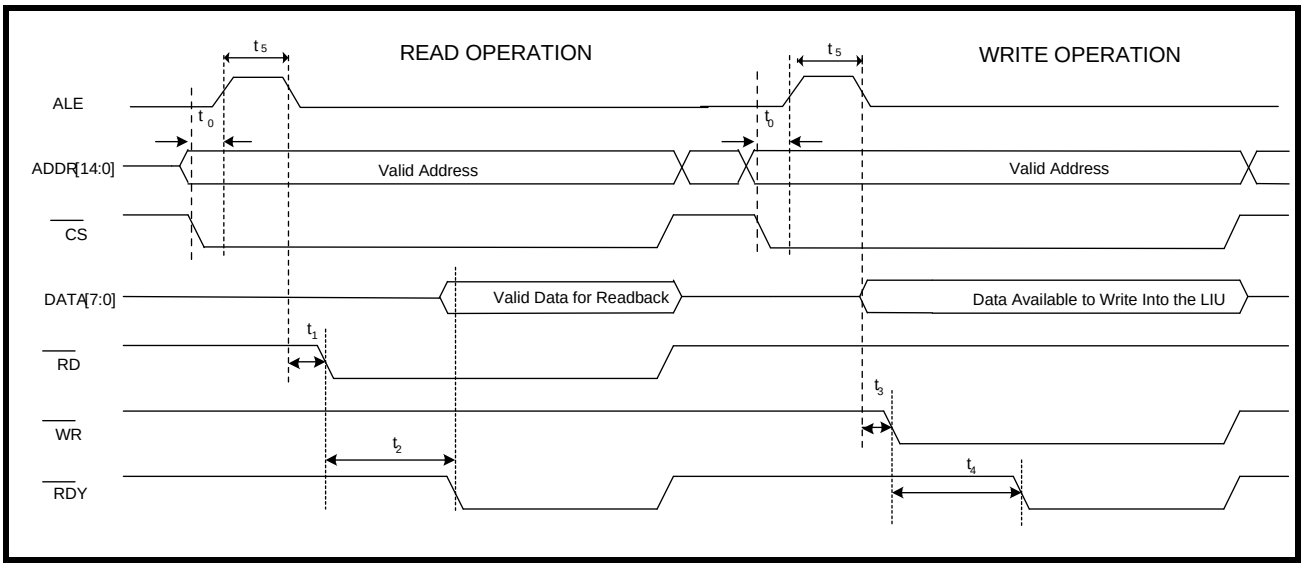


TABLE 11: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge and ALE Rising Edge	0	-	ns
t_1	ALE Falling Edge to $\overline{RD}$ Assert	5	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	ALE Falling Edge to $\overline{WR}$ Assert	5	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns
t_5	ALE Pulse Width(t_5)	10		ns

FIGURE 13. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS TIED 'HIGH'

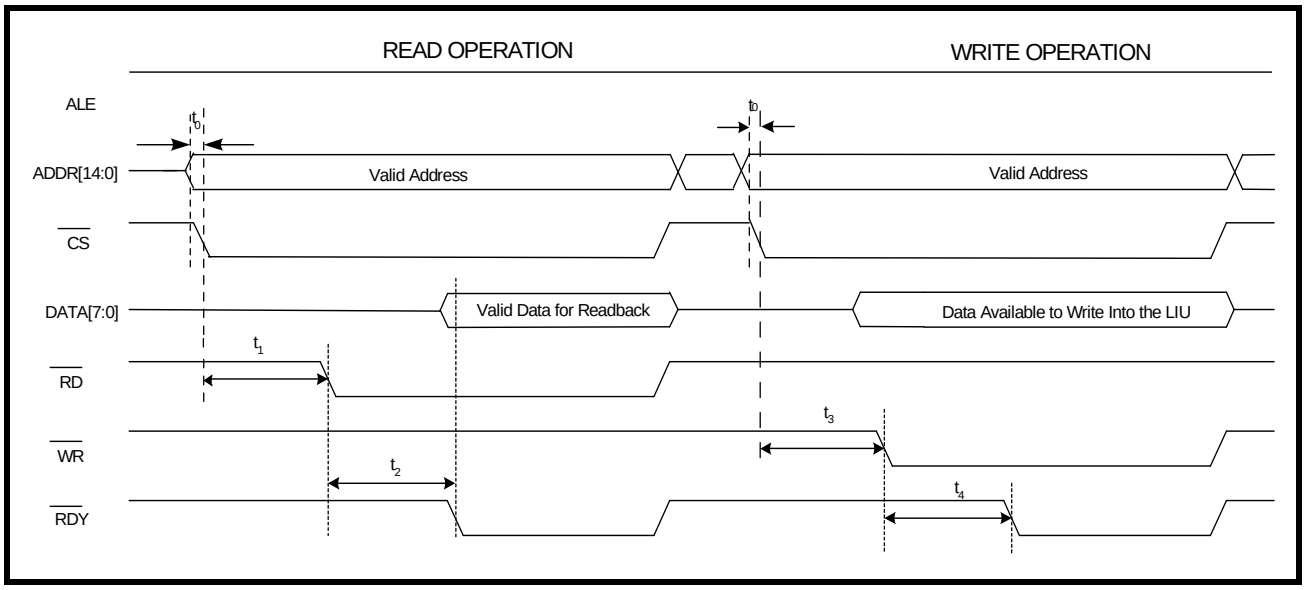


TABLE 12: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns

MOTOROLA ASYNCHRONOUS INTERFACE TIMING

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family. The interface timing is shown in **Figure 14**. The I/O specifications are shown in **Table 13**.

FIGURE 14. MOTOROLA ASYNCHRONOUS MODE INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

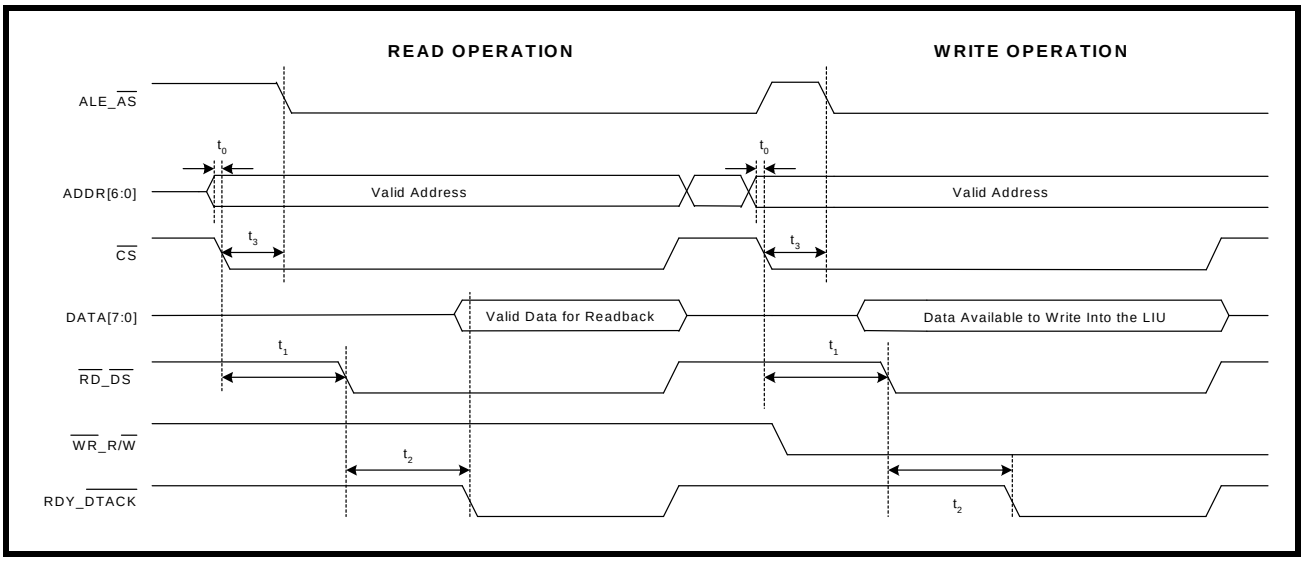


TABLE 13: MOTOROLA ASYNCHRONOUS MODE MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}\_\overline{DS}$) Assert	0	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	320	ns
NA	$\overline{DS}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_AS) Falling Edge	0	-	ns

POWER PC 403 SYCHRONOUS INTERFACE TIMING

The signals used in the Power PC 403 Synchronus microprocessor interface mode are: Address Strobe (AS), Microprocessor Clock (uPCLK), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface timing is shown in **Figure 15**. The I/O specifications are shown in **Table 14**.

FIGURE 15. POWER PC 403 INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

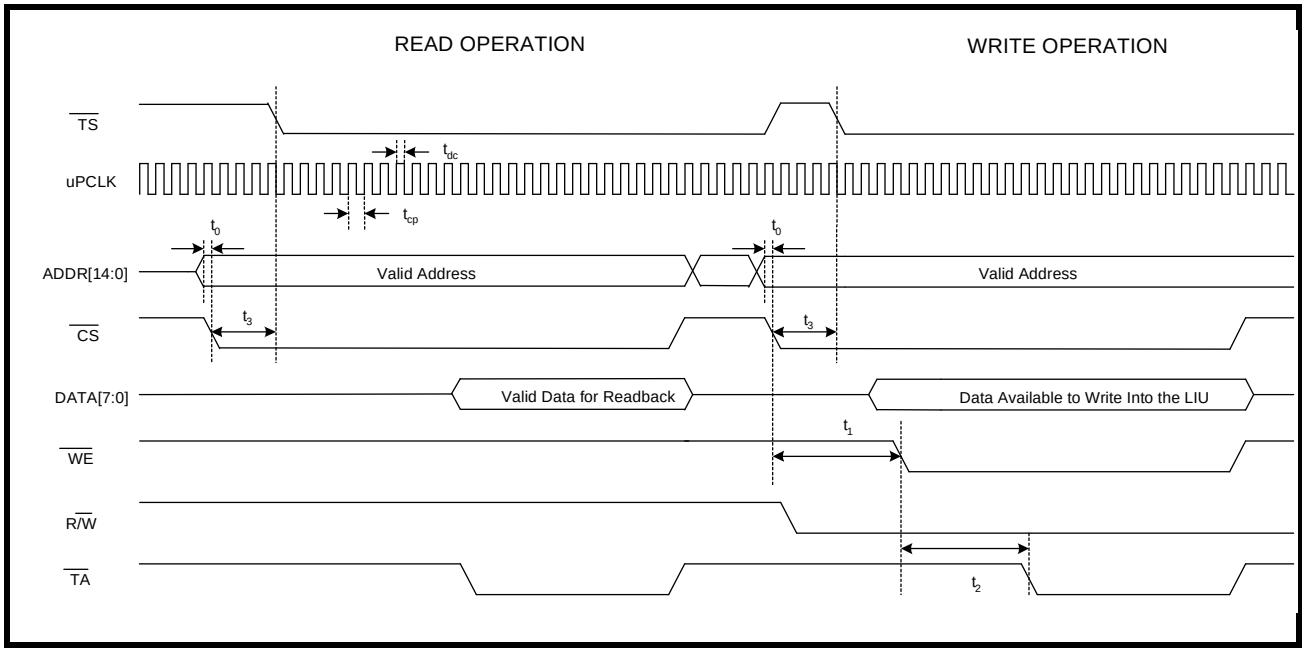


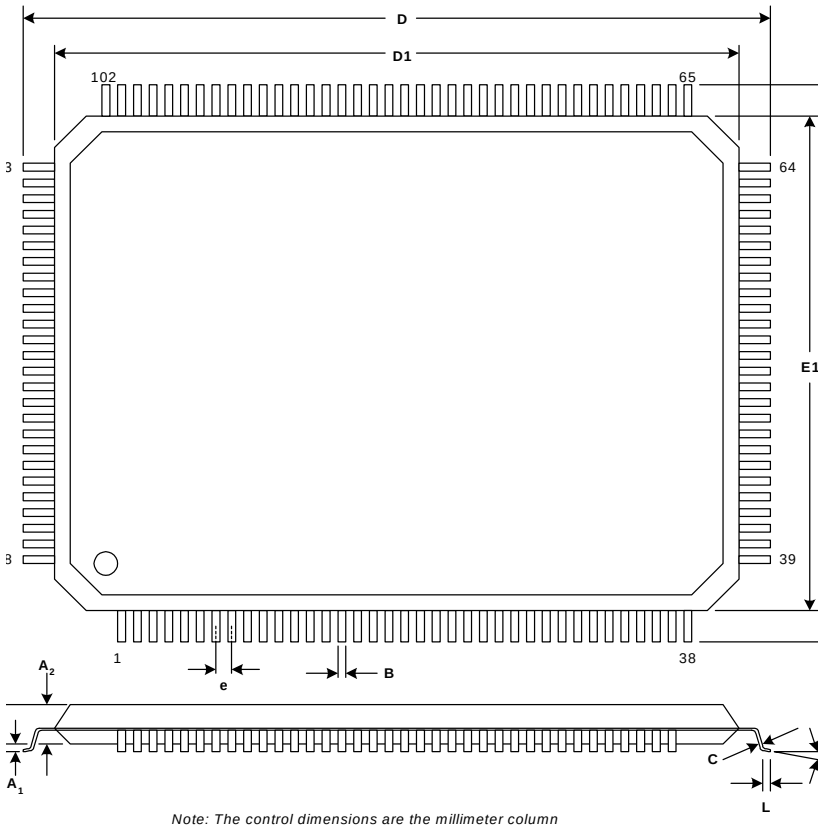
TABLE 14: POWER PC 403 MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	320	ns
NA	$\overline{WE}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL30IV	128 PIn LQFP (14x20x1.4mm)	-40°C to +85°C
XRT86VL30IV80	80 Pin LQFP (12x12x1.4mm)	-40°C to +85°C

PACKAGE DIMENSIONS FOR 128 LQFP



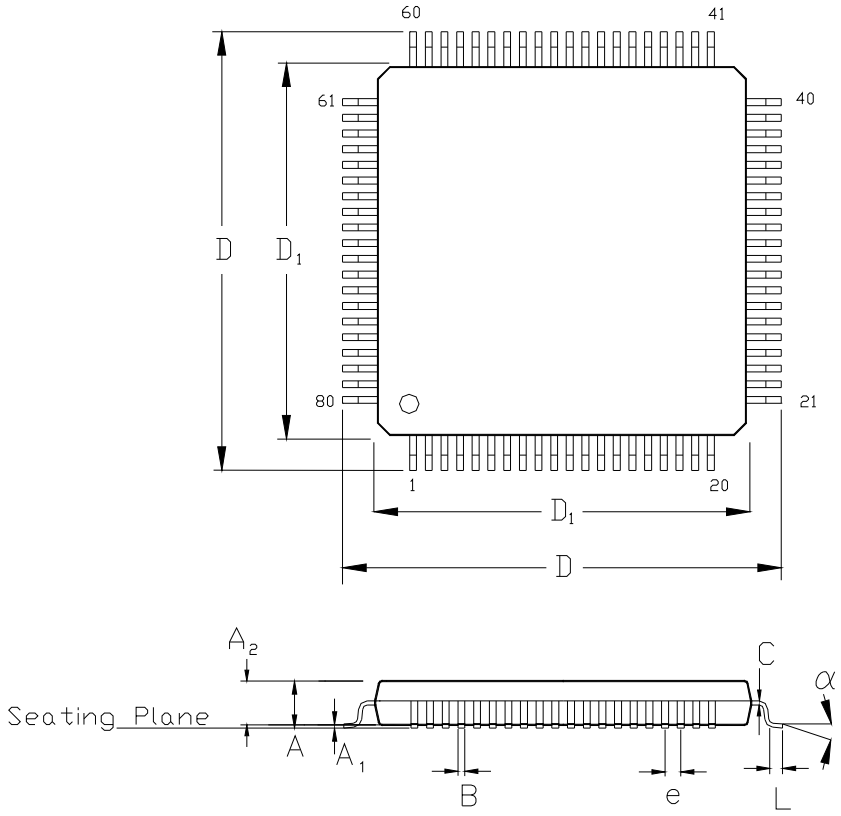
Note: The control dimensions are the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0551	0.0630	1.40	1.60
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
B	0.0067	0.0106	0.17	0.27
C	0.0035	0.0079	0.09	0.20
D	0.8583	0.8740	21.80	22.20
D1	0.7835	0.7913	19.90	20.10
E	0.6220	0.6378	15.80	16.20
E1	0.5472	0.5551	13.90	14.10
e	0.0197 BSC		0.50 BSC	
L	0.0177	0.0295	0.45	0.75
α	0°	7°	0°	7°

PACKAGE DIMENSIONS FOR 80 LQFP

E

80 LEAD LOW-PROFILE QUAD FLAT PACK
(12 x 12 X 1.4 mm LQFP)
Rev. 1.00



Note: The control dimension is in the millimeter column

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.543	0.559	13.80	14.20
D1	0.465	0.480	11.80	12.20
e	0.0197 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	May 30,2008	Initial release of the XRT86VL30 datasheet.
1.0.1	August 08, 2008	Remove SPI functionality descriptions from data sheet.
1.0.2	August 15, 2008	Update Pin Description tables with pin number information for 80pin package.
1.03	September 9, 2008	Update power consumption numbers and thermal characteristics in electrical table.
1.0.4	December 18, 2009	80-pin Package 1. Removed reference to TRST on page 29 (removed note to ground this pin) 2. Added pin 71 to DGND list on page 37

NOTICE

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