# DA7212 stereo CODEC with enhanced automatic level controller and 1.2W speaker driver

## GENERAL DESCRIPTION

DA7212 is a high performance, low-power audio codec with an enhanced hybrid ALC and a powerful speaker driver targeting portable and embedded applications. The audio front-end simultaneously supports stereo FM line input with four analogue (or two analogue and two digital) microphones with two independent microphone biases. Comprehensive analogue mixing and bypass paths to the output drivers are available.

The headphone output is true-ground Class-G with integrated charge pump. There is also a differential Class AB speaker driver that can serve as a mono lineout.

Digital audio transfer to/from the external processor is via a bidirectional I2S interface that supports all common sample rates. The device may be operated in slave or master modes using the internal PLL which may be bypassed if not required.

To fully optimise each customer application, a range of built-in filtering, equalisation and audio enhancements are available. These are accessible by the processor over the I2C serial interface and can be used to minimise latency and power consumption.

***DA7212 chip: WLCSP34, with a staggered 0.5mm pitch***

## KEY FEATURES

- 100dB stereo audio playback into 16-32 ohm headphones
- 67mW headphone driver into 16Ω at 2.5V;
    - Minimal external components: a capless, true-ground driver eliminates bulky headphone coupling capacitors
- 1.2W mono speaker driver
- 3.1mW quiescent power consumption for DAC to headphone playback
- Single supply operation
- Stereo digital microphone support
- Supports up to four microphones with two separate low-noise microphone-bias outputs
- Low-power PLL provides system clocking and audio sample rate flexibility
- Built-in 5-band equaliser, ALC and noise-gate functions
- Built-in beep generator that outputs all DTMF keypad values, as well as mixing two independently configurable sine waves between 10Hz and 12kHz
- 34-ball WLCSP (4.54mm x 1.66mm) package
- Staggered 0.5mm pitch for easy PCB routing

## APPLICATIONS

- Personal Media Players
- Audio headphone/headsets
- Wearables
- Embedded applications
- Arduino compatible development systems



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## SYSTEM OVERVIEW

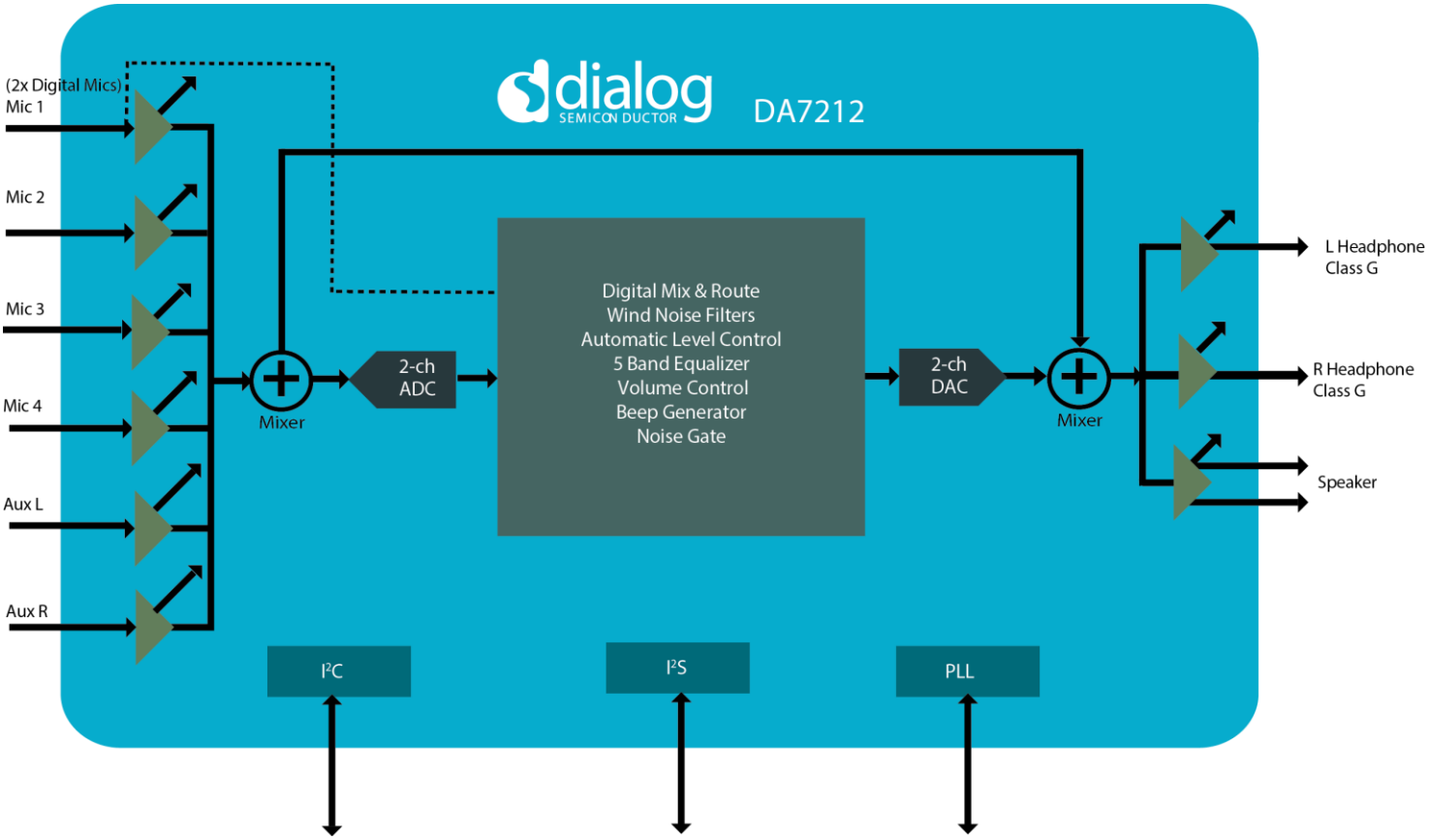


***Figure 1: Component values shown for a typical application***



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## POWER SUPPLY BLOCKS

### Audio Parametrics

#### Analogue to Digital Converter (ADC)

| PARAMETER | SYMBOL | TEST CONDITIONS | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| Full-scale input signal | $V_{MAX}$ | Digital output level = 0dBFS | | 1.6 × VDDA | | $V_{PP}$ |
| Signal to Noise Ratio | SNR[2] | A-weighted<br>no input selected | | 90 | | dB |
| Total Harmonic Distortion plus Noise | THD+N[3] | -1dBFS<br>44.1kHz slave mode | | -85 | | dB |
| | | -1dBFS<br>32kHz PLL mode | | -80 | | dB |
| In-band Spurious | | Analog input level = 0dBFS | | -85 | | dB |
| Channel separation | | | | 90 | | dB |
| Pass band | $B_{PASS}$ | | | | 0.45*Fs | Hz |
| Stop band | $B_{STOP}$ | Fs ≤ 48kHz<br>Fs = 88.2/96kHz | 0.56*Fs | | 7*Fs<br>3.5*Fs | Hz |
| Pass band Ripple | | Voice mode<br>Music mode | | | ±0.3<br>±0.1 | dB |
| Stop band Attenuation | | Voice mode<br>Music mode | 70<br>55 | | | dB |
| Group delay | | Voice mode<br>Music mode<br>Fs = 88.2/96kHz | | 4.3/Fs<br>18/Fs<br>9/Fs | 600 | µs |
| Group delay mismatch | | Between left and right channels | | | 2 | µs |
| Power Supply Rejection Ratio | PSRR[4] with respect to VDDA | 20Hz – 2kHz<br>20kHz | 70<br>50 | | | dB |

[2] SNR (signal-to-noise ratio) is a ratio of the full-scale output signal level to the noise level with no signal applied.
[3] THD+N (total harmonic distortion plus noise) is a ratio of the level of the harmonics and noise to the output signal.
[4] PSRR (power supply rejection ratio) is a measure of the attenuation of a signal on the supply to the signal at the output.



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**Microphone Bias**

| MICBIAS1 and MICBIAS2 | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **Min** | **Typ** | **Max** | **UNIT** |
| Bias Voltage | $V_{MICBIAS}$ | No load, VDD_MIC > $V_{MICBIAS}$ + 200mV | 1.52 | 1.57 | 1.62 | V |
| | | | 2.18 | 2.25 | 2.32 | |
| | | | 2.41 | 2.48 | 2.56 | |
| | | | 2.91 | 3.00 | 3.10 | |
| Maximum Current | $I_{BIAS}$ | Voltage drop < 50mV | | 2 | | mA |
| Power Supply Rejection Ratio | PSRR with respect to VDD_MIC | 20Hz – 200Hz<br>>2kHz | 70<br>50 | | | dB |
| Output Noise Voltage | $V_{NOISE}$ | VMICBIAS ≤ 2.2V | | 5 | | $\mu V_{RMS}$ |
| Capacitive Load | | $I_{BIAS}$ < 100uA<br>100uA < $I_{BIAS}$ < 2mA | | 100<br>200 | | pF |

**Input Mixing Units**

| (MIC1_P/MIC1_N/MIC2_P/MIC2_N/AUX_L/AUX_R ) to ADC_L/ADC_R | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **Min** | **Typ** | **Max** | **UNIT** |
| Full-scale input signal | VMAX | Single-ended<br>Differential<br>MICn_PGA = AUXx_PGA = INx_PGA = 0dB | | 0.8 × VDD_A<br>1.6 × VDD_A | | $V_{PP}$ |
| Input resistance | RIN | MIC, single-ended<br>AUX | 12<br>6 | 15 | 18<br>40 | kΩ |
| Input capacitance | CIN | | | 1 | | pF |
| Amplitude ripple | | 20Hz to 20kHz | -0.5 | | +0.5 | dB |
| Programmable gain | | MIC1_PGA and MIC2_PGA<br>AUXL_PGA and AUXR_PGA<br>INL_PGA and INR_PGA | -6<br>-54<br>-4.5 | | 36<br>15<br>18 | dB |
| Programmable gain step size | | MIC1_PGA and MIC2_PGA<br>AUXL_PGA and AUXR_PGA<br>INL_PGA and INR_PGA | | 6<br>1.5<br>1.5 | | dB |
| Absolute gain accuracy | | 0dB @ 1kHz | -1.0 | | +1.0 | dB |
| Left/Right gain mismatch | | 20Hz to 20kHz | -0.1 | | +0.1 | dB |



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| | | | | | | |
|---|---|---|---|---|---|---|
| Gain step error | | 20Hz to 20kHz | -0.1 | | +0.1 | dB |
| Input noise level | | Inputs connected to GND, A-weighted, input-referred, measured @ ADC output<br>MIC1/2_PGA = 24dB<br>AUXL/R_PGA = 15dB | | <br>5<br>6.5 | | $\mu V_{RMS}$ |
| Input Amplifier SNR | | Differential, A-weighted, input-referenced. | | 110 | | dB |
| Power supply rejection ratio | PSRR with respect to VDDA | Single-ended input<br>20Hz to 2kHz<br>20kHz | <br>70<br>50 | | | dB |
| | | Differential input<br>20Hz to 2kHz<br>20kHz | <br>90<br>70 | | | dB |

## Audio Outputs

### Digital to Analogue Converter (DAC)

| PARAMETER | SYMBOL | TEST CONDITIONS | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| Full-scale output signal | $V_{MAX}$ | Digital input level = 0dBFS | | 1.6×VDDA | | $V_{PP}$ |
| Signal to Noise Ratio | SNR | A-weighted | | 100 | | dB |
| Total Harmonic Distortion Plus Noise | THD+N | -1dBFS<br>44.1kHz slave mode | | -90 | | dB |
| | | -1dBFS<br>32kHz PLL mode | | -80 | | dB |
| Channel separation | | | | 90 | | dB |
| Pass band | $B_{PASS}$ | | | | 0.45×Fs | kHz |
| Stop band | $B_{STOP}$ | Fs ≤ 48kHz<br>Fs = 88.2/96kHz | 0.56×Fs | | 7×Fs<br>3.5×Fs | kHz |
| Pass band Ripple | | Voice mode<br>Music mode | | | ±0.15<br>±0.1 | dB |
| Stop band Attenuation | | Voice mode<br>Music mode | 70<br>55 | | | dB |
| Group delay | | Voice mode<br>Music mode<br>Fs = 88.2/96kHz | | 4.8/Fs<br>18.5/Fs<br>9/Fs | 650 | µs |
| Group delay variation | | 20Hz to 20kHz | | | 1 | µs |
| Group delay mismatch | | Between left and right channels | | | 2 | µs |
| Power Supply Rejection Ratio | PSRR with respect to VDDA | 20Hz to 2kHz<br>20kHz | 70<br>50 | | | dB |



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**Class AB Lineout Amplifier / Speaker Driver**

| From DAC_L/DAC_R to (SP_P, SP_N) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **Min** | **Typ** | **Max** | **UNIT** |
| Full-scale output signal | $V_{MAX}$ | No load | | 1.8×VDD_SP | | $V_{PP}$ |
| Maximum output power | $P_{MAX}$ | VDD_SP = 1.2V<br>THD < 10%<br>$R_{LOAD}$ = 8Ω, 1kHz | | 65 | | $mW_{RMS}$ |
| | | VDD_SP = 1.5V<br>THD < 10%<br>$R_{LOAD}$ = 8Ω, 1kHz | | 115 | | $mW_{RMS}$ |
| | | VDD_SP = 3.7V<br>THD < 10%<br>$R_{LOAD}$ = 8Ω, 1kHz | | 745 | | $mW_{RMS}$ |
| | | VDD_SP = 5.0V<br>THD < 10%<br>$R_{LOAD}$ = 8Ω, 1kHz | | 1200 | | $mW_{RMS}$ |
| Load impedance | $R_{LOAD}$ | | 6.4 | 8 | <br>1<br>200 | Ω<br>µH<br>pF |
| Frequency response | | ±0.5dB | 20 | | 20k | Hz |
| Amplitude ripple | | 20Hz to 20kHz | -0.5 | | 0.5 | dB |
| Programmable gain | | | -48 | | +15 | dB |
| Mute attenuation | | | | 100 | | dB |
| Programmable gain step size | | | | 1 | | dB |
| Absolute gain accuracy | | 0dB @ 1kHz | -0.8 | | +0.8 | dB |
| Gain step error | | 20Hz to 20kHz | -0.1 | | +0.1 | dB |
| Signal to noise ratio | SNR | A-weighted<br>gain = 0dB<br>VDD_SP = 1.6V | | 96.5 | | dB |
| Output Noise Level | $V_{NOISE}$ | Non A-weighted<br>Gain ≤ -15dB<br>20Hz to 20kHz | | 6 | | µV |
| Total Harmonic Distortion Plus Noise | THD+N | VDD_SP = 1.6V<br>-1dBFS<br>44.1kHz slave mode<br>$R_{LOAD}$ > 2kΩ | | -86 | | dB |
| | | VDD_SP = 1.6V<br>-1dBFS<br>32kHz PLL mode<br>$R_{LOAD}$ > 2kΩ | | -80 | | dB |
| Power Supply Rejection Ratio | PSRR with respect to VDD_SP | 20Hz to 2kHz<br>20kHz | 90<br>70 | | | dB |



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**True Ground Charge Pump**

| HPCSP and HPCSN | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **Min** | **Typ** | **Max** | **UNIT** |
| Positive rail output | VDDCSP | CP_MOD = 11<br>CP_MOD = 10 | | VDD_A<br>VDD_A / 2 | | V |
| Negative rail output | VDDCSN | CP_MOD = 11<br>CP_MOD = 10 | | -VDD_A<br>-(VDD_A / 2) | | V |
| Flyback capacitor | | One capacitor | | 1.0 | | µF |
| Reservoir capacitors | | Two capacitors | | 1.0 | | µF |

**True Ground Headphone Amplifier**

| From DAC_L/DAC_R to (HP_L/HP_R) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **Min** | **Typ** | **Max** | **UNIT** |
| Full-scale Output Signal | $V_{MAX}$ | No load | | 1.6×VDD_A | | $V_{PP}$ |
| DC output offset | | HP Gain < -30dB | | | 100 | µV |
| Maximum power per channel | $P_{MAX}$ | VDD_A = 1.6V<br>THD < 0.1%<br>$R_{LOAD}$=16Ω, 1kHz | | L = 23<br>R = 23 | | $mW_{RMS}$ |
| | | VDD_A = 1.8V<br>THD < 0.1%<br>$R_{LOAD}$=16Ω, 1kHz | | L = 29<br>R = 29 | | $mW_{RMS}$ |
| | | VDD_A = 2.5V<br>THD < 0.1%<br>$R_{LOAD}$=16Ω, 1kHz | | L = 67<br>R = 67 | | $mW_{RMS}$ |
| Load Impedance | $R_{LOAD}$<br>$L_{LOAD}$<br>$C_{LOAD}$ | | 13 | 16 | <br>400<br>500 | Ω<br>µH<br>pF |
| Frequency Response | | ±0.5dB | 20 | | 20k | Hz |
| Amplitude Ripple | | 20Hz to 20kHz | -0.5 | | +0.5 | dB |
| Programmable Gain | | | -56 | | +6 | dB |
| Mute Attenuation | | | | 70 | | dB |
| Programmable Gain Step Size | | | | 1.0 | | dB |
| Absolute Gain Accuracy | | 0dB @ 1kHz | -0.8 | | +0.8 | dB |
| Input Gain L/R-Mismatch | | 20Hz to 20kHz | -0.1 | | +0.1 | dB |
| Input Gain Step Error | | 20Hz to 20kHz | -0.1 | | +0.1 | dB |
| Signal to Noise Ratio | SNR | A-weighted<br>gain = 0dB<br>VDD_A = 2.5V<br>VDD_A = 1.8V | | <br>100<br>98 | | dB |



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| | | | | | | |
|---|---|---|---|---|---|---|
| Output Noise Level | $V_{NOISE}$ | 20 to 20kHz,<br>non A-weighted<br>gain < -20dB | | | *2.5* | *uVrms* |
| Total Harmonic Distortion Plus Noise | THD+N | VDD_A = 1.6V<br>-5dBFS<br>$R_{LOAD}$=16Ω | | -87 | | dB |
| Power Supply Rejection Ratio | PSRR with respect to VDD_A | 20Hz to 2kHz<br>20kHz | 70<br>50 | | | dB |

## Clock Generation

### MCLK Input

| PARAMETER | SYMBOL | TEST CONDITIONS | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| Input Amplitude | | MCLK squarer enabled<br>MCLK squarer disabled | 0.3<br>0.9×VDD_IO | | VDD_IO<br>VDD_IO | V |
| Input Impedance | | DC impedance > 10 MΩ | 300<br>0.5 | 1 | 2 | Ω<br>pF |
| MCLK rise time | | | | | 8ns | |

## Phase Locked Loop (PLL)

### PLL Mode

| PARAMETER | SYMBOL | TEST CONDITIONS | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| MCLK Input Jitter | $J_C$<br>$J_A$ | Cycle jitter (rms)<br>Absolute jitter (rms) | | | 50<br>100 | ps<br>ps |
| Input frequency | $F_{IN}$ | Normal mode<br>32kHz mode | 5 | 32.768 | 50 | MHz<br>kHz |
| SRM Tracking Range | | DAI slave mode<br>WCLK frequency variation | -4 | | 4 | % |
| SRM Tracking Rate | | DAI slave mode<br>WCLK drift rate | | | 50 | ppm/s |

### Bypass Mode

| PARAMETER | SYMBOL | TEST CONDITIONS | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| Input Jitter | $J_C$<br>$J_A$ | Cycle jitter (rms)<br>Absolute jitter (rms) | | | TBD<br>TBD | ps<br>ps |
| Input frequency | $F_{IN}$ | Sample frequency:<br>11.025, 22.05, 44.1, 88.2kHz<br>8, 12, 16, 24, 32, 48, 96kHz | | 11.2896<br>12.288 | | MHz |



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## SIGNALS AND PACKAGING

### Pad Description

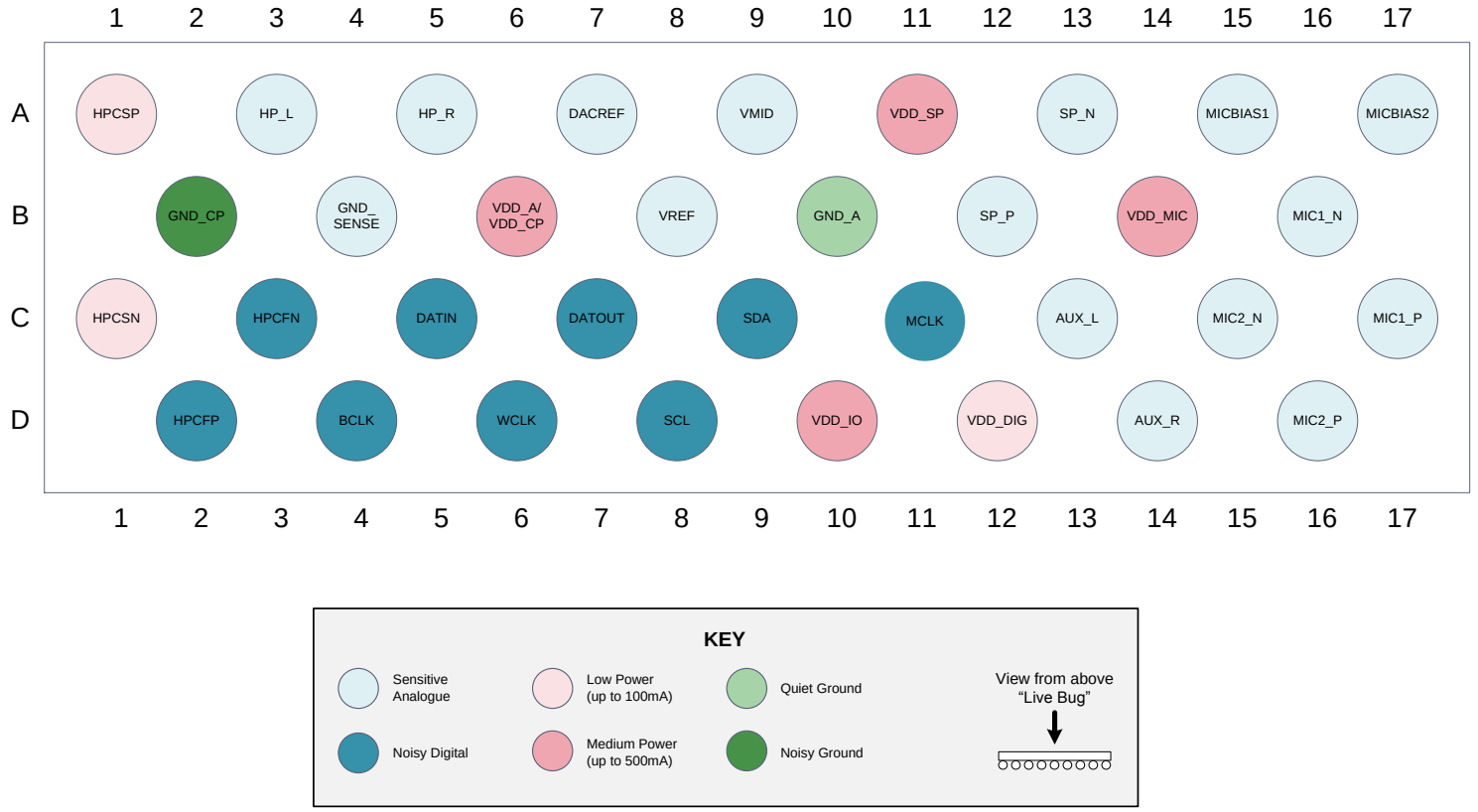


***Figure 2: DA7213 ball layout***



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## Pin Descriptions

| PIN NAME | BUMP / PIN | FUNCTION | ALTERNATE FUNCTION | CLASS |
|---|---|---|---|---|
| **Audio Inputs** | | | | |
| MIC1_P | C17 | Differential mic. input 1 (pos) / Single-ended mic. input 1 (left) | Digital mic. clock (DMICCLK) | AI/DO |
| MIC1_N | B16 | Differential mic. input 1 (neg) / Single-ended mic. input 2 (left) | Digital Mic. data (DMICIN) | AI/DI |
| MIC2_P | D16 | Differential mic. input 2 (pos) / Single-ended mic. input 1 (right) | | AI |
| MIC2_N | C15 | Differential mic. input 2 (neg) / Single-ended mic. input 2 (right) | | AI |
| AUX_L | C13 | Single-ended auxiliary input left | | AI |
| AUX_R | D14 | Single-ended auxiliary input right | | AI |
| MICBIAS1 | A15 | Microphone bias output 1 | | AO |
| MICBIAS2 | A17 | Microphone bias output 2 | | AO |
| **Audio Outputs** | | | | |
| HP_L | A3 | True-ground headphone output left | | AO |
| HP_R | A5 | True-ground headphone output right | | AO |
| SP_P | B12 | Differential speaker output (pos) | | AO |
| SP_N | A13 | Differential speaker output (neg) | | AO |
| **Audio Chargepump** | | | | |
| HPCSP | A1 | Chargepump reservoir capacitor (pos) | | AIO |
| HPCSN | C1 | Chargepump reservoir capacitor (neg) | | AIO |
| HPCFP | D2 | Chargepump flyback capacitor (pos) | | AIO |
| HPCFN | C3 | Chargepump flyback capacitor (neg) | | AIO |
| **Digital Interfaces** | | | | |
| SDA | C9 | I2C bidirectional data | | DIO |
| SCL | D8 | I2C clock input | | DI |
| DATIN | C5 | DAI data input | | DIO |
| DATOUT | C7 | DAI data output | | DIO |
| BCLK | D4 | DAI bit clock | | DIO |
| WCLK | D6 | DAI word clock (L/R select) | | DIO |
| MCLK | C11 | Master clock | | DI |
| **References** | | | | |
| DACREF | A7 | Audio DAC reference capacitor | | AIO |
| VMID | A9 | Audio mid-rail reference capacitor | | AIO |
| GND_SENSE | B4 | Ground reference for headphone output | | AI |
| VREF | B8 | Bandgap reference capacitor | | AIO |
| **Supplies** | | | | |
| VDD_A | B6 | Supply for analogue circuits / headphone charge pump | | PS |
| VDD_IO | D10 | Supply for digital interfaces | | PS |
| VDD_SP | A11 | Supply for speaker driver | | PS |
| VDD_MIC | B14 | Supply for microphone bias circuits | | PS |
| VDIG | D12 | | | PS |
| **Grounds** | | | | |
| GND_A | B10 | Analogue ground | | PG |
| GND_CP | B2 | Chargepump/digital ground | | PG |



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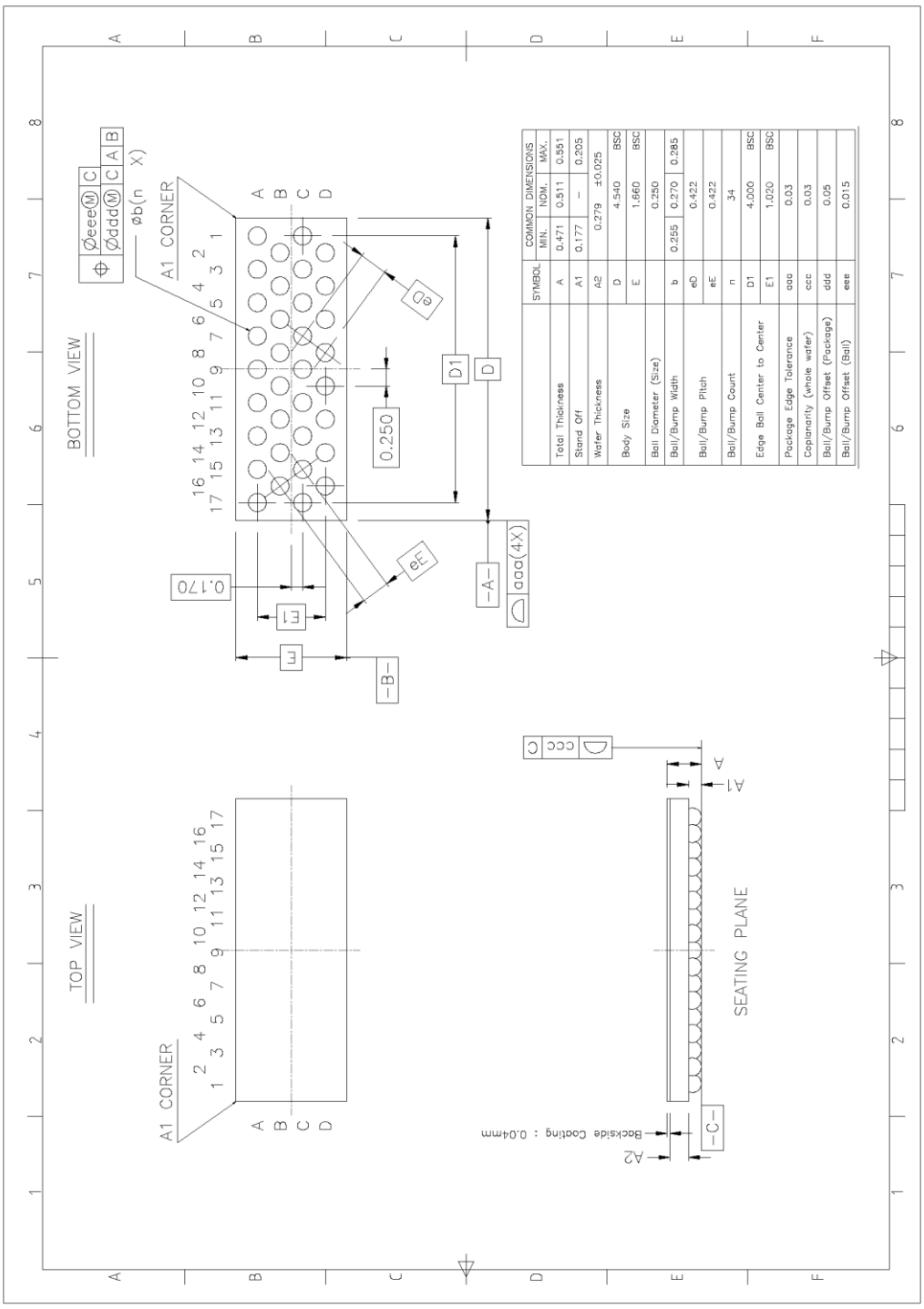
# PACKAGE

## Package Physical Dimensions



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## ORDERING INFORMATION

| Part Number | Package | Shipment Form | Pack quantity |
|---|---|---|---|
| DA7212-00UM2 | 34-bump CSP Pb-free/green | T & R | 4500 |

## Data Sheet Status Definitions

The Data Sheet version consists of two characters, a numeral followed by a lower-case alphabetic character. The numeral indicates Product Status (see table below), and the alphabetic character indicates the document revision level.
Notes:

| Version | Data Sheet Status | Product Status | Definition |
|---|---|---|---|
| 1a – 1z | Draft | Development | Version 1 Data Sheets contain pre-tapeout information from the objective design specification.<br>Dialog reserves the right to change the specification in any manner without notice |
| 2a – 2z | Preliminary | Qualification | Version 2 data sheets contain information on post-tapeout and pre-volume production products.<br>Dialog reserves the right to change the specification in any manner without notice, in order to supply the best possible product by improvements to the design. Relevant changes will be communicated via Dialog's Sales and Marketing departments |
| 3a – 3z | Released | Production | Version 3 Data Sheets contain information on volume production products.<br>Dialog reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notification |

1. To avoid confusion, the following alphabetic characters shall not be used in document version references: **i, j, l, o**.
2. Please consult the latest issued version of the data sheet before initiating or completing a design.
3. The product status of the device may have changed since this data sheet was published.

Please contact Dialog for the latest information.www.dialog-semiconductor.com
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