



The Future of Analog IC Technology®

MP8859

2.8 - 22V V_{IN} , 3A I_{OUT} , 4-Switch,
Integrated Buck-Boost Converter
with I²C Interface

DESCRIPTION

The MP8859 is a synchronous, 4-switch, integrated buck-boost converter capable of regulating the output voltage from a 2.8V to 22V wide input voltage range with high efficiency. The integrated output voltage scaling and adjustable output current limit functions meet the USB power delivery (PD) requirement.

The MP8859 uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MP8859 provides auto PFM/PWM or forced PWM switching modes, programmable output constant current (CC) current limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), programmable soft start, and thermal shutdown.

The MP8859 is available in a 16-pin QFN (3mmx3mm) package.

FEATURES

- Wide 2.8V to 22V Operating Input Voltage Range
- 1V ⁽¹⁾ to 20.47V Output Voltage Range (5V Default) with 10mV Resolution through I²C
- 3A Output Current or 4A Input Current
- Four Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- Adjustable Accurate CC Output Current Limit with Internal Sensing MOSFET via I²C
- 500kHz Switching Frequency
- Output Over-Voltage Protection (OVP) Hiccup
- Output Short-Circuit Protection (SCP) with Hiccup
- Over-Temperature Warning and Shutdown
- I²C Interface with ALT Pin
- Four Programmable I²C Addresses
- One-Time Programmable (OTP) Non-Volatile Memory
- I²C Programmable Line Drop Compensation, PFM/PWM Mode, Soft Start, OCP, etc.
- EN Shutdown Discharge Programmable
- Available in a QFN-16 (3mmx3mm) Package
- UL Certified, UL2367: E322138
UL60950-1/ UL60950-1-07: E500002-A1-CB-1

APPLICATIONS

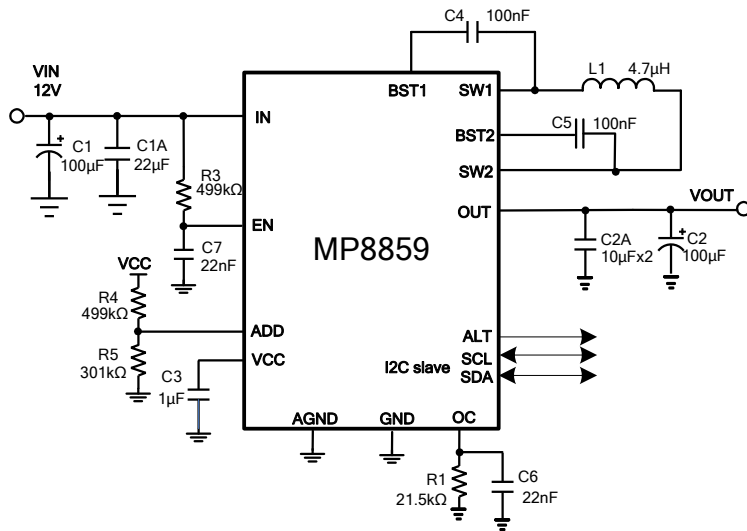
- USB PD Sourcing Ports
- Buck-Boost Bus Supplies

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

NOTE:

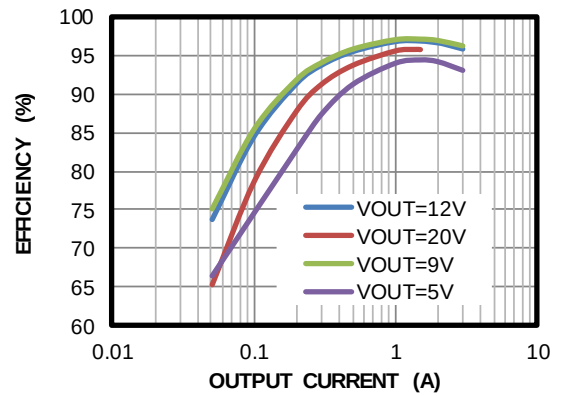
- 1) For $V_{OUT} < 3V$ applications, the switching frequency decreases.

TYPICAL APPLICATION



Efficiency vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5 - 20V$, Forced PWM Mode



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8859GQ-xxxx**	QFN-16 (3mmx3mm)	See Below
MP8859GQ-0000	QFN-16 (3mmx3mm)	See Below
EVKT-8859	Evaluation Kit	

* For Tape & Reel, add suffix -Z (e.g.: MP8859GQ-XXXX-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. The default number is “0000”. Each “x” can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number, even if ordering the “0000” code. MP8859GQ-0000 is the default version.

TOP MARKING

BGRY

LLL

BGR: Product code of MP8859GQ

Y: Year code

LLL: Lot number

EVALUATION KIT EVKT-8859

EVKT-8859 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV8859-Q-00B	MP8859GQ-0000 evaluation board	1
2	EVKT-USB I2C-02	Includes one USB to I2C communication interface device, one USB cable, and one ribbon cable	1
3	Tdrive-8859	USB thumb drive that stores the GUI installation file and supplemental documents	1

Order direct from MonolithicPower.com or our distributors.

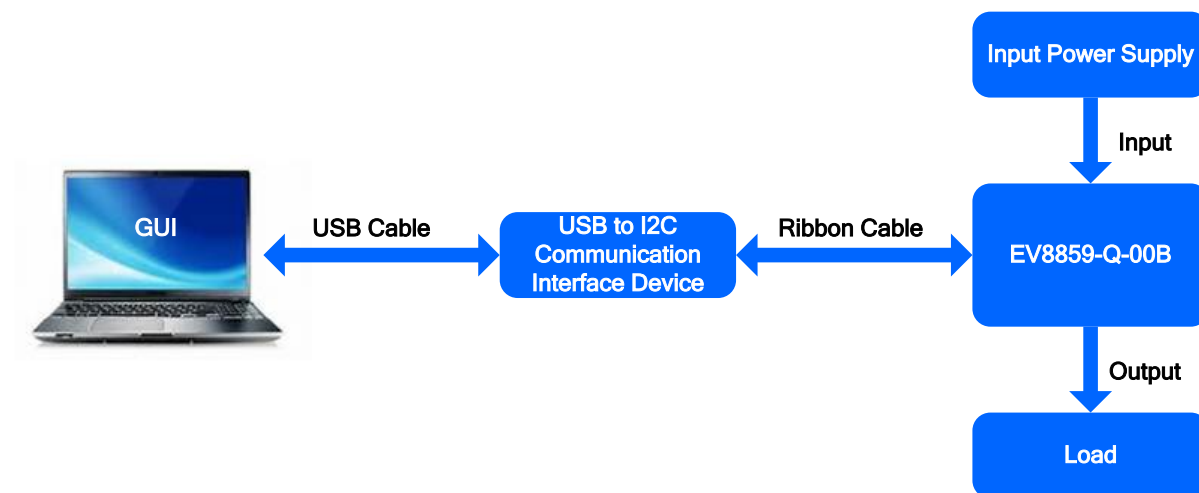
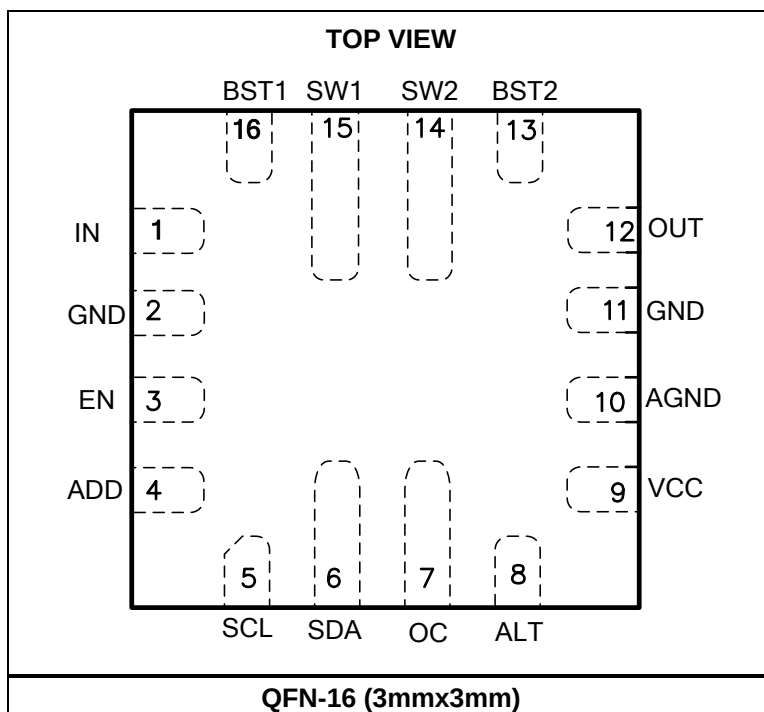


Figure 1: EVKT-8859 Evaluation Kit Set-Up

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽²⁾

Supply voltage (V_{IN} , V_{OUT})	24V
V_{SW1} , $SW2$	-0.3V (-7V for <10ns) to $V_{IN} + 0.3V$ (26V for <10ns)
V_{BST1} , $BST2$	$V_{SWx} + 4V$
V_{EN}	-0.3V to 24V
V_{ALT}	-0.3V to +5.5V
All other pins	-0.3V to +4V
Continuous power dissipation ($T_A = +25^\circ C$) ⁽³⁾⁽⁵⁾	4.8W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽⁴⁾

Operation input voltage range	2.8V to 22V
Output voltage range	1V to 20.47V
Output current	3A continuous current or 4A input current
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance

 θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)

EV8859-Q-00B ⁽⁵⁾	26.....	3.... °C/W
JESD51-7 ⁽⁶⁾	50.....	12... °C/W

NOTES:

- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on EV8859-Q-00B, 4-layer PCB, 64mmx64mm.
- 6) Measured on JESD51-7, 4-layer PCB.

OTP E-Fuse Selection Table by Default (MP8859GQ-0000)

OTP Items	Default Value
Output voltage	5V
IOUT_LIMIT	3.5A (For 21.5k Ω OC resistor)
Switching frequency	500kHz
Mode	Forced PWM mode
Soft start time	900 μ s
Line drop compensation	V_{OUT} compensates 150mV@3A I_{OUT}
Output voltage discharge mode	Enabled
OCP_OVP protection mode	Hiccup
OTP configure code (ID1)	0x00

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C ⁽⁷⁾, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I _{IN}	V _{EN} = 0V		0	3	μA
Supply current (quiescent)	I _Q	Non-switching, I ² C sets PFM mode		1		mA
EN rising threshold	V _{EN_Rising}		1.04	1.10	1.16	V
EN hysteresis	V _{EN_Falling}		65	110	160	mV
EN to ground resistance	R _{EN}	V _{EN} = 2V		2		MΩ
EN on to V _{OUT} > 90% delay	T _{Delay}	See Figure 8.		900		μs
VCC regulator	V _{CC}		3.4	3.6	3.8	V
VCC load regulation	V _{CC_LOG}	I _{CC} = 10mA		1		%
V _{IN} under-voltage lockout threshold rising	V _{IN_UVLO}		2.50	2.65	2.79	V
V _{IN} under-voltage lockout threshold hysteresis	V _{UVLO_HYS}		115	160	205	mV
Power Converter						
HS switch on resistance	R _{DS(on)_HS}	Switch A, D		25	40	mΩ
LS switch on resistance	R _{DS(on)_LSB}	Switch B, C		21	35	mΩ
Output voltage	V _{OUT}		-1.5%	5.0	+1.5%	V
Output discharge resistance	R _{DIS}			60	100	Ω
Switch leakage	SW _{LKG}	V _{EN} = 0V, V _{SW1, SW2} = 22V, T _J = +25°C			1	μA
		V _{EN} = 0V, V _{SW1, SW2} = 22V, T _J = -40°C to +125°C			5	
Oscillator frequency	F _s		-20%	500	20%	kHz
Minimum on time ⁽⁸⁾	T _{ON_MIN1}	Switch A, B, C, D		160		ns
Maximum duty cycle	D _{MAX}	Buck mode, FREQ = 500kHz		85		%
Minimum duty cycle	D _{MIN}	Boost mode, FREQ = 500kHz		15		%
Protection						
Output over-voltage protection	V _{OVP_R}		150	160	170	%
Output OVP recovery	V _{OVP_F}		130	140	150	%
Low-side B valley limit	I _{LIMIT2}	Switch B	6	8	10	A
Low-side C peak current limit	I _{LIMIT3}	Switch C		10		A
Output average current	I _{OUT_LIM1}	V _{OUT} = 5V, over 0-125°C temp range	0.85	1	1.15	A
	I _{OUT_LIM2}	V _{OUT} = 5V, over 0-125°C temp range	-5%	3.5	+5%	A
Output UV threshold	V _{UVP}	20μs deglitch, UV falling	45%	50%	55%	V _{REF}

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C ⁽⁷⁾, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ALT sink current capability	ALT _{LOW}	Sink 4mA		0.2	0.4	V
ALT leakage	ALT _{LKG}	V _{PULL} = 5V			1	μA
Thermal shutdown rising threshold ⁽⁸⁾	T _{STD}			150		°C
Thermal hysteresis ⁽⁸⁾	T _{STD_HYS}			20		°C
I²C Specification						
ADD voltage threshold 1	V _{ADD_1}	ADD pin float		60H		
ADD voltage threshold 2	V _{ADD_2}	R4 = 499kΩ, R5 = 301kΩ		62H		
ADD voltage threshold 3	V _{ADD_3}	R4 = 301kΩ, R5 = 499kΩ		64H		
ADD voltage threshold 4	V _{ADD_4}	R4 = 100kΩ		66H		
ADD to GND pull-down resistor	R _{ADD}			2		MΩ
Input logic high	V _{IH}	I ² C pull-up VDD can be 1.8V to 5V	1.4			V
Input logic low	V _{IL}				0.4	V
Output voltage logic low	V _{OUT_L}				0.4	V
SCL clock frequency	f _{SCL}			400	3400	kHz
SCL high time	t _{HIGH}		60			ns
SCL low time	t _{LOW}		160			ns
Data set-up time	t _{SU.DAT}		10			ns
Data hold time	t _{HD.DAT}		0	60		ns
Set-up time for (repeated) start condition	t _{SU.STA}		160			ns
Hold time for (repeated) start condition	t _{HD.STA}		160			ns
Bus free time between a start and a stop condition	t _{BUF}		160			ns
Set-up time for stop condition	T _{SU.STO}		160			ns
Rise time of SCL and SDA	t _R		10		300	ns
Fall time of SCL and SDA	t _F		10		300	ns
Pulse width of suppressed spike	t _{SP}		0		50	ns
Capacitance for each bus line	C _B				400	pF

NOTES:

7) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.

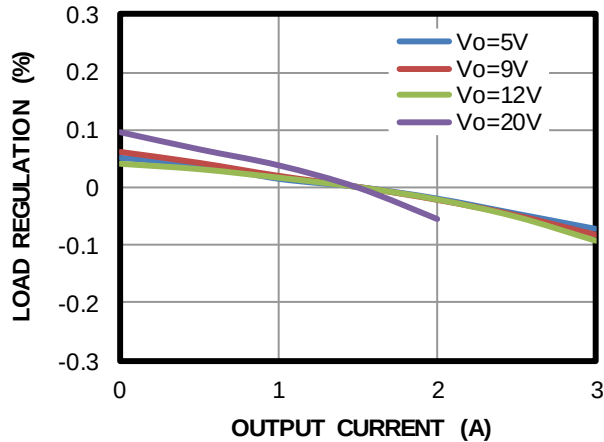
8) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

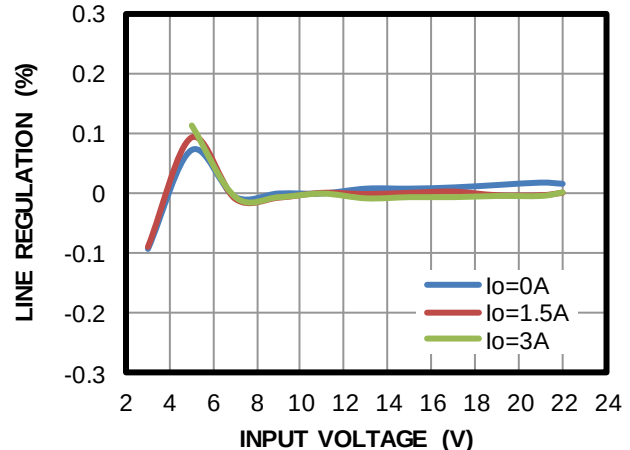
Load Regulation vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5V/9V/12V/20V$, $I_{OUT} = 0A$ to 3A, no line drop compensation



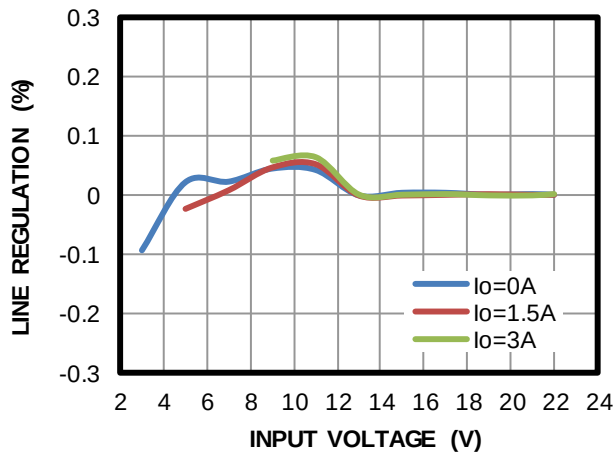
Line Regulation vs. Input Voltage

$V_{OUT} = 5V$



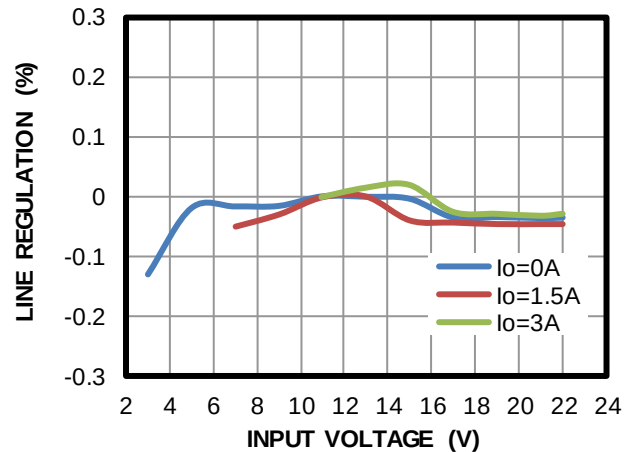
Line Regulation vs. Input Voltage

$V_{OUT} = 9V$



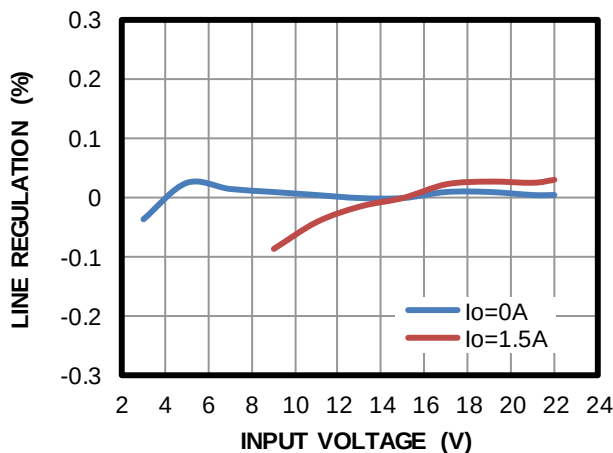
Line Regulation vs. Input Voltage

$V_{OUT} = 12V$



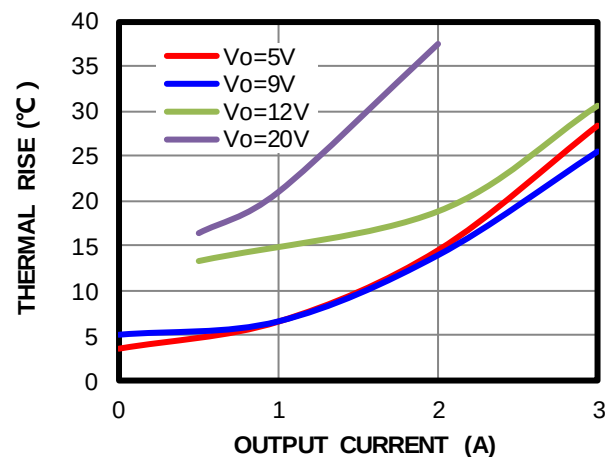
Line Regulation vs. Input Voltage

$V_{OUT} = 20V$



Thermal Rising vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5 - 20V$, $I_{OUT} = 0 - 3A$

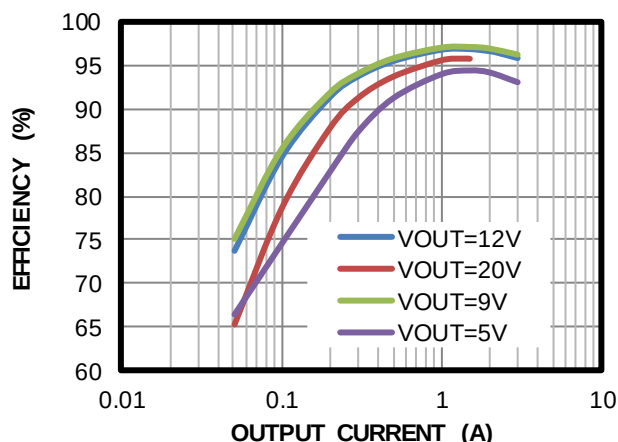


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

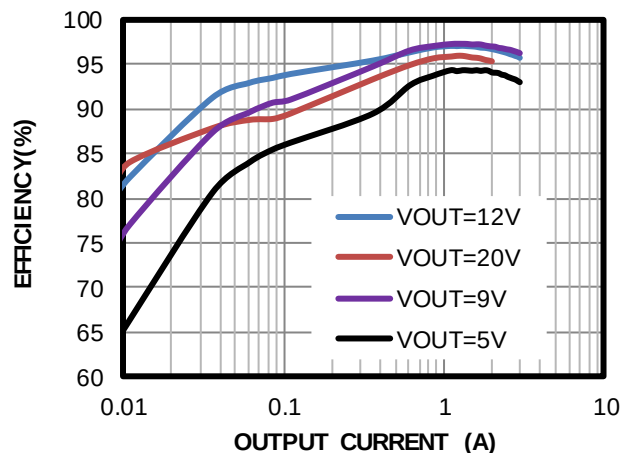
Efficiency vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5 - 20V$, forced PWM mode



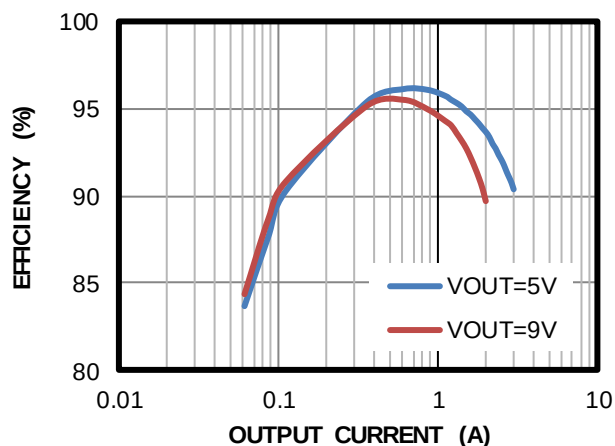
Efficiency vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5 - 20V$, auto PFM/PWM mode



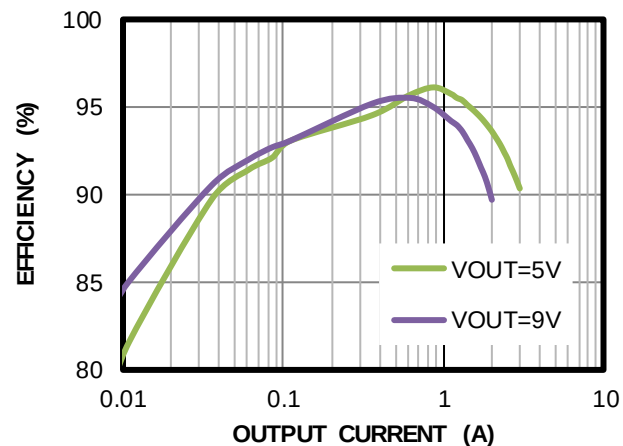
Efficiency vs. Output Current

$V_{IN} = 5V$, $V_{OUT} = 5V/9V$, forced PWM mode

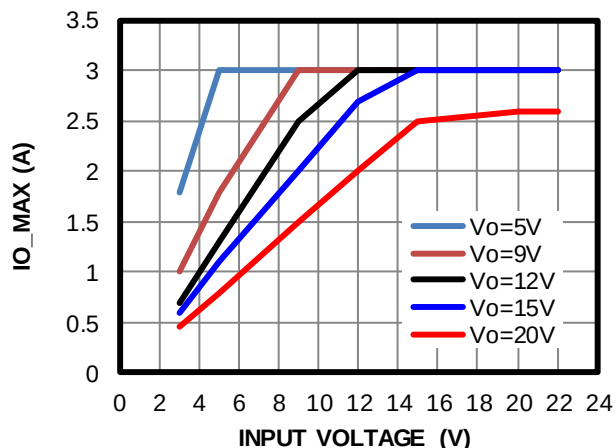


Efficiency vs. Output Current

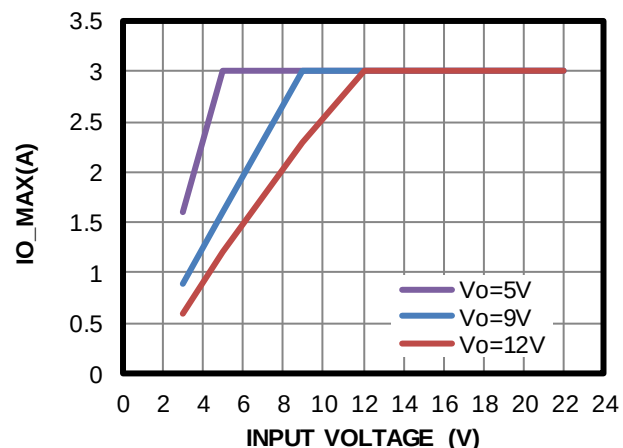
$V_{IN} = 5V$, $V_{OUT} = 5V/9V$, auto PFM/PWM mode



Recommended Maximum I_{OUT} vs. V_{IN} and V_{OUT} with 120 μF Low ESR C_{OUT} Capacitor



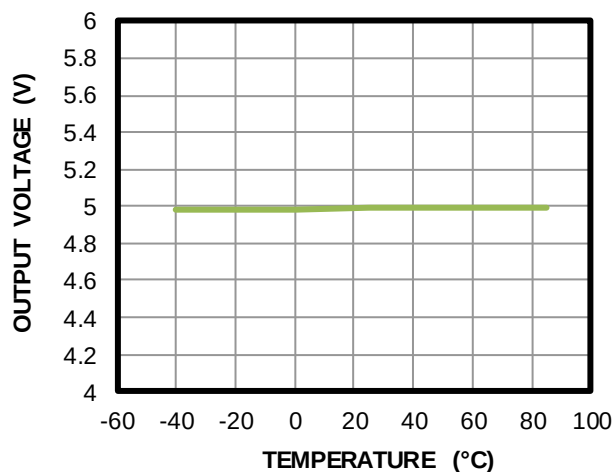
Recommended Maximum I_{OUT} vs. V_{IN} and V_{OUT} with 22 $\mu F \times 5$ Ceramic C_{OUT} Capacitor



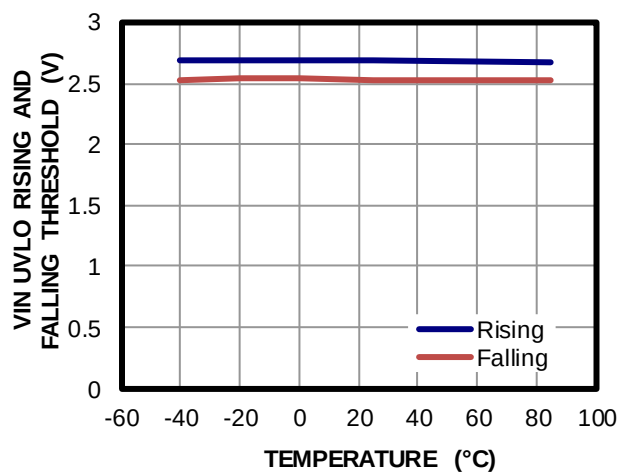
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

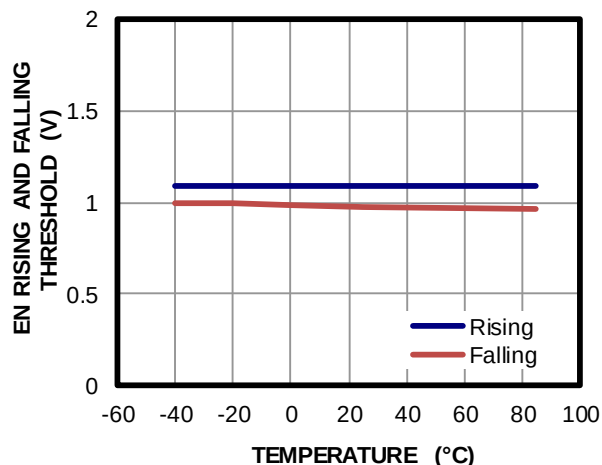
Output Voltage vs. Temperature



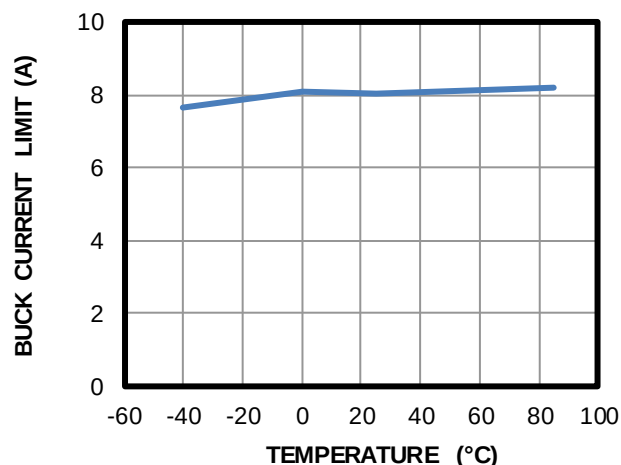
V_{IN} UVLO Rising and Falling Threshold vs. Temperature



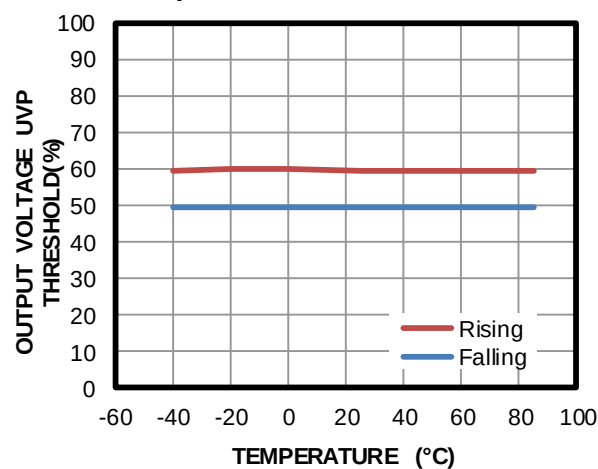
EN Rising and Falling Threshold vs. Temperature



Buck Valley Current Limit vs. Temperature

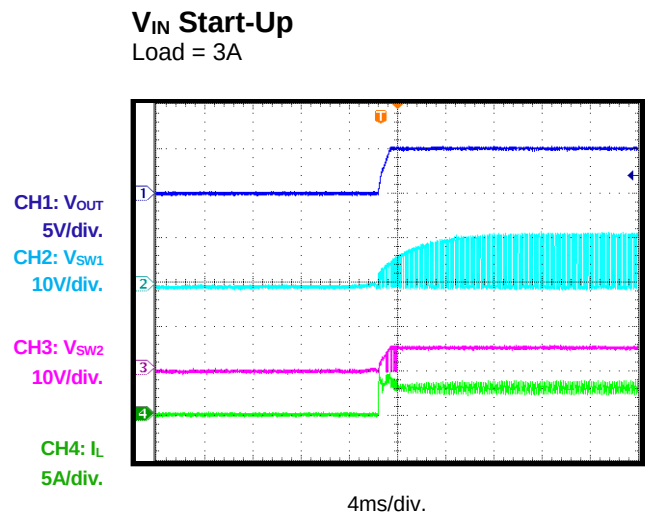
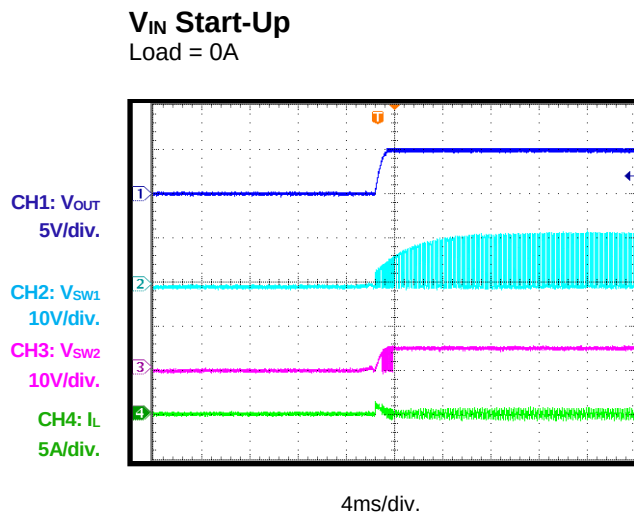
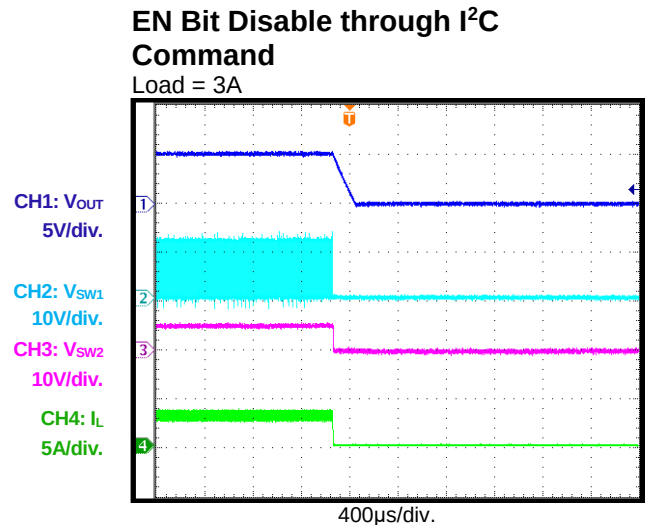
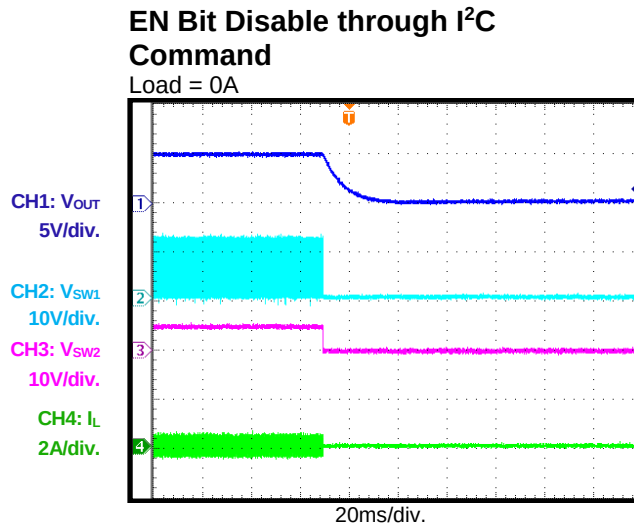
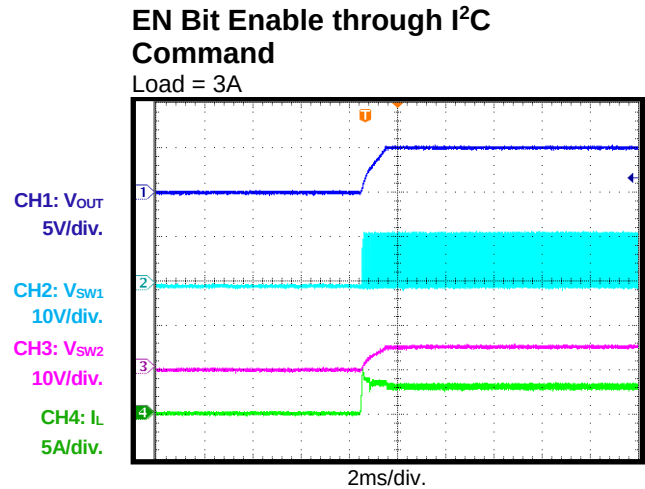
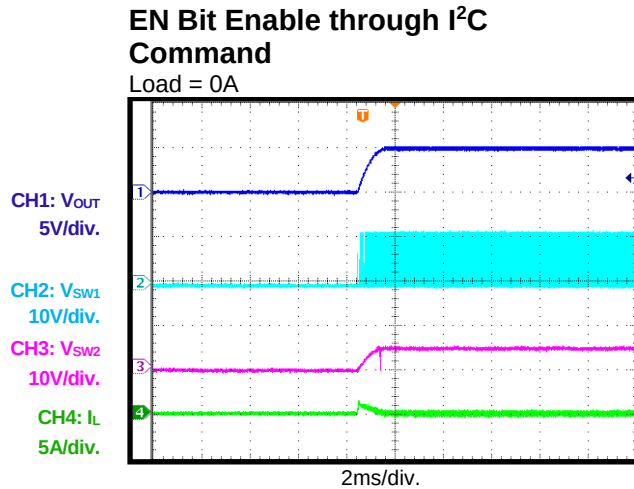


Output Voltage UVP Threshold vs. Temperature



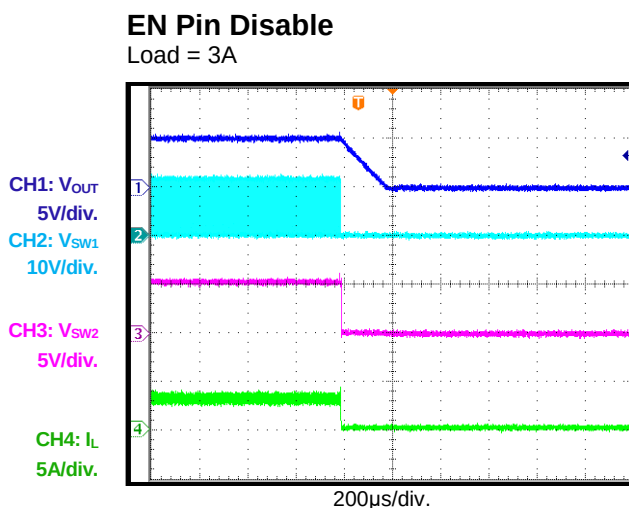
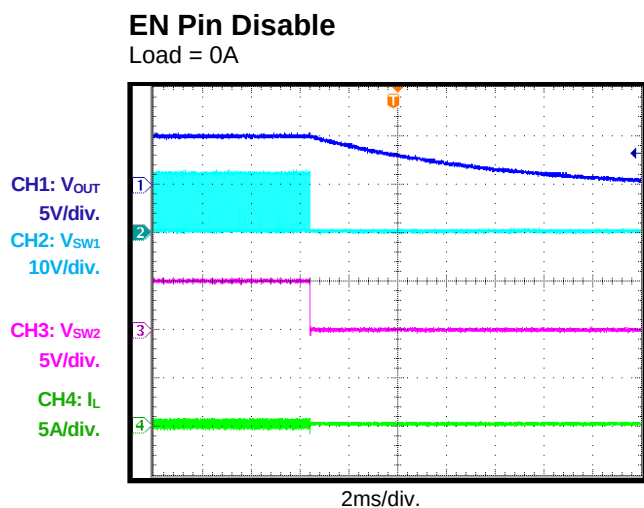
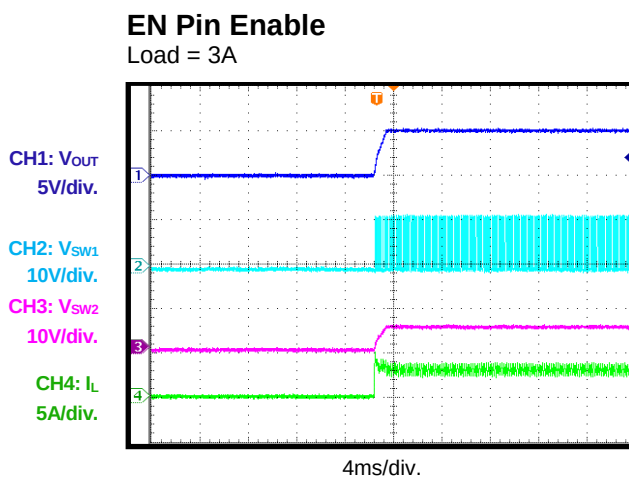
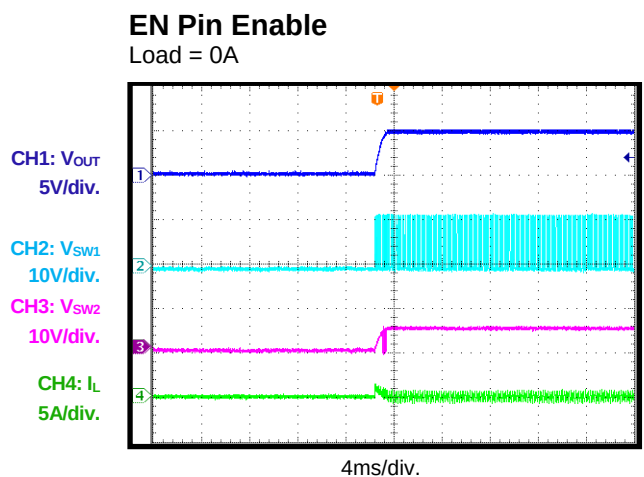
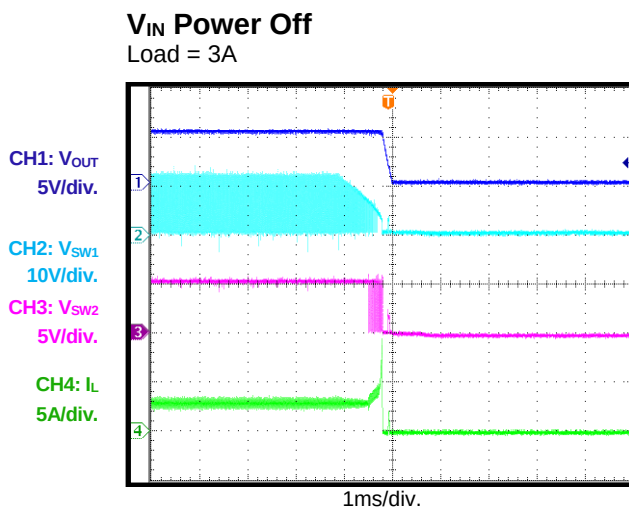
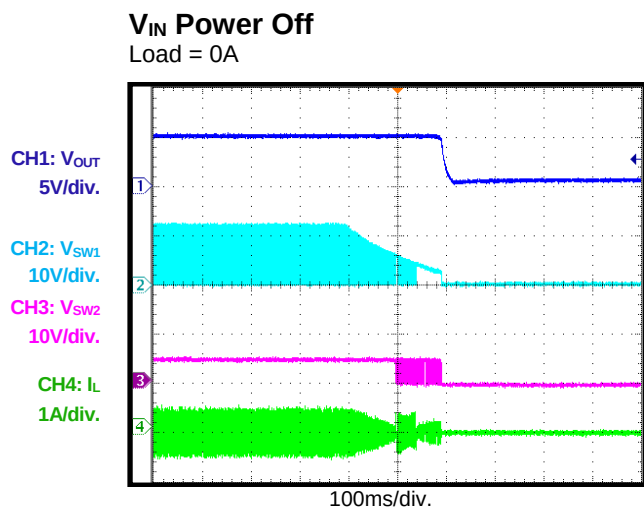
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

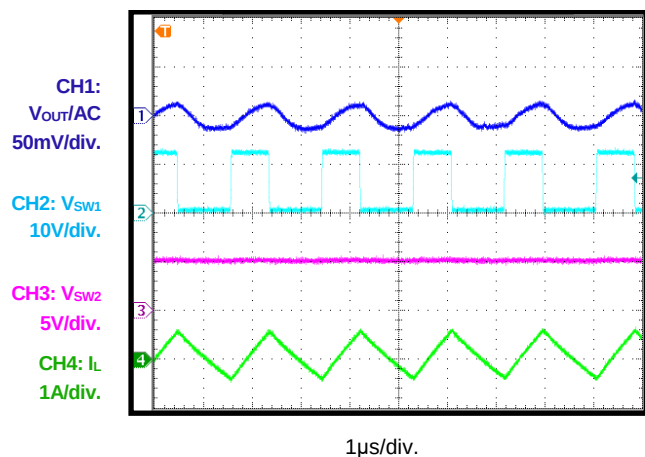


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

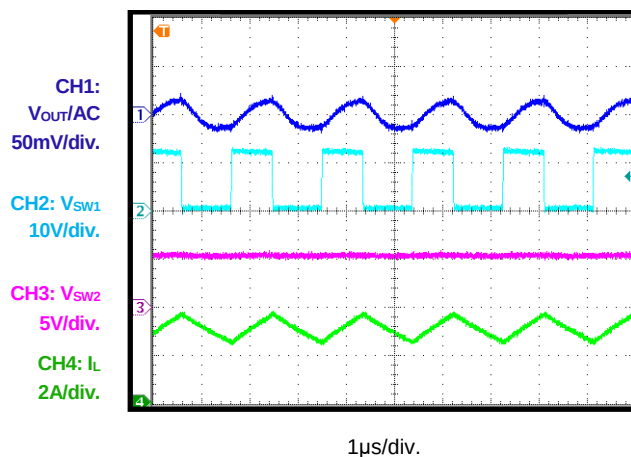
Steady State

$V_{OUT} = 5V$, load = 0A



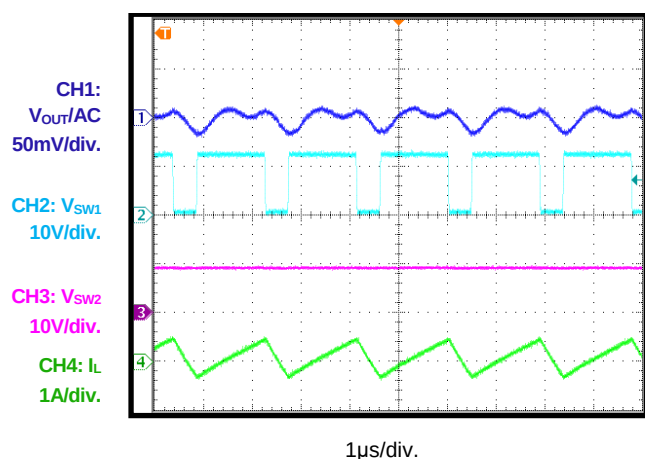
Steady State

$V_{OUT} = 5V$, load = 3A



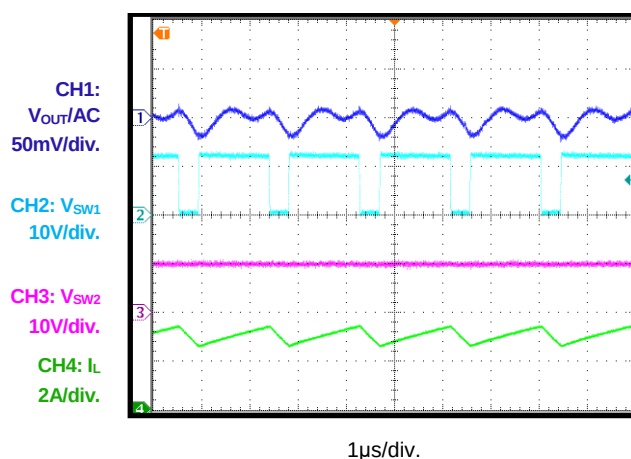
Steady State

$V_{OUT} = 9V$, load = 0A



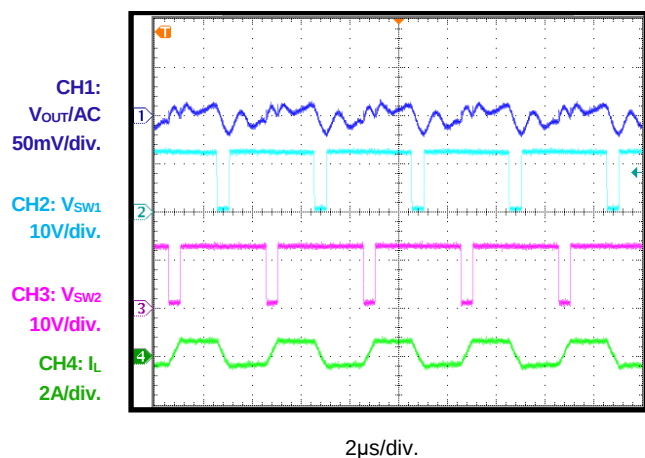
Steady State

$V_{OUT} = 9V$, load = 3A



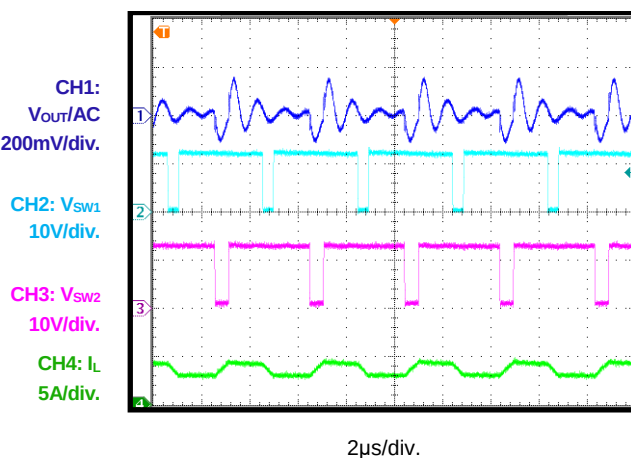
Steady State

$V_{OUT} = 12V$, load = 0A



Steady State

$V_{OUT} = 12V$, load = 3A

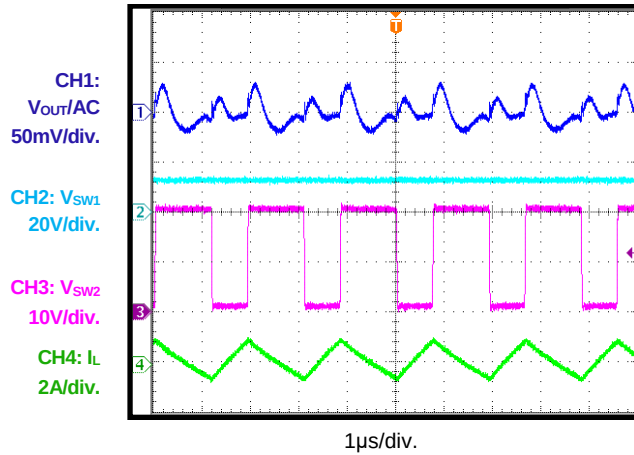


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

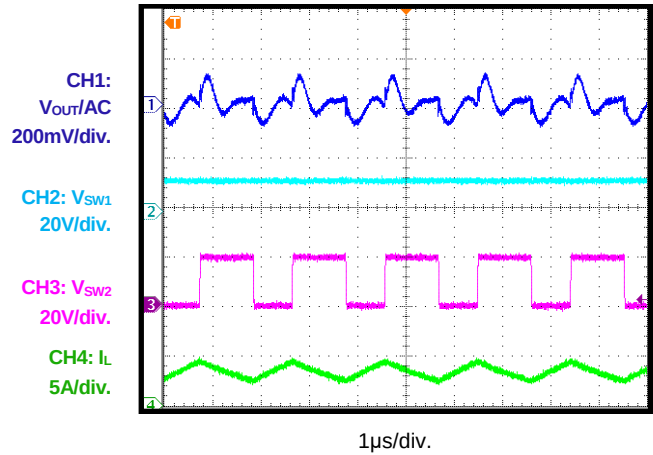
Steady State

$V_{OUT} = 20V$, load = 0A



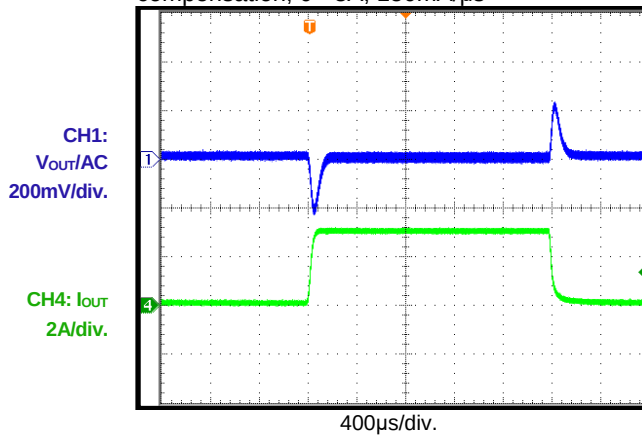
Steady State

$V_{OUT} = 20V$, load = 2A



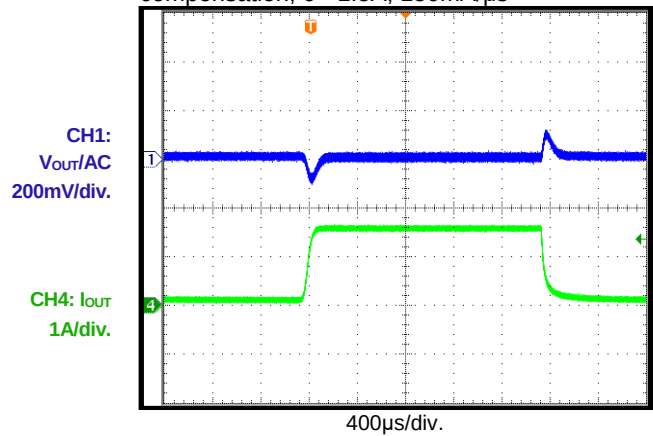
Load Transient

$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 0 - 3A, 150mA/µs



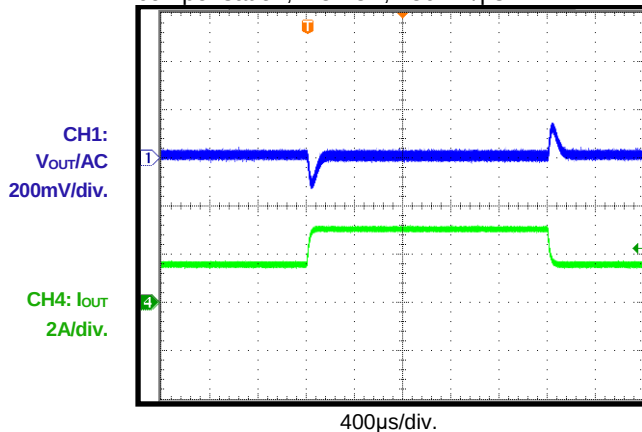
Load Transient

$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 0 - 1.5A, 150mA/µs

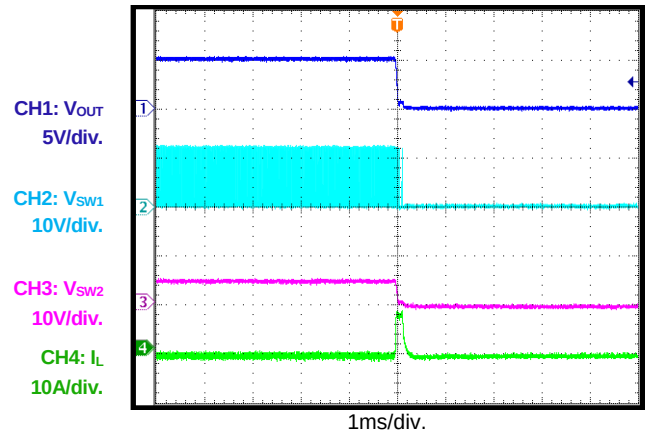


Load Transient

$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 1.5 - 3A, 150mA/µs



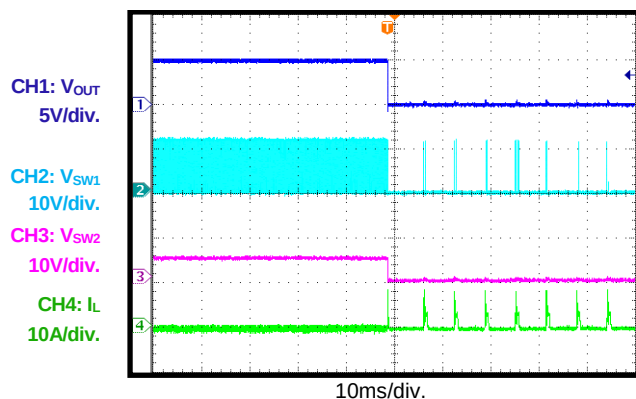
SCP Entry with Latch-Off Mode



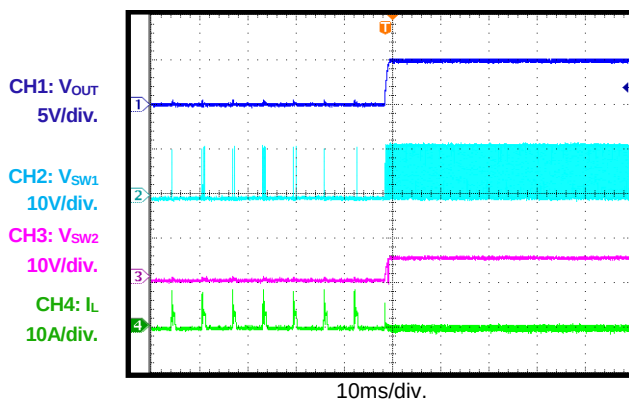
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

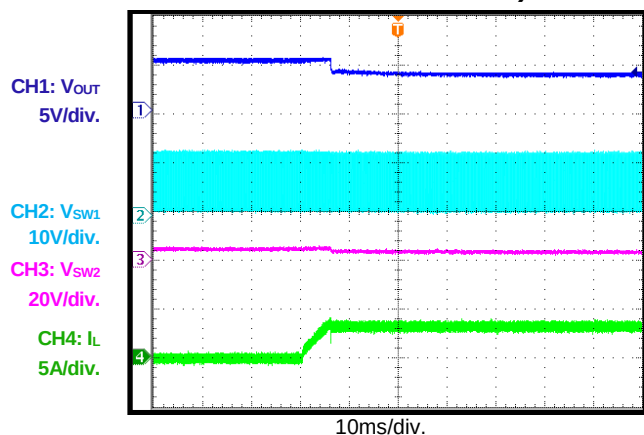
SCP Entry with Hiccup Mode



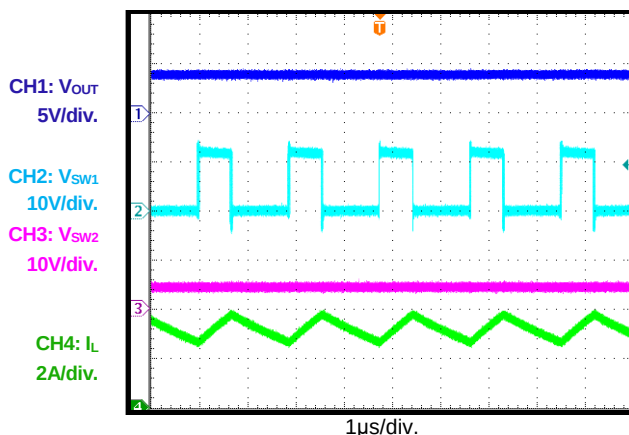
SCP Recovery with Hiccup Mode



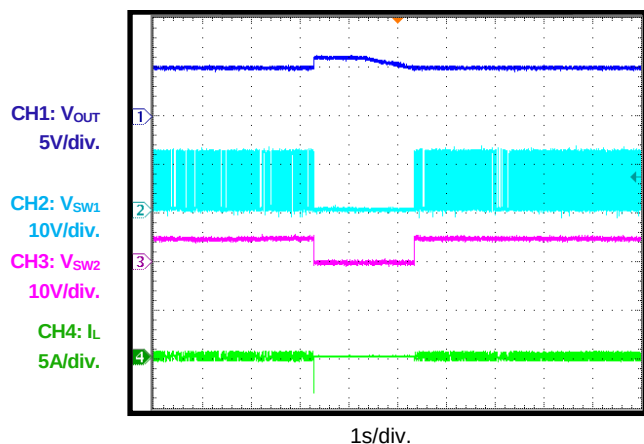
CC Current Limit Entry (Test with CV Mode of Electronic Load)



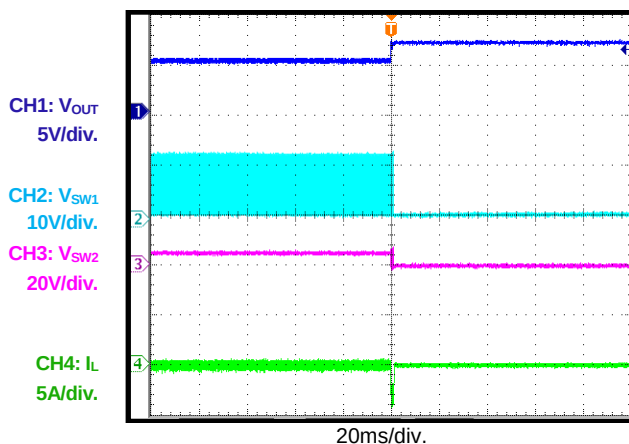
CC Current Limit Steady State



V_{OUT} OVP with Hiccup Mode

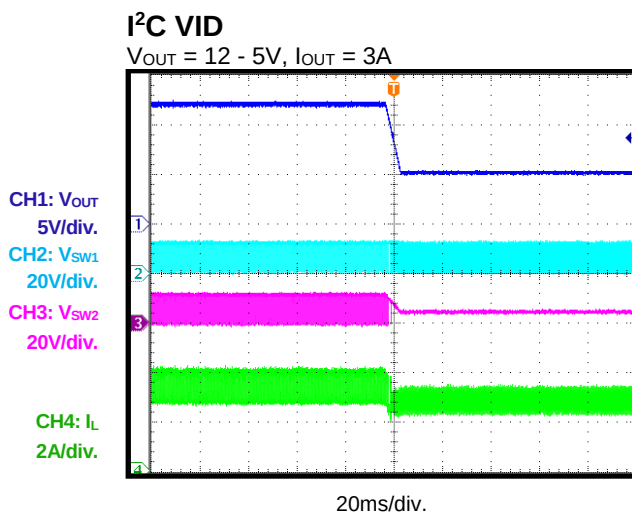
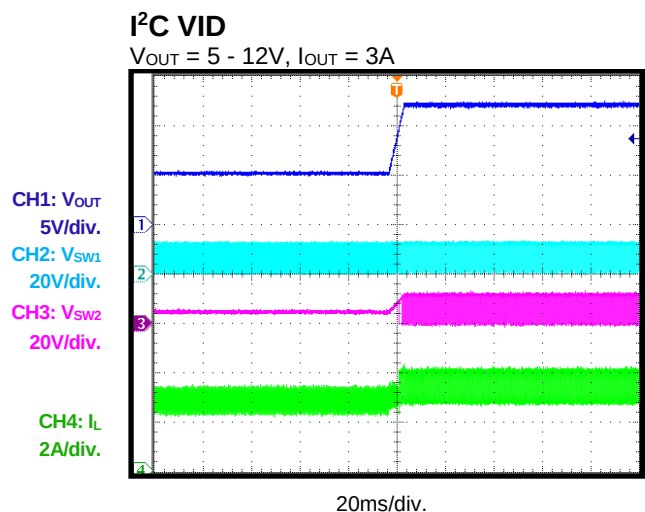
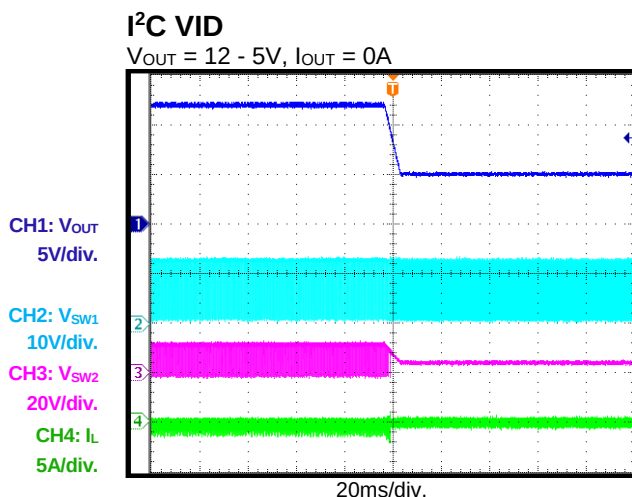
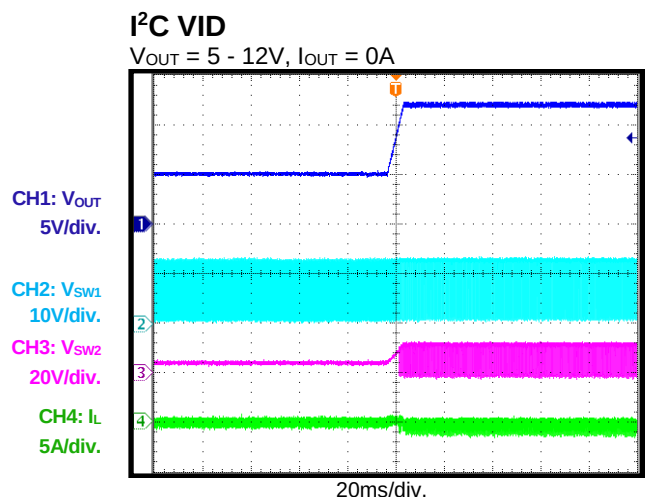


V_{OUT} OVP with Latch-Off Mode



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, Test waveform is based on Figure 12, unless otherwise noted.



PIN FUNCTIONS

QFN 3x3 Pin #	Name	Description
1	IN	Supply voltage. IN is the drain of the internal power device and provides power to the entire chip. The MP8859 operates from a 2.8V to 22V input voltage. A capacitor (C _{IN}) is required to prevent large voltage spikes from appearing at the input. Place C _{IN} as close to the IC as possible.
2, 11	GND	Power ground. GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND with copper traces and vias.
3	EN	On/off control for entire chip. Drive EN high to turn on the chip. Drive EN low or float EN to turn off the device. EN has internal 2MΩ pull-down resistor to ground.
4	ADD	I²C slave addresses program pin. Connect a resistor divider from VCC to ADD to set four different I ² C slave addresses.
5	SCL	Clock pin of the I²C interface. SCL can support an I ² C clock up to 3.4MHz.
6	SDA	Data pin of the I²C interface.
7	OC	Output constant current limit set pin.
8	ALT	Alert output. ALT pulling to logic low indicates that a fault or warning has occurred.
9	VCC	Internal 3.6V LDO regulator output. Decouple VCC with a 1μF capacitor.
10	AGND	Analog Ground. Connect AGND to GND.
12	OUT	Output power pin. Place the output capacitor close to OUT and GND.
13	BST2	Bootstrap. Connect a 0.1μF capacitor between SW2 and BST2 to form a floating supply across the high-side switch driver.
14	SW2	Switching node of the second half bridge. Connect one end of the inductor to SW2 for the current to run through the bridge.
15	SW1	Switching node of the first half bridge. Connect one end of the inductor to SW1 for the current to run through the bridge.
16	BST1	Bootstrap. Connect a 0.1μF capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver.

BLOCK DIAGRAM

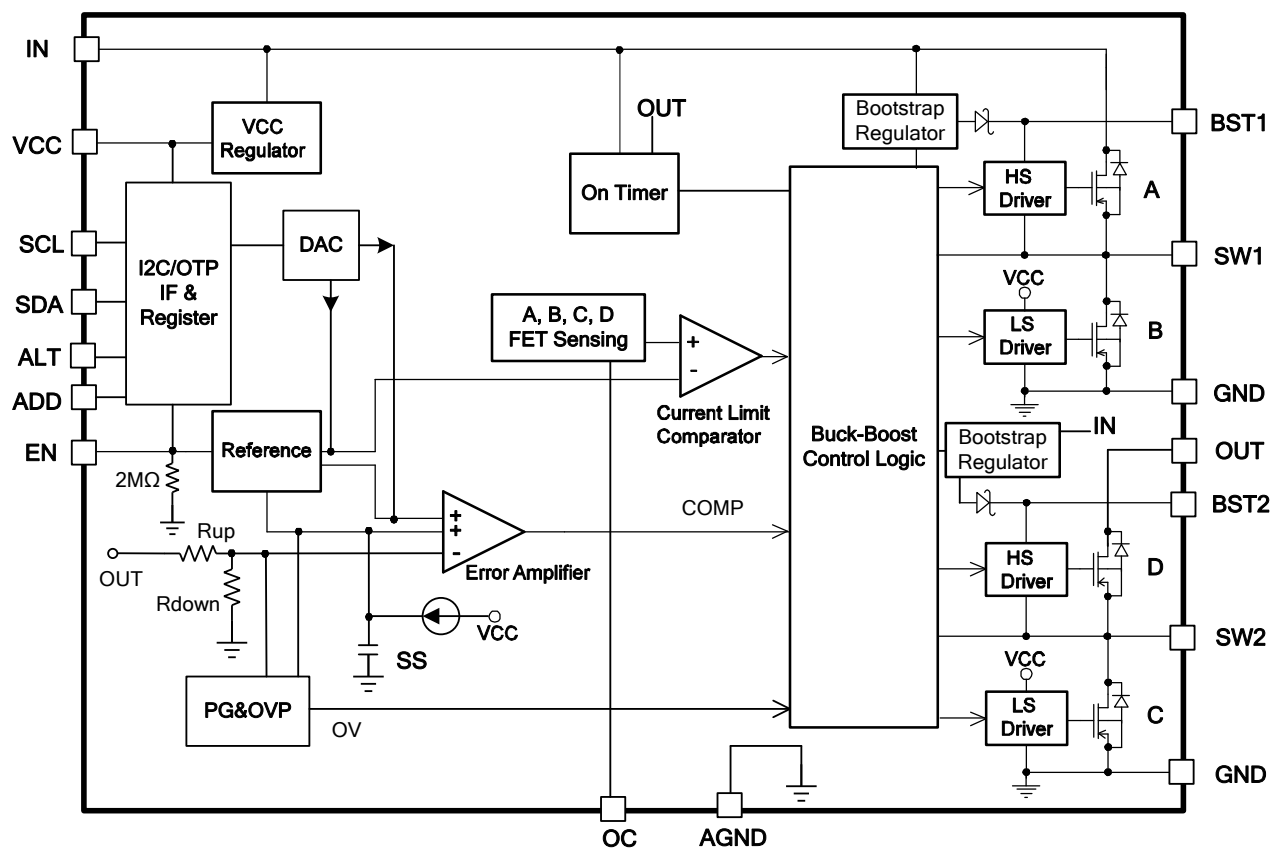


Figure 2: Functional Block Diagram

OPERATION

The MP8859 is a 4-switch, integrated buck-boost converter that can work in constant-on-time (COT) mode with fixed frequency, which provides fast transient response for the buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the full input range and smooth transient between different modes.

Buck-Boost Operation

The MP8859 can regulate the output to be above, equal to, or below the input voltage. Based on the one-inductor, four-switch power structure shown in Figure 3, the MP8859 can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

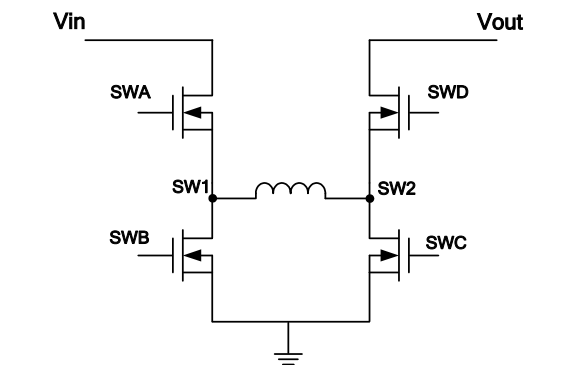


Figure 3: Buck-Boost Topology

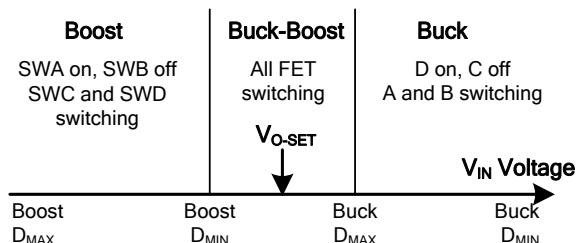


Figure 4: Buck-Boost Operation Range

Buck Mode ($V_{IN} > V_{OUT}$)

When the input voltage is significantly higher than the output voltage, the MP8859 works in buck mode. In buck mode, SWA and SWB are switching for the buck regulation. SWC is off, and SWD remains on to conduct the inductor current.

SWA works with COT control logic, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct the inductor current. When the inductor current drops to the COMP voltage (V_{COMP}), SWB turns off, and SWA turns

on. SWA turns on for a fixed on-time period before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier (EA) output from the V_{OUT} feedback and internal FB reference voltage (see Figure 5).

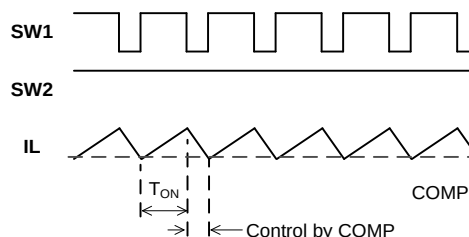


Figure 5: Buck Waveform

Boost Mode ($V_{IN} < V_{OUT}$)

When the input voltage is significantly lower than the output voltage, the MP8859 works in boost mode. In boost mode, SWC and SWD are switching for the boost regulation. SWB is off, and SWA remains on to conduct the inductor current.

SWC remains off with COT control in each period, while SWD turns on as a complement of SWC to boost the inductor current to the output. In each cycle, SWC turns on to conduct the inductor current. When the inductor current rises and reaches V_{COMP} , SWC turns off and SWD turns on. SWC turns off with a fixed off-time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 6).

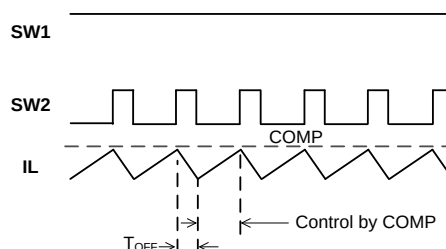


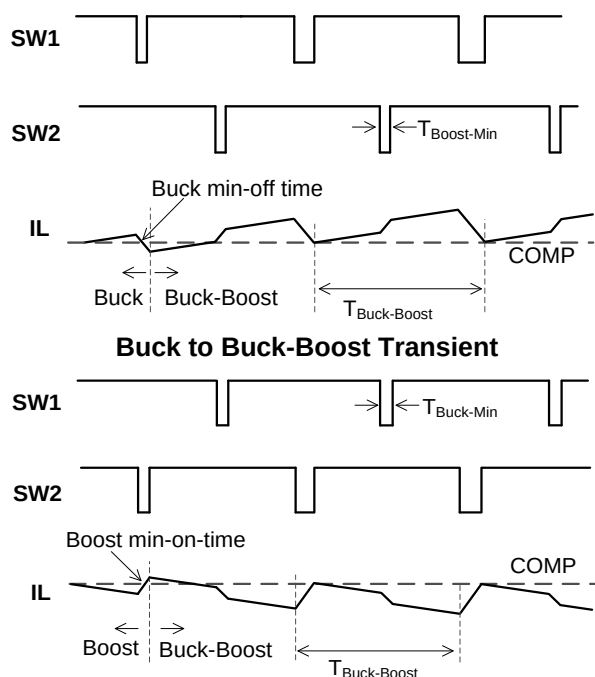
Figure 6: Boost Waveform

Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

When V_{IN} is close to V_{OUT} , the converter cannot provide enough energy to operate in buck mode due to SWA's minimum off time, or the converter supplies too much power to V_{OUT} in boost mode due to SWC's minimum on time. The MP8859 uses buck-boost control to regulate the output in these conditions.

In buck mode, if V_{IN} drops and the SWA off period is close to the buck minimum off time, the buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on-time period (buck high-side MOSFET (HS-FET) on period), the boost starts with SWA and SWC on (boost low-side MOSFET (LS-FET) on). SWA and SWD turn on again for the rest period of the boost period (boost HS-FET on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until the inductor current drops to V_{COMP} . Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

In boost mode, if V_{IN} drops and the SWC on period is close to the boost minimum on time, buck-boost mode engaged. After the boost constant-off time period (SWA and SWD on), SWB and SWD remain on until the inductor current signal drops to V_{COMP} , just like a buck off-time period control. After the inductor current signal triggers V_{COMP} , SWA and SWB turn on for the buck on time, which is followed by a boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period. Figure 7 shows the buck-boost waveform for both $V_{IN} > V_{OUT}$ and $V_{IN} < V_{OUT}$.



Boost to Buck-Boost Transient
Figure 7: Buck-Boost Waveform

In buck-boost mode, if V_{IN} is higher than 130% of V_{OUT} , the MP8859 switches from buck-boost mode to buck mode. If V_{IN} is lower than 20% of V_{OUT} , the MP8859 switches from buck-boost mode to boost mode.

Working Mode Selection

The MP8859 works with a fixed frequency in heavy-load condition. When the load current decreases, the MP8859 can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

FCCM (or Forced PWM)

In FCCM condition, the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN}/V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces the inductor current to work in continuous mode with a fixed frequency, producing a lower V_{OUT} ripple than in PSM mode.

PSM (Auto PFM/PWM Mode)

In PSM condition, once the inductor current drops to 0A, SWD turns off to prevent the current from flowing from V_{OUT} to V_{IN} , forcing the inductor current to work in discontinuous conduction mode (DCM). Simultaneously, the internal off-time clock stretches once the MP8859 enters DCM mode. The frequency drops when the inductor current conduction period decreases, helping to save power loss and reduce the V_{OUT} ripple.

If V_{COMP} drops to the PSM threshold, even if the IC stretches the frequency, the MP8859 stops switching to decrease more switching power loss. The MP8859 recovers switching once V_{COMP} rises above the PSM threshold. The switching pulse skips based on V_{COMP} in very light-load condition. PSM has a much higher efficiency than FCCM mode in light load, but the V_{OUT} ripple may be higher due to the group switching pulse.

Internal VCC Regulator

The 3.6V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 3.6V, the output of the regulator is in

full regulation. If V_{IN} is less than 3.6V, the output decreases with V_{IN} . VCC requires an external 1 μ F ceramic capacitor for decoupling.

Enable Control (EN)

The MP8859 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MP8859 truly shuts down after 55ms. The MP8859's I²C register value is reset to default only after the MP8859 truly shuts down. If EN is pulled high within 55ms, the I²C register is not reset, and the MP8859 enables the output with previous register setting.

If the output discharge function is disabled, the MP8859 truly shuts down once EN is pulled down for more than 100 μ s, and the MP8859 I²C register is reset after a 100 μ s delay.

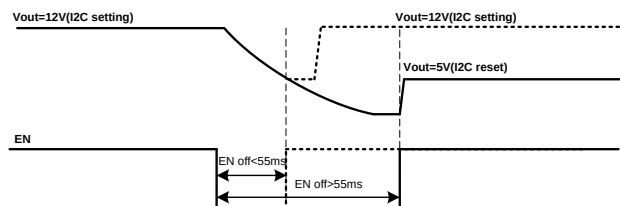


Figure 8: EN On/Off Logic for I²C Register Reset

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage and enables or disables the entire IC.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 3.6V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

If the output of the MP8859 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage (see Figure 9).

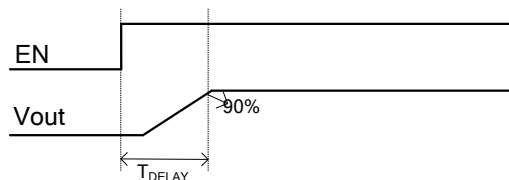


Figure 9: EN On to $V_{OUT} > 90\%$ Delay

Output Constant Current Limit (OCP)

The MP8859 has a constant-current limit control loop to limit the output average current. The current information is sensed from switch A, B, C, and D. Then an average algorithm is used to calculate the output current.

When the output current exceeds the current-limit threshold, the output voltage starts to drop. If V_{OUT} drops below the under-voltage (UV) threshold (typically 50% below the reference), the MP8859 enters hiccup mode or latch-off mode according to the I²C setting.

In hiccup mode, the MP8859 stops switching and recovers automatically with 12.5% duty cycles. In latch-off mode, the MP8859 stops switching until the IC restarts (V_{IN} , EN, or EN bit toggle).

Over-Voltage Protection (OVP)

The MP8859 monitors a resistor-divided feedback voltage to detect output over-voltage. When the feedback voltage rises higher than 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V_{OUT} is higher than the absolute OVP threshold (23V), the MP8859 stops switching and turns on the OUT-to-ground discharge resistor.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal

supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP8859 has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or enable off), the discharge path is turned off when $V_{OUT} < 50\text{mV}$ or waits for the 50ms maximum timer to pass. This function can also be disabled via the I²C.

Thermal Warning (TSW) and Shutdown (TSD)

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP8859 sets the OTW bit[D5] to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit[D5] is 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8859 interface is an I²C slave, which supports both fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously via the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of an I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition

is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

The master then generates the SCL clocks and transmits the device address and the read/write direction bit (r/w) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by an SDA line. Each byte of data is to be followed by an acknowledge bit.

I²C Update Sequence

The MP8859 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP8859 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8859. The MP8859 performs an update on the falling edge of the LSB byte. Examples of an I²C write and read sequence are shown on page 23.

I²C Start-Up Timing

The I²C function is enabled once $V_{IN} > UVLO$ and EN is active. The I²C function continues working during OCP, OVP, and thermal shutdown.

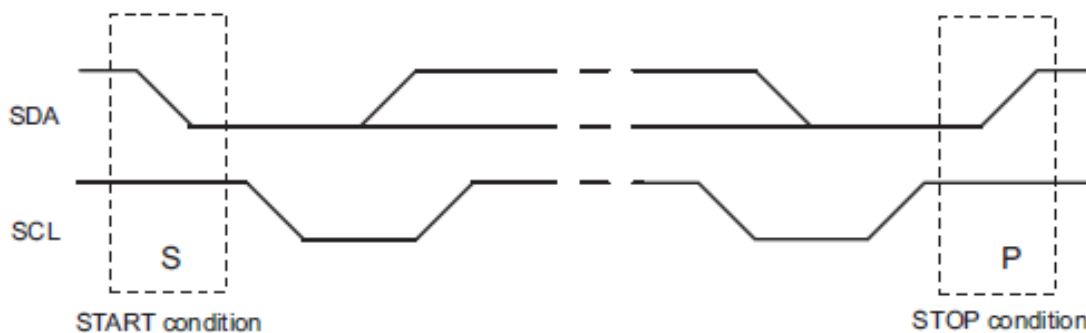
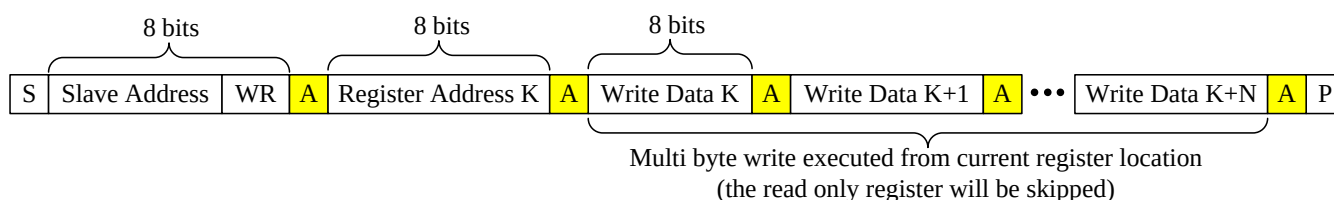


Figure 10: Start and Stop Condition



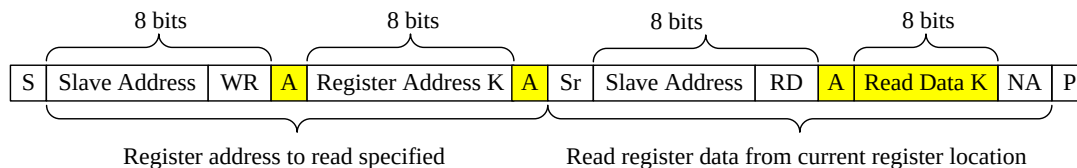
☐	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	WR Write = 0
☒	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition	RD Read = 1

I²C Write Example – Write Single Register



☐	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	WR Write = 0
☒	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition	RD Read = 1

I²C Write Example – Write Multi Register



☐	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	Sr = Repeat Start Condition	WR Write = 0
☒	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition		RD Read = 1

I²C Read Example – Read Single Register

I²C REGISTER MAP

ADD (HEX)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
00	VOUT_L	r/w	RESERVED					VOUT DATA BIT LOW [2:0]*			
01	VOUT_H	r/w	VOUT DATA BIT HIGH [10:3]*								
02	VOUT_GO	r/w	RESERVED						PG_DELAY_EN*	GO_BIT	
03	IOUT_LIM	r/w	reserved	OUTPUT CURRENT LIMIT THRESHOLD (0A-6.35A/50mA STEP FOR 21.5K OC RESISTOR)*							
04	CTL1	r/w	EN*	HICCUP_OCP_OVP*	DISCHG_EN*	MODE*	FREQ		RESERVED		
05	CTL2	r/w	LINE DROP COMP*		SS*		RESERVED				
06	RESERVED	r	RESERVED, ALL "0"							RESERVED	
07	RESERVED	r	RESERVED								
08	RESERVED	r	RESERVED								
09	Status	r	PG	OTP	OTW	CC_CV	RESERVED				
0A	Interrupt	W1C	OTEMPP_ENTER	OT_WARNING_ENTER	OC_ENTER	OC_RECOVER	UVP_FALLING	OTEMPP_EXIT	OT_WARNING_EXIT	PG_RISING	
0B	Mask	r/w	RESERVED			OTPMASK*	OTWMSK*	OC_MSK*	UVP_MSK*	PG_MSK*	
0C	ID1	r	OTP Configure Code. "0x00" means standard MP8859, "0x01" means MP8859-0001 part number*								
27	MFR_ID	r	MANUFACTURER ID: b '0000 1001'								
28	DEV_ID	r	DEVICE ID: b '0101 1000'								
29	IC_REV	r	IC REVISION: b '0000 0001'								

NOTE:

* These items have one-time programmable (OTP) non-volatile memory. The OTP is reloaded to the I²C register during V_{IN} > UVLO or EN shutdown.

REGISTER DESCRIPTION

I²C Bus Slave Address

A resistor-divider from VCC to GND can achieve an accurate reference voltage. Connect ADD to this reference voltage to set different I²C addresses. The internal circuit changes the I²C address accordingly. Table 1 shows the four voltage thresholds for the four I²C addresses and recommended setting resistors.

Table 1: I²C Address Setting via ADD Voltage

ADD Voltage	ADD Upper Resistor R4 (kΩ)	ADD Lower Resistor R5 (kΩ)	I ² C Address	
			Binary	Hex
<25%V _{CC}	No connection	No connection	1100 000	60H
25%V _{CC} -50%V _{CC}	499	301	1100 010	62H
50%V _{CC} -75%V _{CC}	301	499	1100 100	64H
>75%V _{CC}	100	No connection	1100 110	66H

VOUT Setting

The registers VOUT_L and VOUT_H set the output voltage and follow the 11-bit direct format below.

Name	VOUT															
Format	Direct, unsigned binary integer															
Register Name	N/A					VOUT_H D[7:0]								VOUT_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	N/A					Data bit high								Data bit Low		
Default value (5V)	N/A					500 Integer										

The output voltage can be calculated with Equation (1):

$$V_{out} (V) = V/100 \quad (1)$$

Where V is an 11-bit unsigned binary integer of VOUT[10:0], and V ranges from 0 to 2047. The V_{OUT} resolution is 10mV/LSB.

Inside the MP8859, there is a feedback resistor network from OUT to the internal FB reference voltage. The feedback resistor ratio is V_{OUT}/V_{FB} = 12.5. The output voltage change slew rate is fixed at 1mV/μs. Refer to the GO_BIT bit when implementing the output voltage change.

VOUT_GO Register

GO_BIT D[0]

The MP8859 can be controlled when to V_{OUT} begins to change. Set GO_BIT to 1 to start the output change based on the V_{OUT} register. When the V_{OUT} change is complete (internal V_{REF} steps to the goal of V_{REF}), GO_BIT auto-resets to 0. This prevents a false operation of the V_{OUT} scaling.

Write the output voltage (0x00 and 0x01 registers) first, and then write GO_BIT = 1. V_{OUT} changes based on new register setting. GO_BIT resets to 0 when V_{OUT} reaches a new value. The host can read GO_BIT to determine if the V_{OUT} scaling is finished or not.

The V_{OUT}-to-ground discharge function is enabled when GO_BIT is 1. This can help ramp V_{OUT} from high to low in light-load condition.

When GO_BIT is 0, V_{OUT} will not change. When GO_BIT is 1, V_{OUT} changes based on the V_{OUT} register setting. After V_{OUT} scaling finishes, GO_BIT is reset to 0 automatically.

PG_DELAY_EN D[1]

When PG_DELAY_EN D[1] is 0, there is no delay on PG. When PG_DELAY_EN D[1] is 1, PG experiences a 100µs rising delay. The default value is 0.

IOUT_LIM Register

Set the output current limit threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	N/A	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default value (3.5A)	N/A	70 Integer						

IOUT_OC can be calculated with Equation (2):

$$\text{IOUT_OC (A)} = \text{IOUT_LIM} \times 0.05 \quad (2)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM D[6:0]. The IOUT_OC resolution is 50mA/LSB (maximum value is 6.35A).

The OC pin-to-ground resistor should be 21.5KΩ when using the above IOUT_LIM register. A 22nF (C6) filter capacitor should be added on OC to keep the CC loop stable. The MP8859 supports the I²C setting IOUT_LIM directly. If the CC threshold needs to be changed dynamically after the MP8859 has already entered the CC limit operation state, it is recommended to change the CC threshold step-by-step (e.g.: 50mA per step) instead of changing the current value to the final value directly.

CTL1 Register

NAME	BITS	DEFAULT	DESCRIPTION
EN	D[7]	1	I ² C controlled turn-on or turn-off of the part. When the external EN pin is low, the converter is off, and the I ² C shuts down. When EN is high, the EN bit takes over. 1: part is turned on. Default. 0: part is turned off. I ² C register does not reset.
HICCUP OCP_OVP	D[6]	1	Over-current and over-voltage protection mode selection. 1: hiccup mode 0: latch-off mode
DISCHG_EN	D[5]	1	Output discharge enable bit. 1: output discharge function during EN or V _{IN} shutdown 0: no discharge output during shutdown
MODE	D[4]	1	Default is PWM mode for light load. 0: enables auto PFM/PWM mode 1: sets forced PWM mode
FREQ	D[3:2]	00	Sets the switching frequency. 00: 500kHz 01, 10, 11: reserved

CTL2 Register

NAME	BITS	DEFAULT	DESCRIPTION
LINE DROP COMP	D[7:6]	01	Sets the output voltage compensation vs. the load feature. 00: no compensation 01: V_{OUT} compensates 150mV @ 3A I_{OUT} 10: V_{OUT} compensates 300mV @ 3A I_{OUT} 11: V_{OUT} compensates 500mV @ 3A I_{OUT} The above compensation amplitude is fixed for any output voltage. Line drop compensation is only enabled for V_{OUT} 5V and above.
SS	D[5:4]	11	Sets the output start-up soft-start timer (from 0 to 100%). For 5V output voltage: 00: 300μs 01: 500μs 10: 700μs 11: 900μs The SS slew rate is constant but changes for different V_{OUT} values.

Status Register

NAME	BITS	DEFAULT	DESCRIPTION	
PG	D[7]	X	Output power good indication. 0: output power is not good 1: output power is good	These status bits indicate instantaneous value.
OTP	D[6]	X	Over temperature protection indication. 0: normal state 1: chip is in over-temperature protection state	
OTW	D[5]	X	Over-temperature warning indication. 0: normal state 1: chip is in-over temperature warning state	
CC_ CV	D[4]	X	The chip works in constant-current output mode or constant-voltage output mode. 0: CV mode 1: CC mode	

Interrupt Register

NAME	BITS	DESCRIPTION	
OTEMPP_ ENTER	D[7]	Over-temperature protection entry indication. When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if setting OTPMSK = 1. OTPMSK = 1 only masks the interrupt pin's output (ALT).	This bit is latched once triggered. Write 0xFF to this register to reset the interrupt and ALT pin's state.
OTWARNING_ ENTER	D[6]	Die temperature early warning entry bit. When this bit is high, the die temperature is higher than 120°C. This bit is not masked, even if setting OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).	
OC_ENTER	D[5]	Entry of OC or CC current-limit mode. The OC_MSK bit can enable or disable OC_ENTER and OC_RECOVER alert output.	
OC_RECOVER	D[4]	Recovery from CC current-limit mode. Recovering from a hiccup will not trigger this interrupt signal.	
UVP_FALLING	D[3]	Output voltage is in under-voltage protection.	
OTEMPP_EXIT	D[2]	Over-temperature protection exit. OTPMSK can mask off the ALT of this bit.	
OTWARNING_ EXIT	D[1]	Die temperature early warning exit bit. When the die temperature is lower than 100°C, this bit is set to 1. This bit is not masked, even if setting OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).	
PG_RISING	D[0]	Output power good rising edge.	

MSK Register

NAME	BITS	DEFAULT	DESCRIPTION
OTPMSK	D[4]	0	Set OTPMSK = 1 to mask off the OTP alert. OTPMSK = 1 only masks the interrupt pin's output (ALT). This is not the interrupt register, but is similar for other mask bits.
OTWMSK	D[3]	0	Masks off the over-temperature warning
OC_MSK	D[2]	0	Masks off both OC/CC entry and recovery.
UVP_MSK	D[1]	0	Masks off the output UVP interrupt.
PG_MSK	D[0]	0	Masks off the PG indication function on ALT. 1: ALT pin does not indicate a PG event 0: ALT indicates a PG rising event.

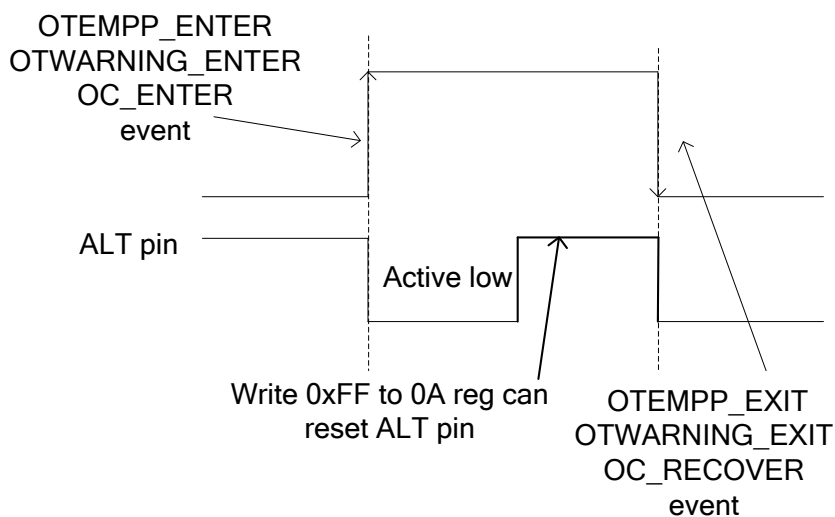


Figure 11: ALT Behavior of OTP, OT Warning, and OC Recovery

APPLICATION INFORMATION

Selecting the Inductor

In a buck-boost topology circuit, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. Two critical inductance values can be determined according to the buck mode and boost mode current ripple using Equation (2) and Equation (3):

$$L_{\text{MIN-BUCK}} = \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times F_{\text{REQ}} \times \Delta I_L} \quad (2)$$

$$L_{\text{MIN-BOOST}} = \frac{V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{V_{\text{OUT}} \times F_{\text{REQ}} \times \Delta I_L} \quad (3)$$

Where F_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set to 10 - 40% of the inductor current. The minimum inductor value for the application is the higher than both the Equation (2) and Equation (3) results.

In addition to the inductance value, the inductor must support the peak current based on Equation (4) and Equation (5) to avoid saturation:

$$I_{\text{PEAK-BUCK}} = I_{\text{OUT}} + \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{2 \times V_{\text{IN(MAX)}} \times F_{\text{REQ}} \times L} \quad (4)$$

$$I_{\text{PEAK-BOOST}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{\eta \times V_{\text{IN(MIN)}}} + \frac{V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{2 \times V_{\text{OUT}} \times F_{\text{REQ}} \times L} \quad (5)$$

Where η is the estimated efficiency of the MP8859.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors plus an electrolytic capacitor for input and output capacitors to filter the input and output ripple current and achieve stable operation.

Since the input capacitor absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100μF electrolytic capacitor and a 22μF ceramic capacitor are sufficient.

The output capacitor stabilizes the DC output voltage. Low ESR capacitors and a sufficient capacitor value are recommended to limit the output voltage ripple. Considering the ceramic DC voltage derating, if the output voltage is less than 12V, the minimum C_{OUT} should be 22μF×5 ceramic. If the output voltage is higher than 12V, use a 100μF low ESR ($\leq 80\text{m}\Omega$) aluminum electrolytic or polymer capacitor and two 10μF ceramic capacitors.

The input and output ceramic capacitors must be placed as close as possible to the device.

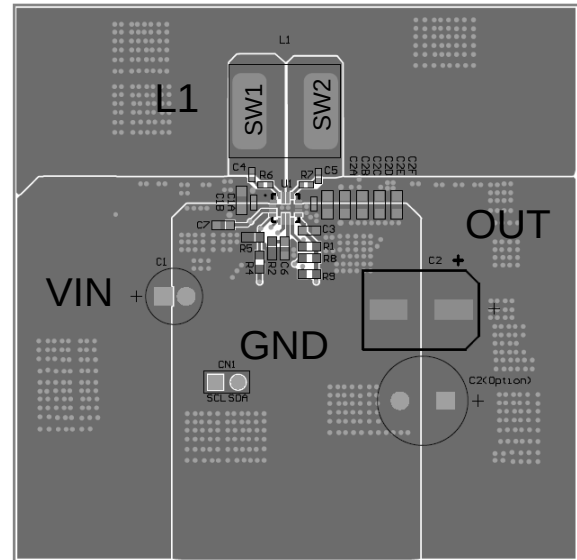
PCB Layout Guidelines ⁽⁹⁾

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 12 and follow the guidelines below.

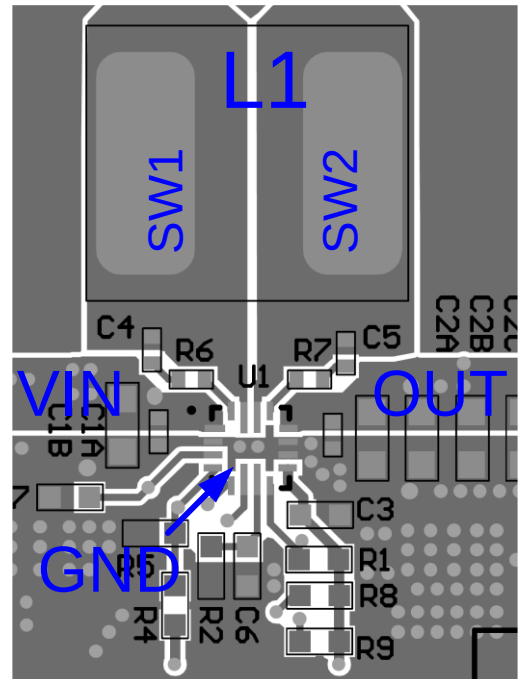
1. Place the ceramic C_{IN} and C_{OUT} capacitor close to the IC's V_{IN} -to-GND and OUT -to-GND pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Use short, direct, and wide traces to connect OUT .
6. Add vias under the IC and routing the OUT trace on both PCB layers (highly recommended).
7. Use a large copper plane for SW1 and SW2.
8. Place the VCC decoupling capacitor as close to VCC as possible.

NOTES:

- 9) The recommended layout is based on the typical application circuits in Figure 13 and Figure 14.



Top Layer



Close-Up of Layout

Figure 12: Recommended Layout

TYPICAL APPLICATION CIRCUITS

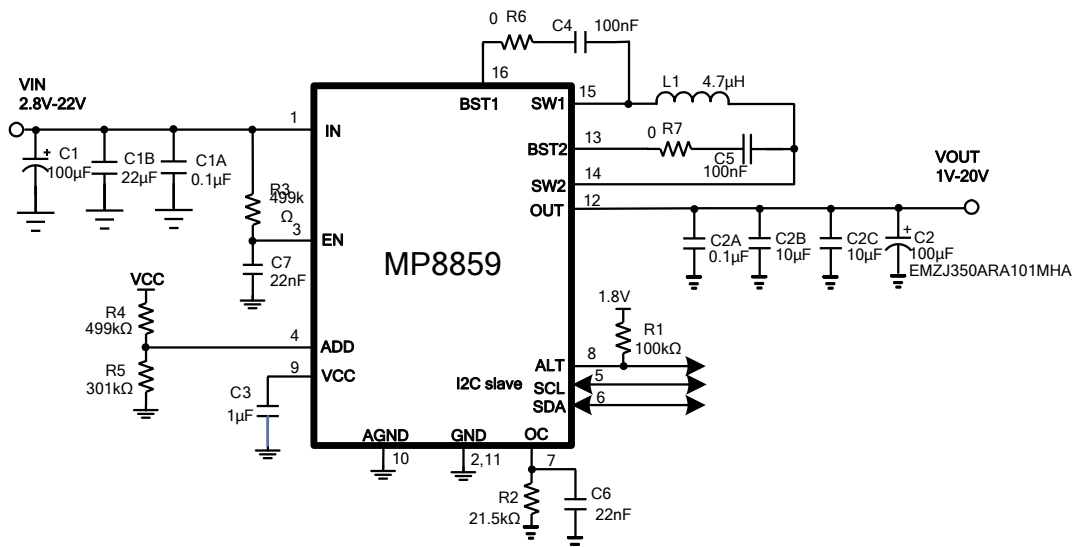


Figure 13: Typical Application Circuit for 1 - 20V_{OUT}

NOTE: Refer to the recommended maximum I_{OUT} vs. V_{IN} and V_{OUT} with 120µF low ESR C_{OUT} capacitor curve on page 9.

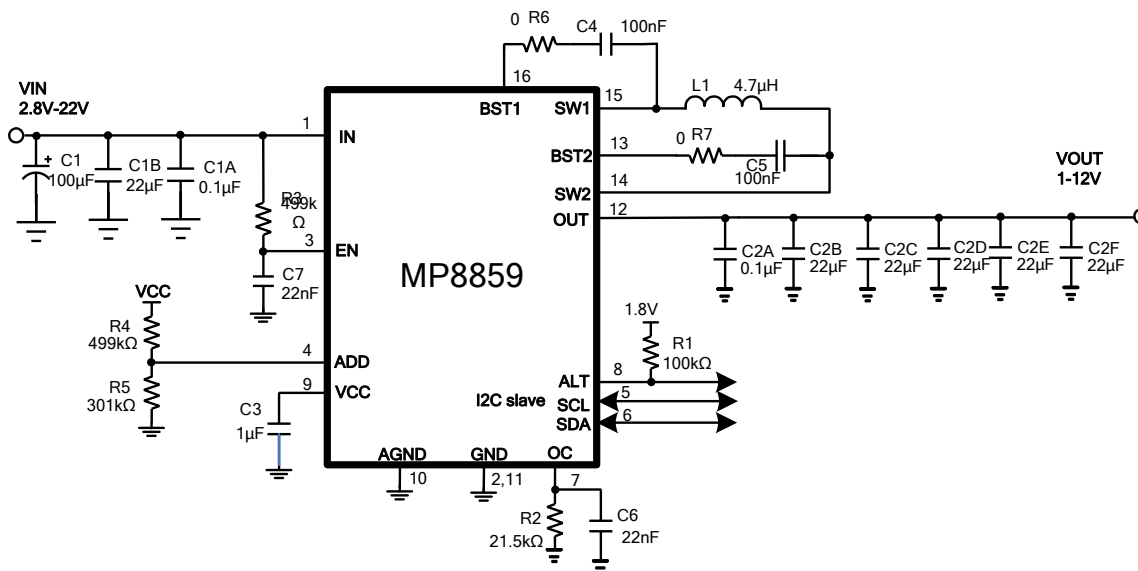
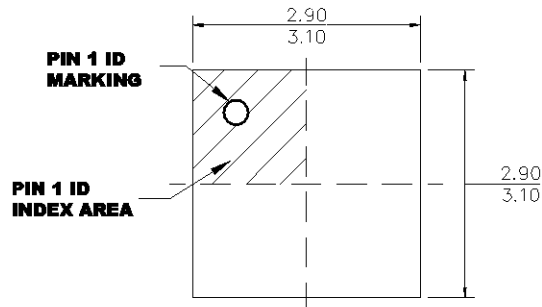


Figure 14: Typical Application Circuit for 1 - 12V_{OUT}

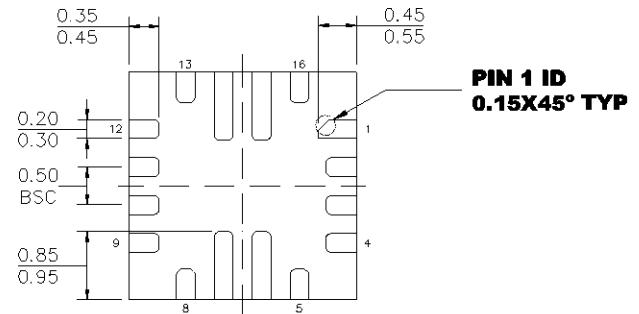
NOTE: Refer to the recommended maximum I_{OUT} vs. V_{IN} and V_{OUT} with 22µF x5 ceramic C_{OUT} capacitor curve on page 9.

PACKAGE INFORMATION

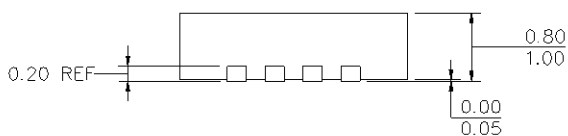
QFN-16 (3mmx3mm)



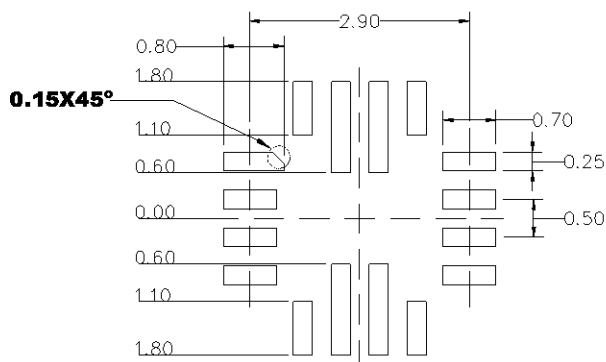
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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