Thyristor

V_{RRM}	=	1200 V
I_{TAV}	=	45 A
V_T	=	1.37 V

Single Thyristor

Part number

CS45-12io1

1
2
3

Backside: anode

2 ○—◁▷—○ 1

3
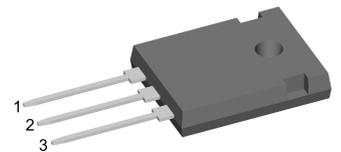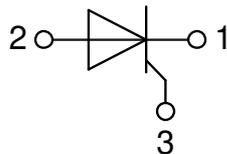
Features / Advantages:
- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:
- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-247
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Terms and Conditions of Usage

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office.

Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend
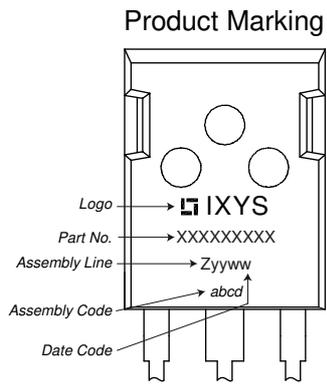- to perform joint risk and quality assessments;
- the conclusion of quality agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

Thyristor | Ratings

Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25°C$				1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25°C$				1200	V
$I_{R/D}$	reverse current, drain current	$V_{R/D} = 1200$ V	$T_{VJ} = 25°C$			50	µA
		$V_{R/D} = 1200$ V	$T_{VJ} = 125°C$			3	mA
V_T	forward voltage drop	$I_T = 45$ A	$T_{VJ} = 25°C$			1.36	V
		$I_T = 90$ A				1.73	V
		$I_T = 45$ A	$T_{VJ} = 125°C$			1.37	V
		$I_T = 90$ A				1.85	V
I_{TAV}	average forward current	$T_C = 110°C$	$T_{VJ} = 150°C$			45	A
$I_{T(RMS)}$	RMS forward current	180° sine				71	A
V_{T0}	threshold voltage	for power loss calculation only	$T_{VJ} = 150°C$			0.88	V
r_T	slope resistance					11	mΩ
R_{thJC}	thermal resistance junction to case					0.4	K/W
R_{thCH}	thermal resistance case to heatsink				0.25		K/W
P_{tot}	total power dissipation	$T_C = 25°C$				310	W
I_{TSM}	max. forward surge current	t = 10 ms; (50 Hz), sine	$T_{VJ} = 45°C$			520	A
		t = 8,3 ms; (60 Hz), sine	$V_R = 0$ V			560	A
		t = 10 ms; (50 Hz), sine	$T_{VJ} = 150°C$			440	A
		t = 8,3 ms; (60 Hz), sine	$V_R = 0$ V			475	A
I^2t	value for fusing	t = 10 ms; (50 Hz), sine	$T_{VJ} = 45°C$			1.35	kA²s
		t = 8,3 ms; (60 Hz), sine	$V_R = 0$ V			1.31	kA²s
		t = 10 ms; (50 Hz), sine	$T_{VJ} = 150°C$			970	A²s
		t = 8,3 ms; (60 Hz), sine	$V_R = 0$ V			940	A²s
C_J	junction capacitance	$V_R = 400$ V f = 1 MHz	$T_{VJ} = 25°C$		22		pF
P_{GM}	max. gate power dissipation	$t_P = 30$ µs	$T_C = 150°C$			10	W
		$t_P = 300$ µs				5	W
P_{GAV}	average gate power dissipation					0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125°C$; f = 50 Hz repetitive, $I_T = 135$ A				150	A/µs
		$t_P = 200$ µs; $di_G/dt = 0.3$ A/µs;					
		$I_G = 0.3$ A; V = ⅔ V_{DRM} non-repet., $I_T = 45$ A				500	A/µs
$(dv/dt)_{cr}$	critical rate of rise of voltage	V = ⅔ V_{DRM}	$T_{VJ} = 125°C$			1000	V/µs
		$R_{GK} = ∞$; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	$V_D = 6$ V	$T_{VJ} = 25°C$			1.5	V
			$T_{VJ} = -40°C$			1.6	V
I_{GT}	gate trigger current	$V_D = 6$ V	$T_{VJ} = 25°C$			80	mA
			$T_{VJ} = -40°C$			200	mA
V_{GD}	gate non-trigger voltage	$V_D = ⅔ V_{DRM}$	$T_{VJ} = 125°C$			0.2	V
I_{GD}	gate non-trigger current					10	mA
I_L	latching current	$t_p = 10$ µs	$T_{VJ} = 25°C$			150	mA
		$I_G = 0.3$ A; $di_G/dt = 0.3$ A/µs					
I_H	holding current	$V_D = 6$ V $R_{GK} = ∞$	$T_{VJ} = 25°C$			100	mA
t_{gd}	gate controlled delay time	$V_D = ½ V_{DRM}$	$T_{VJ} = 25°C$			2	µs
		$I_G = 0.3$ A; $di_G/dt = 0.3$ A/µs					
t_q	turn-off time	$V_R = 100$ V; $I_T = 45$ A; V = ⅔ V_{DRM} $T_{VJ} = 125$ °C			150		µs
		di/dt = 15 A/µs dv/dt = 20 V/µs $t_p = 200$ µs					

IXYS reserves the right to change limits, conditions and dimensions.   Data according to IEC 60747and per semiconductor unless otherwise specified   20150827b

Package	TO-247			Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal				70	A
T_{VJ}	virtual junction temperature			-40		150	°C
T_{op}	operation temperature			-40		125	°C
T_{stg}	storage temperature			-40		150	°C
Weight					6		g
M_D	mounting torque			0.8		1.2	Nm
F_c	mounting force with clip			20		120	N

Product Marking

Logo → IXYS
Part No. → XXXXXXXXX
Assembly Line → Zyyww
Assembly Code → abcd
Date Code

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CS45-12io1	CS45-12io1	Tube	30	467685

Similar Part	Package	Voltage class
CS45-08io1	TO-247AD (3)	800
CS45-16io1	TO-247AD (3)	1600
CS45-16io1R	ISOPLUS247 (3)	1600
CLA50E1200HB	TO-247AD (3)	1200

Equivalent Circuits for Simulation   *on die level* $T_{VJ} = 150\,°C$

I → V_0 — R_0 **Thyristor**

$V_{0\,max}$	threshold voltage	0.88	V
$R_{0\,max}$	slope resistance *	8.5	mΩ

Outlines   TO-247
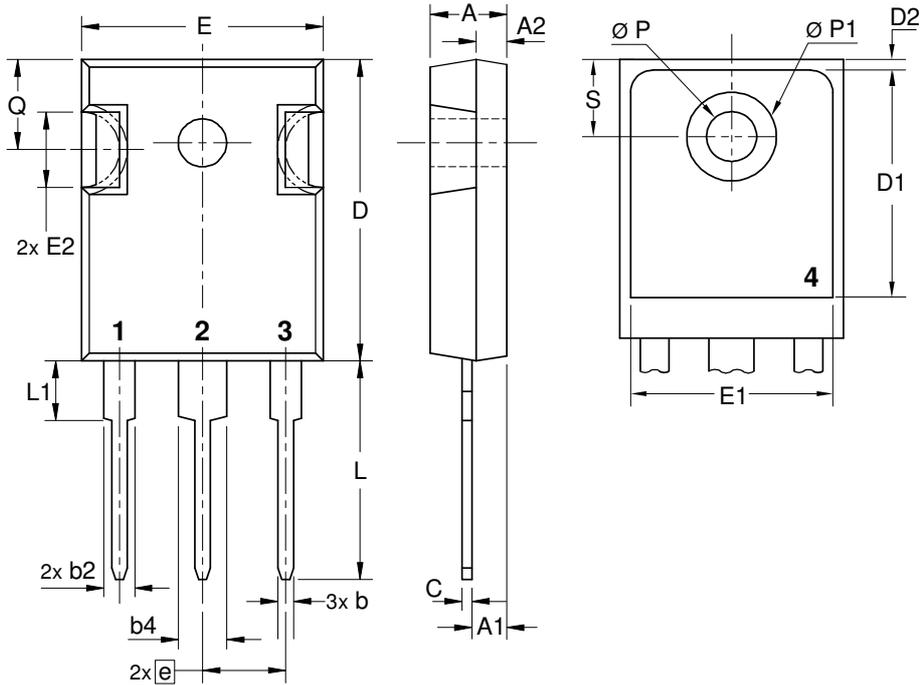
Sym.	Inches		Millimeter	
	min.	max.	min.	max.
A	0.185	0.209	4.70	5.30
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.50	2.49
D	0.819	0.845	20.79	21.45
E	0.610	0.640	15.48	16.24
E2	0.170	0.216	4.31	5.48
e	0.215 BSC		5.46 BSC	
L	0.780	0.800	19.80	20.30
L1	-	0.177	-	4.49
Ø P	0.140	0.144	3.55	3.65
Q	0.212	0.244	5.38	6.19
S	0.242 BSC		6.14 BSC	
b	0.039	0.055	0.99	1.40
b2	0.065	0.094	1.65	2.39
b4	0.102	0.135	2.59	3.43
c	0.015	0.035	0.38	0.89
D1	0.515	-	13.07	-
D2	0.020	0.053	0.51	1.35
E1	0.530	-	13.45	-
Ø P1	-	0.29	-	7.39
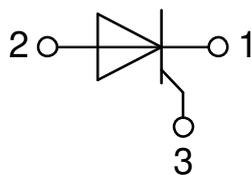
Thyristor
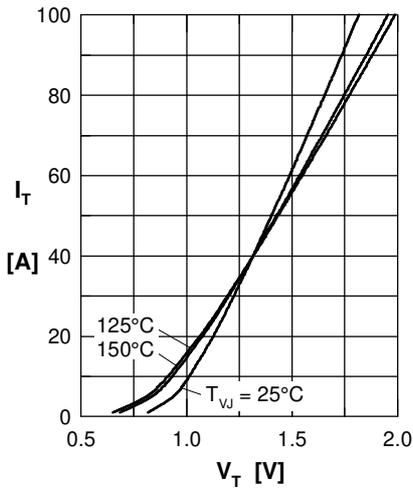
Fig. 1 Forward characteristics
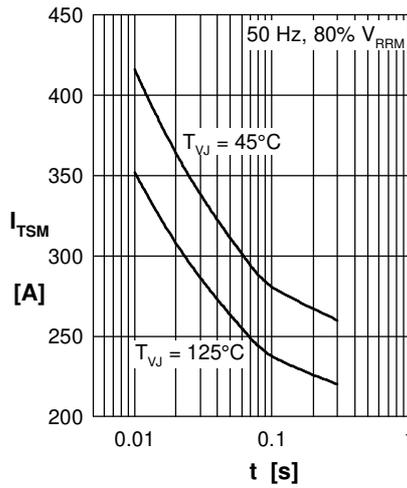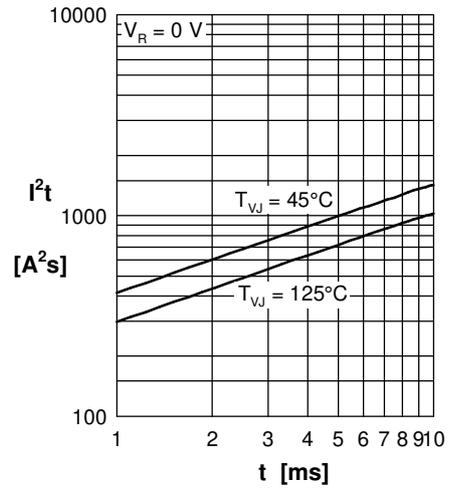

Fig. 2 Surge overload current
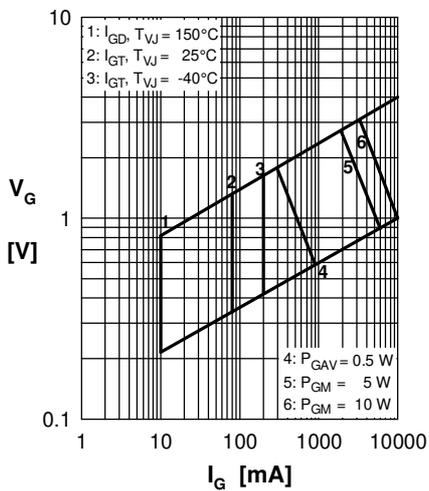

Fig. 3 I²t versus time (1-10 ms)

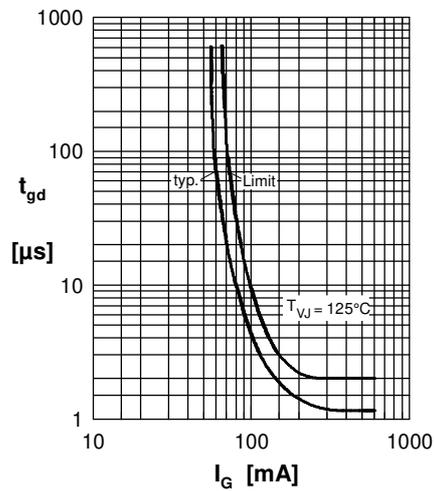Fig. 4 Gate trigger characteristics

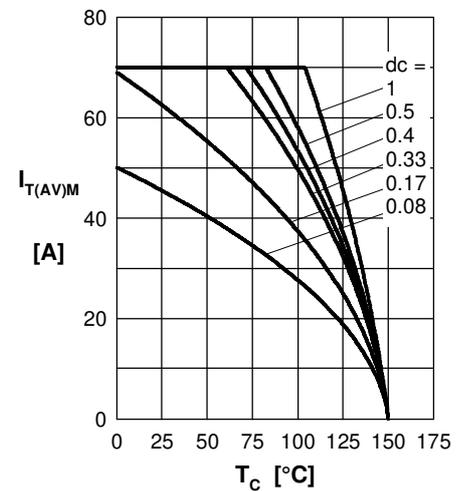Fig. 5 Gate controlled delay time

Fig. 6 Max. forward current
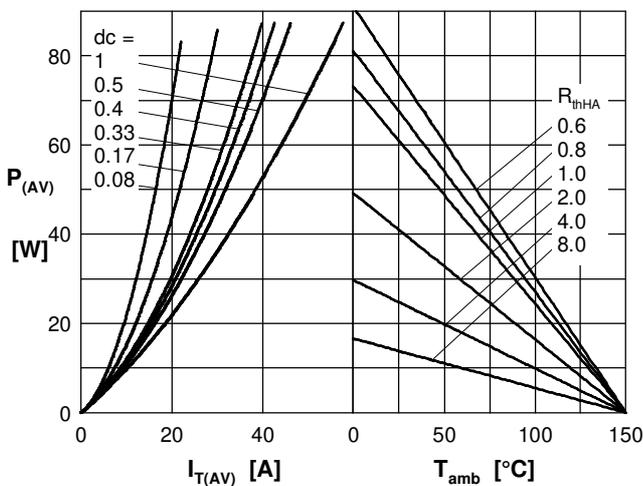at case temperature

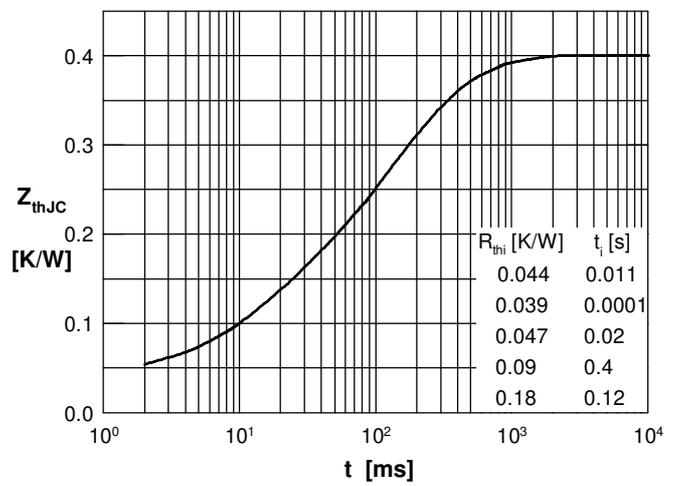Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

Fig. 8 Transient thermal impedance junction to case