Single-Channel, 16-Bit Current/Voltage Output DAC with HART Connectivity

Data Sheet **AD5423**

FEATURES

- 16-bit resolution and monotonicity
- Current or voltage output available on a single terminal
- Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, 0 mA to 24 mA, ±20 mA, ±24 mA, and −1 mA to +22 mA
- Voltage output ranges (with 20% overrange): 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V
- User programmable offset and gain
- Advanced on-chip diagnostics, including a 12-bit ADC
- On-chip reference
- −40°C to +115°C temperature range
- 32-Lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

- Process control
- Actuator control
- Channel isolated analog outputs
- Programmable logic controller (PLC) and distributed control systems (DCS) applications
- HART network connectivity

GENERAL DESCRIPTION

The AD5423 is a single-channel, voltage and current output digital-to-analog converter (DAC) that operates with a power supply range from −33 V minimum on AV_{SS} to +33 V maximum on AV_{DD1}. The C_{HART} pin enables a Highway Addressable Remote Transducer® (HART) signal to be coupled on the current output.

The AD5423 uses a versatile, 4-wire, serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, digital signal processor (DSP), and microcontroller interface standards. The interface also features an optional SPI cyclic redundancy check (CRC) and a watchdog timer (WDT). The AD5423 offers improved diagnostic features from earlier versions of similar DACs, such as an integrated, 12-bit diagnostic analog-to-digital converter (ADC).

PRODUCT HIGHLIGHTS

1. 16-bit performance.
2. Range of diagnostic features.
3. Integrated 12-bit monitoring ADC.
4. HART compliant.

COMPANION PRODUCTS

Product Family: AD5758, AD5753, AD5755-1, AD5422
HART Modem: AD5700, AD5700-1
External References: ADR431, ADR3425, ADR4525
Digital Isolators: ADuM141D, ADuM142D
Power: ADP1031, ADP2360, ADM6339

Rev. A
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REVISION HISTORY

1/2020—Rev. 0 to Rev. A

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7/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

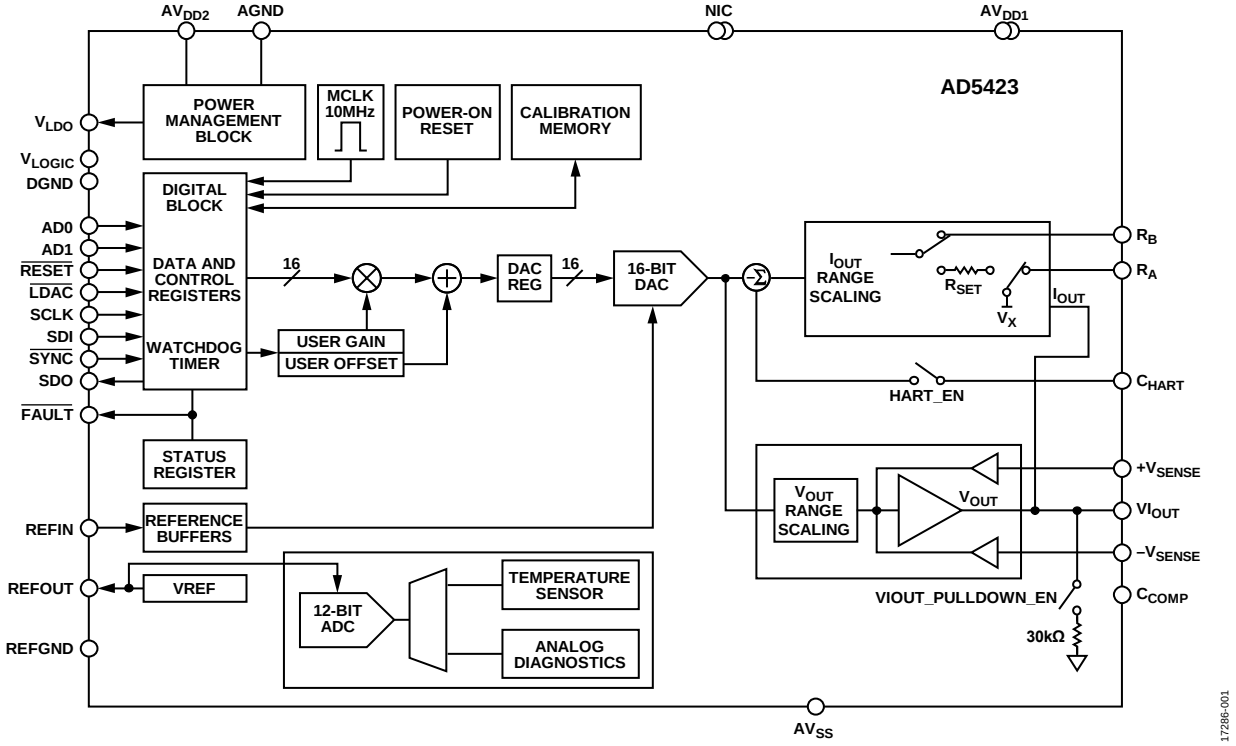


Figure 1.

SPECIFICATIONS

AV_{DD1} = 15 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = 0 V, REFIN = 2.5 V external, voltage output: load resistor (R_{LOAD}) = 1 kΩ, load capacitor (C_{LOAD}) = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, junction temperature (T_J) < 125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					Statement of available ranges rather than absolute minimum and maximum values
Output Voltage Ranges (V_{OUT})	0		5	V	Trimmed V_{OUT} ranges
	0		10	V	
	−5		+5	V	
	−10		+10	V	
Output Voltage Overranges	0		6	V	Untrimmed overranges
	0		12	V	
	−6		+6	V	
	−12		+12	V	
Output Voltage Offset Ranges	−0.3		+5.7	V	Untrimmed negatively offset ranges
	−0.4		+11.6	V	
Resolution	16			Bits	
VOLTAGE OUTPUT ACCURACY					Loaded and unloaded, accuracy specifications refer to trimmed V_{OUT} ranges only, unless otherwise noted
Total Unadjusted Error (TUE)	−0.05		+0.05	% full-scale range (FSR)	
	−0.01		+0.01	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		15		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		0.35	1.5	ppm FSR/°C	
Integral Nonlinearity (INL)	−0.006		+0.006	% FSR	All ranges
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic, all ranges
Zero-Scale Error	−0.02	±0.002	+0.02	% FSR	
Zero-Scale Error Temperature Coefficient (TC)[2]		±0.3		ppm FSR/°C	
Bipolar Zero Error	−0.017	+0.001	+0.017	% FSR	±5 V, ±10 V
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	±5 V, ±10 V
Offset Error	−0.022	±0.002	+0.022	% FSR	
Offset Error TC[2]		±0.3		ppm FSR/°C	
Gain Error	−0.022	±0.001	+0.022	% FSR	
Gain Error TC[2]		±0.6		ppm FSR/°C	
Full-Scale Error	−0.022	±0.001	+0.022	% FSR	
Full-Scale Error TC[2]		±0.5		ppm FSR/°C	
VOLTAGE OUTPUT CHARACTERISTICS					
Headroom	2			V	Minimum voltage required between VI_{OUT} and AV_{DD1} supply
Footroom	2			V	Minimum voltage required between VI_{OUT} and AV_{SS} supply
Short-Circuit Current		16		mA	
Load	1			kΩ	For specified performance
Capacitive Load Stability[2]			10	nF	
			2	µF	External compensation capacitor of 220 pF connected
DC Output Impedance		7		mΩ	
DC Power Supply Rejection Ratio (PSRR)		10		µV/V	
V_{OUT} and −V_{SENSE} Common-Mode Rejection Ratio (CMRR)		10		µV/V	Error in V_{OUT} voltage due to changes in −V_{SENSE} voltage

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT (I_{OUT})					
Current Output Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
	−20		+20	mA	
	−24		+24	mA	
	−1		+22	mA	
Resolution	16			Bits	
CURRENT OUTPUT ACCURACY (EXTERNAL CURRENT SETTING RESISTOR (R_{SET}))[3]					Assumes ideal 13.7 kΩ resistor
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.05		+0.05	% FSR	
	−0.01		+0.01	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		2	5	ppm FSR/°C	
INL	−0.006		+0.006	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.03	±0.002	+0.03	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.03	±0.001	+0.03	% FSR	
Offset Error TC[2]		±0.7		ppm FSR/°C	
Gain Error	−0.05	±0.002	+0.05	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.05	±0.002	+0.05	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
TUE	−0.06		+0.06	% FSR	
	−0.012		+0.012	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		12	15.5	ppm FSR/°C	
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.04	±0.003	+0.04	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.003	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	
Offset Error	−0.04	±0.002	+0.04	% FSR	
Offset Error TC[2]		±0.6		ppm FSR/°C	
Gain Error	−0.06	±0.002	+0.06	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.06	±0.003	+0.06	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT ACCURACY (INTERNAL R_{SET})					
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.12		+0.12	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	6	ppm FSR/°C	Output drift
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.04	±0.001	+0.04	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.04	±0.001	+0.04	% FSR	
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.1	±0.003	+0.1	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.12	±0.003	+0.12	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
TUE	−0.12		+0.12	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	6	ppm FSR/°C	Output drift
INL	−0.02		+0.02	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.06	±0.002	+0.06	% FSR	
Zero-Scale TC[2]		±2		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.002	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.3		ppm FSR/°C	
Offset Error	−0.06	±0.001	+0.06	% FSR	
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.12	±0.003	+0.12	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.12	±0.003	0.12	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
CURRENT OUTPUT CHARACTERISTICS					
Headroom	2.3			V	Minimum voltage required between VI_{OUT} and AV_{DD1} supply
Footroom	2.35/0			V	Minimum voltage required between VI_{OUT} and AV_{SS} supply, unipolar ranges do not require any footroom
Resistive Load[2]			1000	Ω	The current output is characterized with a maximum load of 1 kΩ, do not exceed the headroom and footroom compliance
Output Impedance		100		MΩ	Midscale output
DC PSRR		0.1		µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input					
Reference Input Voltage[4]		2.5		V	For specified performance
DC Input Impedance	55	120		MΩ	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C (including drift after 1000 hours at T_J = 150°C)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Reference TC[2]	−12		+12	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		80		nV/√Hz	At 10 kHz
Capacitive Load[2]			1000	nF	
Load Current		3		mA	
Short-Circuit Current		5		mA	
Line Regulation		1		ppm/V	
Load Regulation		80		ppm/mA	
Thermal Hysteresis[2]		150		ppm	
V_{LDO} PIN OUTPUT					
Output Voltage		3.3		V	
Output Voltage TC[2]		25		ppm/°C	
Output Voltage Accuracy	−2		+2	%	
Externally Available Current			30	mA	
Short-Circuit Current		55		mA	
Load Regulation		0.8		mV/mA	
Capacitive Load		0.1		µF	Recommended operation
ADC					
Resolution		12		Bits	
Total Error		±0.3		% FSR	Total error including reference, Table 15 lists all ADC input nodes
Conversion Time		100		µs	
DIGITAL INPUTS					
Input Voltage					
3 V ≤ V_{LOGIC} ≤ 5.5 V					
High (V_{IH})	0.7 × V_{LOGIC}			V	
Low (V_{IL})			0.3 × V_{LOGIC}	V	
1.71 V ≤ V_{LOGIC} < 3 V					
V_{IH}	0.8 × V_{LOGIC}			V	
V_{IL}			0.2 × V_{LOGIC}	V	
Input Current	−1.5		+1.5	µA	Per pin, internal pull-down on SCLK, SDI, $\overline{\text{RESET}}$, and $\overline{\text{LDAC}}$, internal pull-up on $\overline{\text{SYNC}}$
Pin Capacitance[2]		2.4		pF	Per pin
DIGITAL OUTPUTS					
SDO					
Output Voltage					
Low (V_{OL})			0.4	V	Sinking 200 µA
High (V_{OH})	V_{LOGIC} − 0.2			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance[2]		2.2		pF	
$\overline{\text{FAULT}}$					
Output Voltage					
V_{OL}			0.4	V	10 kΩ pull-up resistor to V_{LOGIC}
		0.6		V	At 2.5 mA
V_{OH}	V_{LOGIC} −0.05			V	10 kΩ pull-up resistor to V_{LOGIC}

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AV_{DD1}	7		33	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 50 V
AV_{DD2}	5		33	V	Maximum operating range of $\lvert AV_{DD2}$ to $AV_{SS}\rvert$ = 50 V
AV_{SS}	−33		0	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 50 V
V_{LOGIC}	1.71		5.5	V	
Supply Quiescent Currents[5]					Quiescent current, assuming no load current
AI_{DD1}		1.0		mA	Voltage output mode
		0.8		mA	Current output mode (unipolar)
AI_{DD2}		3.3		mA	Voltage output mode
		2.9		mA	Current output mode
AI_{SS}		−1.1		mA	Voltage output mode
		−0.23		mA	Current output mode (unipolar)
Current Drawn from V_{LOGIC} Supply (I_{LOGIC})			0.01	mA	V_{IH} = the voltage on the V_{LOGIC} pin, V_{IL} = DGND
Power Dissipation					Power dissipation assuming an ideal power supply and excluding external load power dissipation
		108		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		505		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA
		155		mW	AV_{DD1} = AV_{DD2} = 24 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} =20 mA
		550		mW	AV_{DD1} = AV_{DD2} = 24 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[2] Guaranteed by design and characterization. Not production tested.
[3] See the Current Output section for more information about the internal and external R_{SET} resistors.
[4] The AD5423 is factory calibrated with an external 2.5 V reference connected to REFIN.
[5] Production tested to AV_{DD1} = 30 V, AV_{SS} = −20 V.

AC PERFORMANCE CHARACTERISTICS

AV_{DD1} = 15 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = 0 V, REFIN = 2.5 V external, voltage output: R_{LOAD} = 1 kΩ, C_{LOAD} = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, T_J < 125°C, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Voltage Output					
Output Voltage Settling Time					
		6	20	µs	5 V step to ±0.03% FSR, 0 V to 5 V range
		12	20	µs	10 V step to ±0.03% FSR, 0 V to 10 V range
			15	µs	100 mV step to 1 LSB (16-bit LSB), 0 V to 10 V range
Slew Rate		3		V/µs	0 V to 10 V range, digital slew rate control disabled
Power-On Glitch Energy		25		nV-sec	
Digital-to-Analog Glitch Energy		7		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		2		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 V to 10 V range
Output Noise Spectral Density		185		nV/√Hz	Measured at 10 kHz, midscale output, 0 V to 10 V range
AC PSRR		70		dB	200 mV, 50 Hz and 60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time		15		µs	To 0.1% FSR (0 mA to 24 mA)
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.8		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range
AC PSRR		80		dB	200 mV, 50 Hz and 60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by design and characterization. Not production tested.

TIMING CHARACTERISTICS

AV_{DD1} = 15 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = 0 V, REFIN = 2.5 V external, voltage output: R_{LOAD} = 1 kΩ, C_{LOAD} = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, T_J < 125°C, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	1.71 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Description
t_1	33	20	ns minimum	Serial clock input (SCLK) cycle time, write operation
	120	66	ns minimum	SCLK cycle time, read operation
t_2	16	10	ns minimum	SCLK high time, write operation
	60	33	ns minimum	SCLK high time, read operation
t_3	16	10	ns minimum	SCLK low time, write operation
	60	33	ns minimum	SCLK low time, read operation
t_4	10	10	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, write operation
	33	33	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, read operation
t_5	10	10	ns minimum	24th or 32nd SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	500	500	ns minimum	$\overline{SYNC}$ high time (applies to all register writes outside of those listed in this table)
	1.5	1.5	µs minimum	$\overline{SYNC}$ high time (DAC_INPUT register write)
	500	500	µs minimum	$\overline{SYNC}$ high time (DAC_CONFIG register write, where the RANGE bits (Bits[3:0]) change, see the Calibration Memory CRC section for more timing information)
t_7	5	5	ns minimum	Data setup time
t_8	6	6	ns minimum	Data hold time
t_9	750	750	ns minimum	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{10}	1.5	1.5	µs minimum	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	250	250	ns minimum	$\overline{LDAC}$ pulse width low
t_{12}	600	600	ns maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control disabled
	2	2	µs maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control enabled
t_{13}	See the AC Performance Characteristics section		µs maximum	DAC output settling time
t_{14}	1.5	1.5	µs maximum	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0)
t_{15}	5	5	µs minimum	$\overline{RESET}$ pulse width
t_{16}	40	28	ns maximum	SCLK rising edge to SDO valid
t_{17}	100	100	µs minimum	$\overline{RESET}$ rising edge to first SCLK falling edge after $\overline{SYNC}$ falling edge

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{LOGIC}) and timed from a voltage level of 1.2 V. t_R is rise time. t_F is fall time.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.

Timing Diagrams

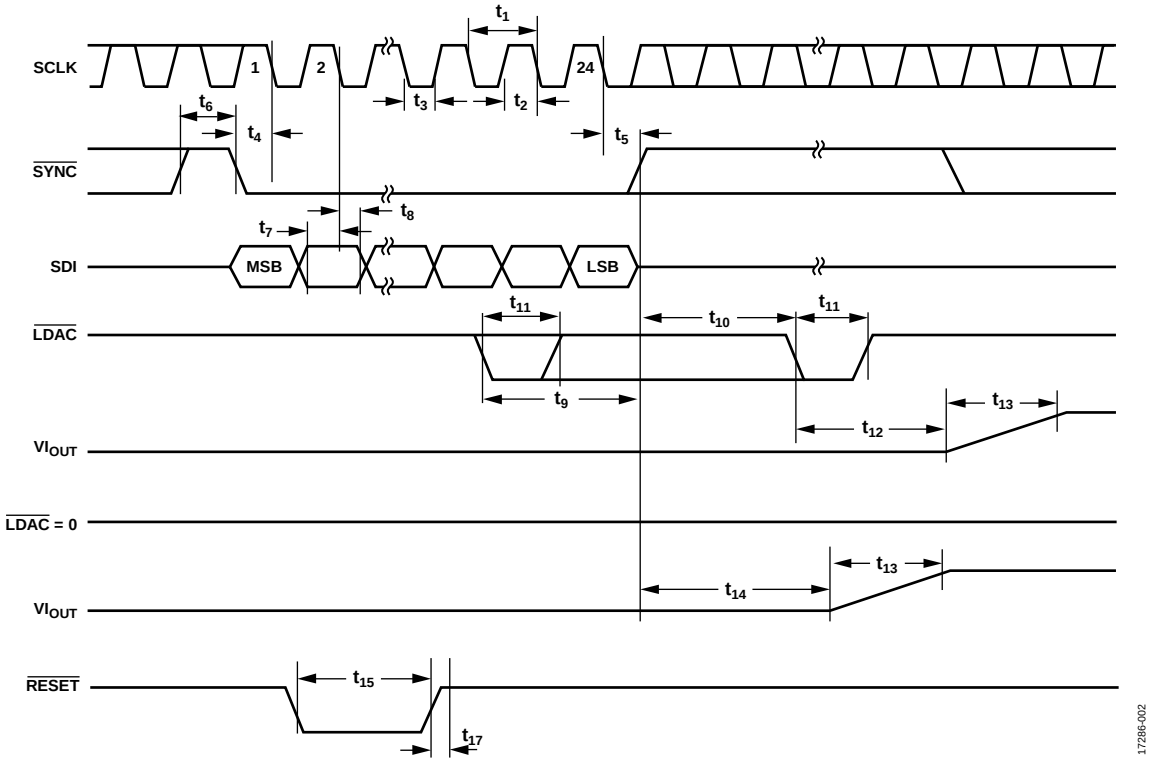


Figure 2. Serial Interface Timing Diagram

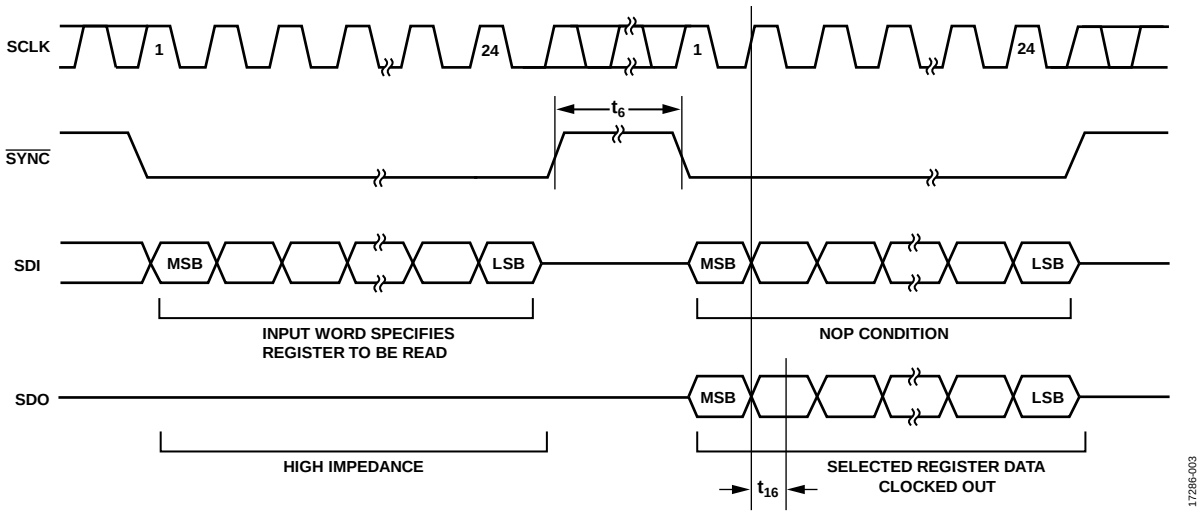
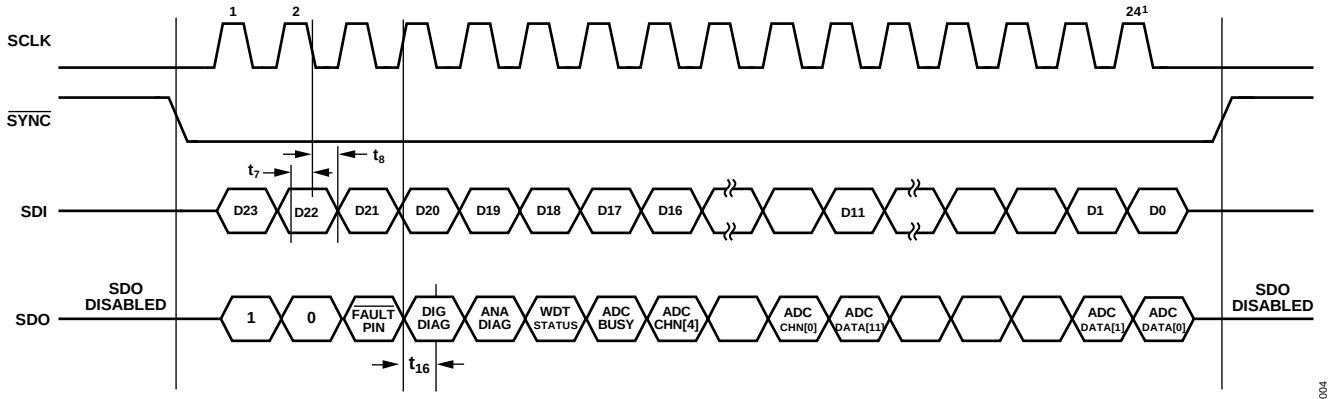


Figure 3. Readback Timing Diagram



[1]IF ANY EXTRA SCLK FALLING EDGES ARE RECEIVED AFTER THE 24TH (OR 32ND, IF CRC IS ENABLED) SCLK, BEFORE SYNC RETURNS HIGH, SDO CLOCKS OUT 0.

Figure 4. Autostatus Readback Timing Diagram

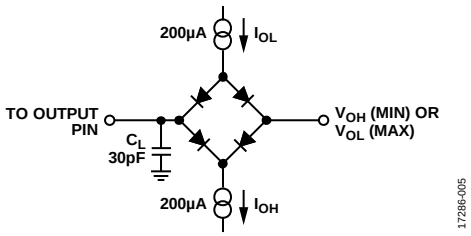


Figure 5. Load Circuit for the SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to ±180 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
AV_{DD1} to AGND, DGND	−0.3 V to +35 V
AV_{SS} to AGND, DGND	+0.3 V to −35 V
AV_{DD1} to AV_{SS}	−0.3 V to +55 V
AV_{DD2} to AGND, DGND	−0.3 V to +35 V
AV_{DD2} to AV_{SS}	−0.3 V to +55 V
V_{LOGIC} to DGND	−0.3 V to +6 V
Digital Inputs[1] to DGND	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
Digital Outputs[2] to DGND	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
REFIN, REFOUT, V_{LDO}, C_{HART} to AGND	−0.3 V to AV_{DD2} + 0.3 V or +6 V (whichever voltage is less)
R_A to AGND	−0.3 V to +4.5 V
R_B to AGND	−0.3 V to +4.5 V
VI_{OUT} to AGND	AV_{SS} − 0.3 V or −35 V (whichever voltage is greater) to AV_{DD1} + 0.3 V or +35 V (whichever voltage is less)
$+V_{SENSE}$ to AGND	±35 V
$-V_{SENSE}$ to AGND	±35 V
C_{COMP} to AGND	AV_{SS} − 0.3 V to AV_{DD1} + 0.3 V
AGND, DGND to REFGND	−0.3 V to +0.3 V
Industrial Operating Temperature Range (T_A)[3]	−40°C to +115°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model[4]	±3 kV
Field Induced Charged Device Model[5]	±750 V

[1] The digital inputs are SCLK, SDI, $\overline{SYNC}$, AD0, AD1, $\overline{RESET}$, and $\overline{LDAC}$.
[2] The digital outputs are $\overline{FAULT}$ and SDO.
[3] Power dissipated on the chip must be derated to keep the junction temperature below 125°C.
[4] As per ANSI/ESDA/JEDEC JS-001, all pins.
[5] As per ANSI/ESDA/JEDEC JS-002, all pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required. θ_{JA} is the junction to ambient thermal resistance and Ψ_{JT} is the junction to top of package thermal resistance.

Table 5. Thermal Resistance

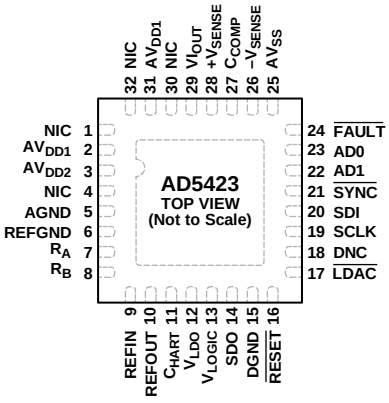
Package Type	θ_{JA}	Ψ_{JT}	Unit
CP-32-12[1]	41.43	0.29	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. DNC = DO NOT CONNECT.
3. CONNECT THE EXPOSED PAD TO THE POTENTIAL OF THE AV_{SS} PIN, OR, ALTERNATIVELY, IT CAN BE LEFT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PAD BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

17286-006

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 30, 32	NIC	No Internal Connection.
2, 31	AV_{DD1}	Positive Analog Supply. The voltage range is 7 V to 33 V.
3	AV_{DD2}	Positive Low Voltage Analog Supply. The voltage range is 5 V to 33 V.
5	AGND	Ground Reference Point for the Analog Circuitry. This pin must be connected to 0 V.
6	REFGND	Ground Reference Point for Internal Reference. This pin must be connected to 0 V.
7	R_A	External Current Setting Resistor. An external, precision, low drift 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the I_{OUT} temperature drift performance.
8	R_B	External Current Setting Resistor. An external, precision, low drift 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the I_{OUT} temperature drift performance.
9	REFIN	External Reference Voltage Input.
10	REFOUT	Internal 2.5 V Reference Voltage Output. REFOUT must be connected to REFIN to use the internal reference. A capacitor between REFOUT and REFGND is not recommended.
11	C_{HART}	HART Input Connection. The HART signal must be ac-coupled to this pin. If HART is not being used, leave this pin unconnected. This pin is disconnected from the HART summing node by default and can be connected via the HART_EN bit in the General Purpose Configuration1 register.
12	V_{LDO}	3.3 V Low Dropout (LDO) Output Voltage. V_{LDO} must be decoupled to AGND with a 0.1 µF capacitor.
13	V_{LOGIC}	Digital Supply. The voltage range on this pin is from 1.71 V to 5.5 V. V_{LOGIC} must be decoupled to DGND with a 0.1 µF capacitor.
14	SDO	Serial Data Output. This pin clocks data from the serial register in readback mode. The maximum SCLK speed for readback mode is 15 MHz and this speed is dependent on the V_{LOGIC} voltage.
15	DGND	Digital Ground.
16	$\overline{\text{RESET}}$	Hardware Reset. Active low input.
17	$\overline{\text{LDAC}}$	Load DAC. Active low input. This pin updates the DAC_OUTPUT register and, consequently, the DAC output. Do not assert $\overline{\text{LDAC}}$ within the 500 ns window before the rising edge of $\overline{\text{SYNC}}$, or 1.5 µs after the rising edge of $\overline{\text{SYNC}}$.
18	DNC	Do Not Connect. Do not connect this pin.
19	SCLK	Serial Clock Input. Data is clocked to the input shift register on the falling edge of the SCLK. In write mode, this pin operates at clock speeds of up to 50 MHz and this speed is dependent on the V_{LOGIC} voltage. In read mode, the maximum SCLK speed is 20 MHz and this speed is dependent on the V_{LOGIC} voltage.

Pin No.	Mnemonic	Description
20	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
21	$\overline{\text{SYNC}}$	Frame Synchronization Signal for the Serial Interface. Active low input. While $\overline{\text{SYNC}}$ is low, data is transferred to the device on the falling edge of SCLK.
22	AD1	Address Decode 1 for the AD5423 on the Board.
23	AD0	Address Decode 0 for the AD5423 on the Board.
24	$\overline{\text{FAULT}}$	Fault Pin. Active low, pseudo open-drain output. This pin is high impedance when no faults are detected and is asserted low when certain faults are detected. Some of these faults include, for example, an open circuit in current mode, a short-circuit in voltage mode, a CRC error, or an overtemperature error. This pin must be connected to V_{LOGIC} with a 10 kΩ pull-up resistor.
25	AV_{SS}	Negative Analog Supply. The voltage range on this pin is 0 V to −33 V. If 0 V is applied, only unipolar ranges are available at V_{OUT} or I_{OUT}.
26	$-V_{SENSE}$	Sense Connection for the Negative Voltage Output Load Connection for V_{OUT} Mode. This pin must stay within ±10 V of AGND for specified operation. It is recommended to connect a series 1 kΩ resistor to this pin. If remote sensing is not used, short this pin to AGND.
27	C_{COMP}	Optional Compensation Capacitor Connection for the V_{OUT} Buffer. Connecting a 220 pF capacitor between this pin and the VI_{OUT} pin allows the voltage output to drive up to 2 µF. The addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
28	$+V_{SENSE}$	Sense Connection for the Positive Voltage Output Load Connection for V_{OUT} Mode. If remote sensing is not being used, short this pin to VI_{OUT} via a series 1 kΩ resistor. It is recommended to connect a series 1 kΩ resistor to this pin.
29	VI_{OUT}	Voltage or Current Output Pin. VI_{OUT} is a shared pin that provides either a buffered output voltage or current.
	EPAD	Exposed Pad. Connect the exposed pad to the potential of the AV_{SS} pin, or, alternatively, it can be left electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

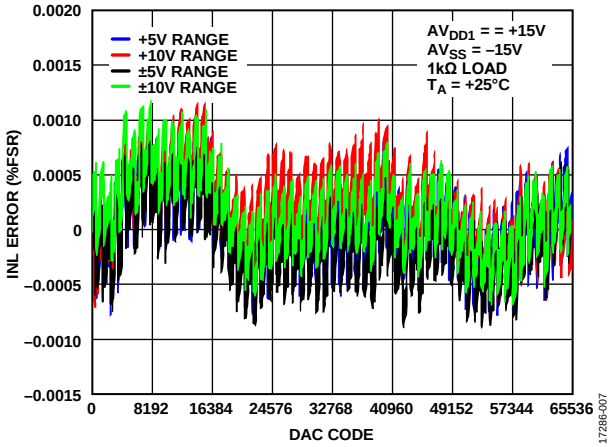


Figure 7. INL Error vs. DAC Code

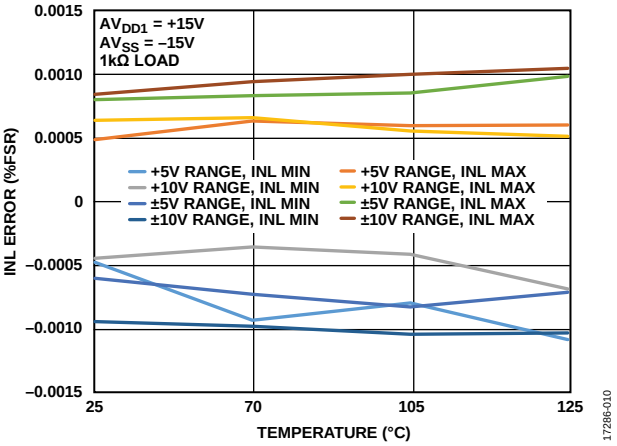


Figure 10. INL Error vs. Temperature

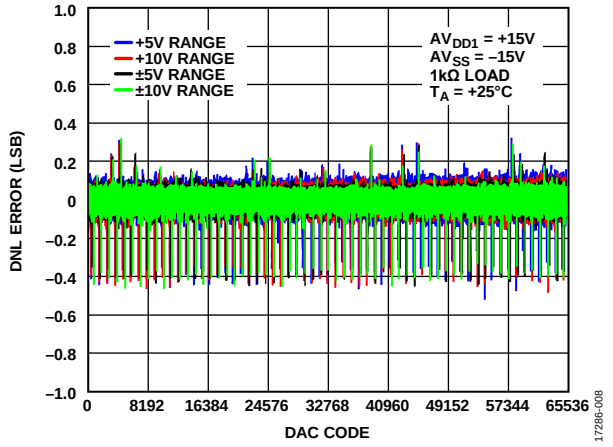


Figure 8. DNL Error vs. DAC Code

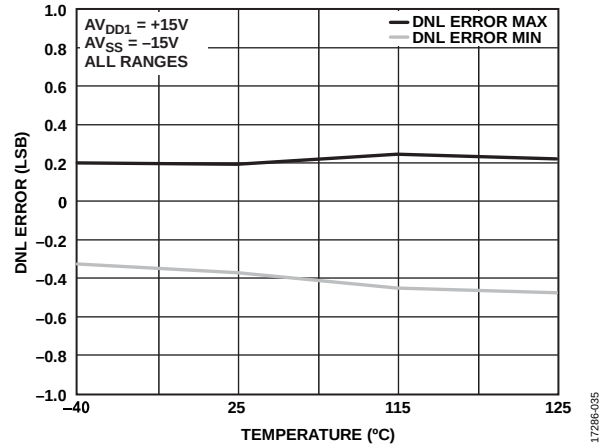


Figure 11. DNL Error vs. Temperature

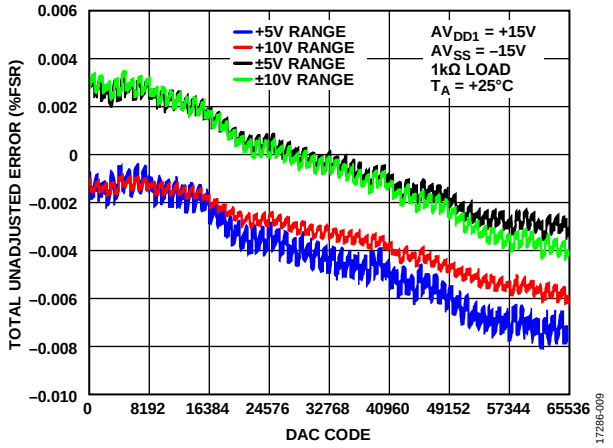


Figure 9. Total Unadjusted Error vs. DAC Code

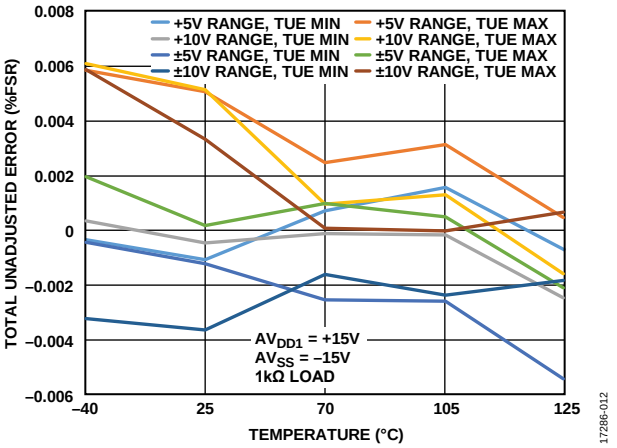


Figure 12. Total Unadjusted Error vs. Temperature

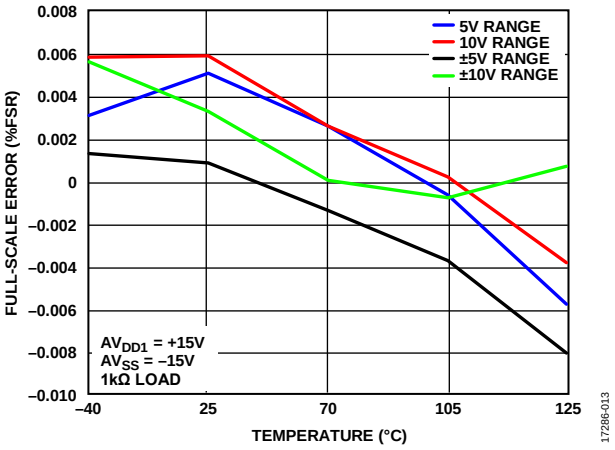


Figure 13. Full-Scale Error vs. Temperature

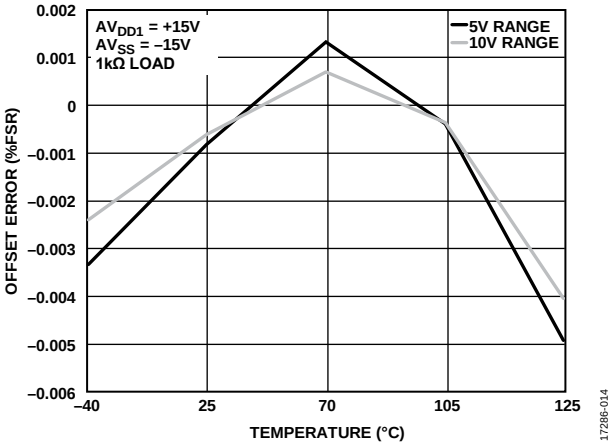


Figure 14. Offset Error vs. Temperature

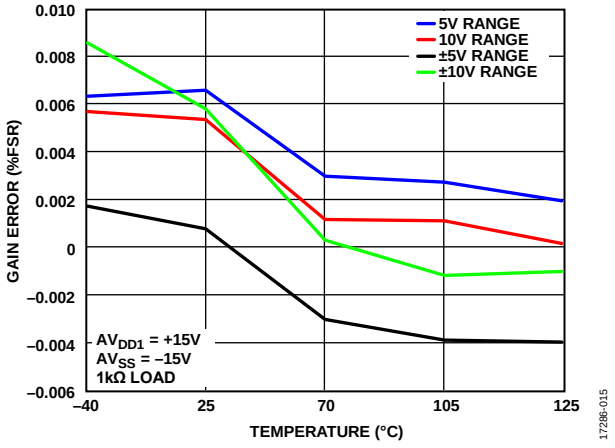


Figure 15. Gain Error vs. Temperature

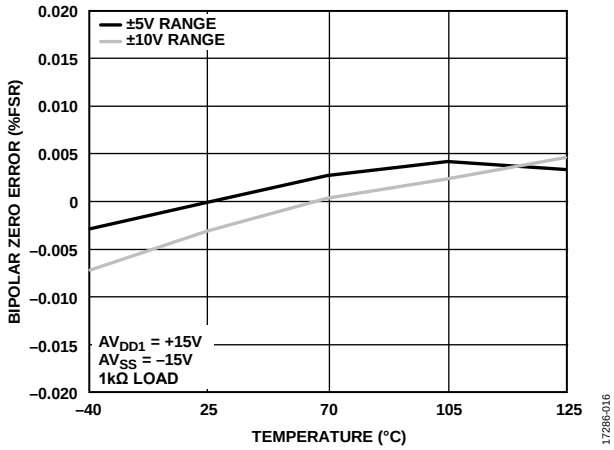


Figure 16. Bipolar Zero Error vs. Temperature

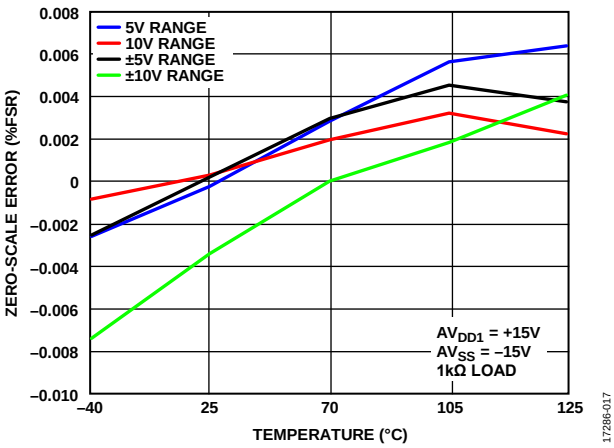


Figure 17. Zero-Scale Error vs. Temperature

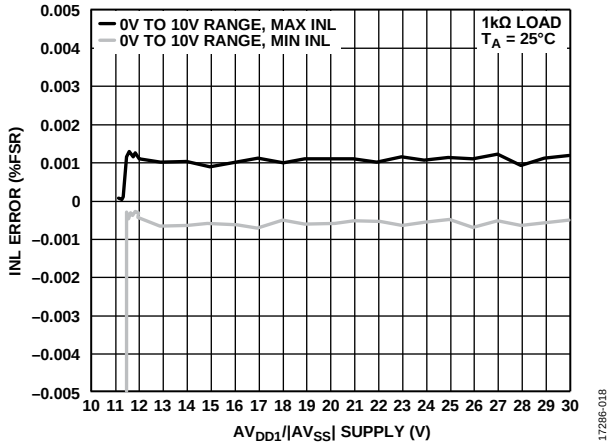


Figure 18. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply

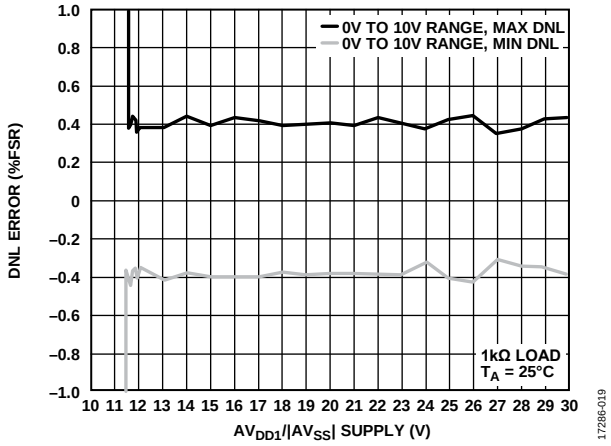


Figure 19. DNL Error vs. AV_{DD1}/|AV_{SS}| Supply

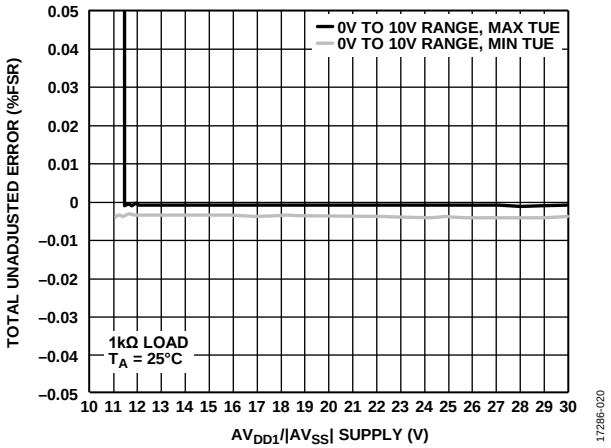


Figure 20. Total Unadjusted Error vs. AV_{DD1}/|AV_{SS}| Supply

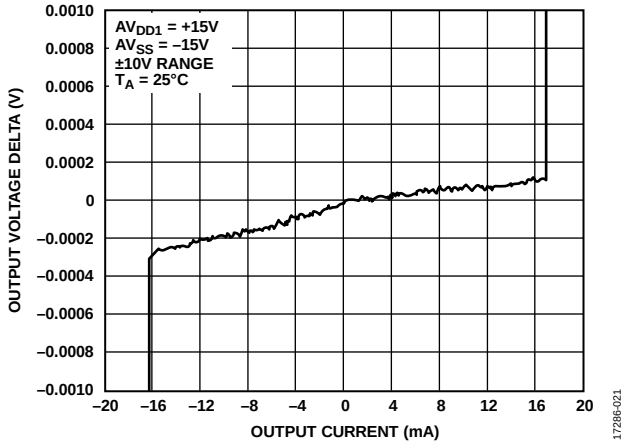


Figure 21. Sink and Source Capability of the Output Amplifier

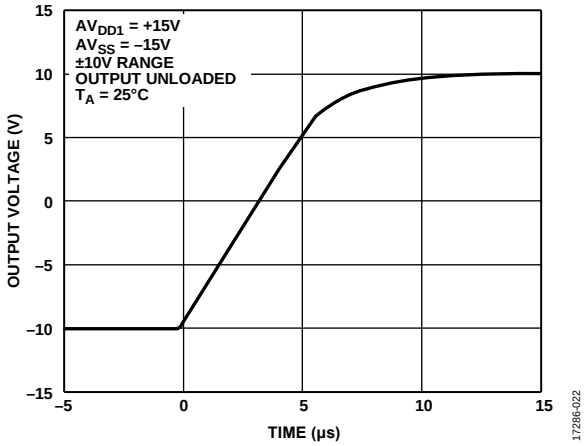


Figure 22. Full-Scale Positive Step

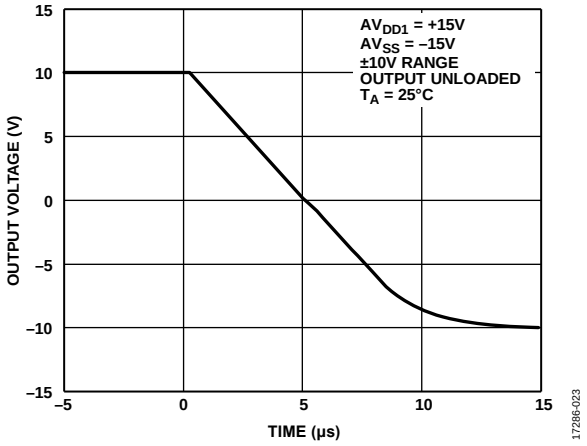


Figure 23. Full-Scale Negative Step

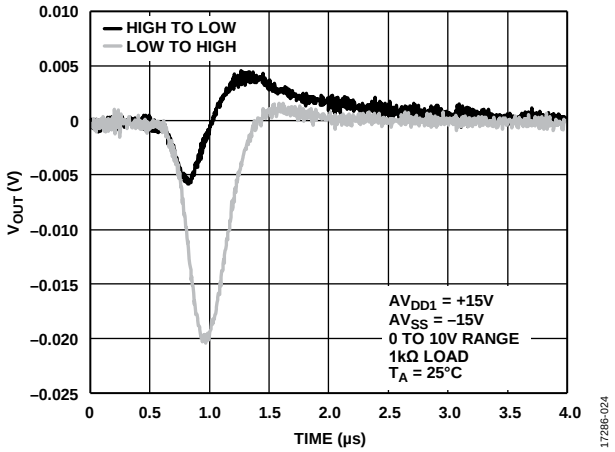


Figure 24. Digital-to-Analog Glitch Major Code Transition

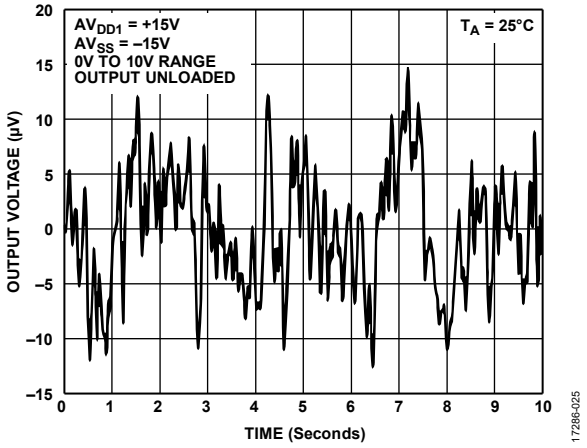


Figure 25. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

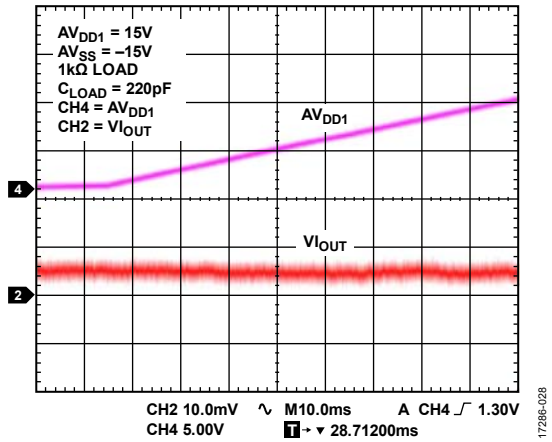


Figure 28. V_{OUT} vs. Time on Power Up

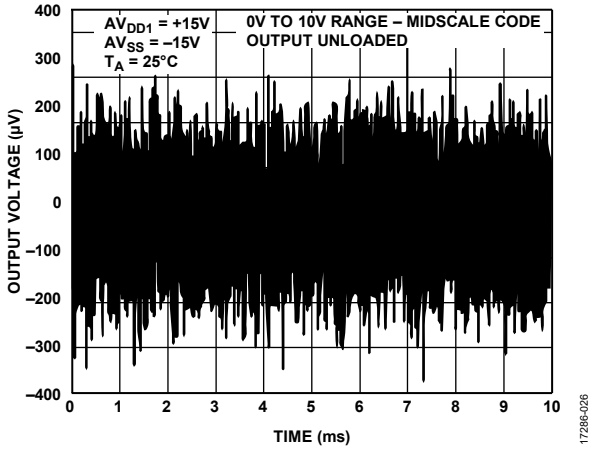


Figure 26. Peak-to-Peak Noise (100 kHz Bandwidth)

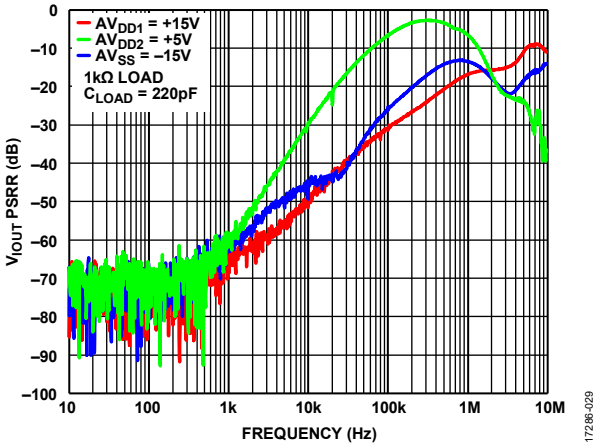


Figure 29. V_{OUT} PSRR vs. Frequency

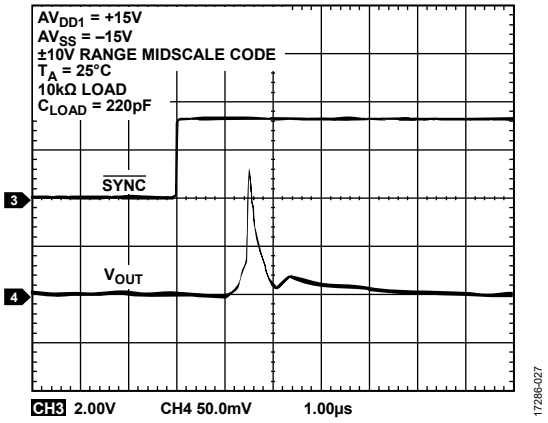


Figure 27. $\overline{SYNC}$ and V_{OUT} vs. Time on Output Enable

CURRENT OUTPUT

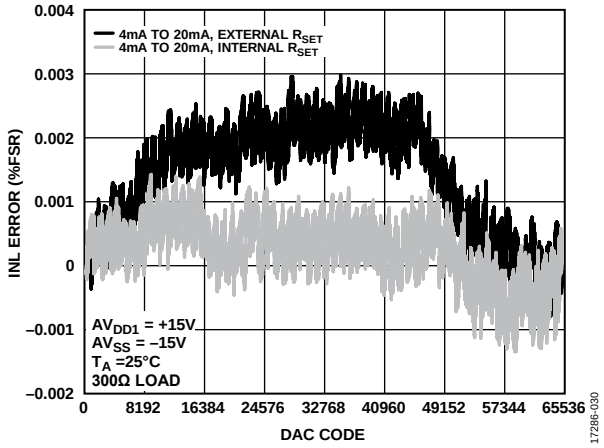


Figure 30. INL Error vs. DAC Code

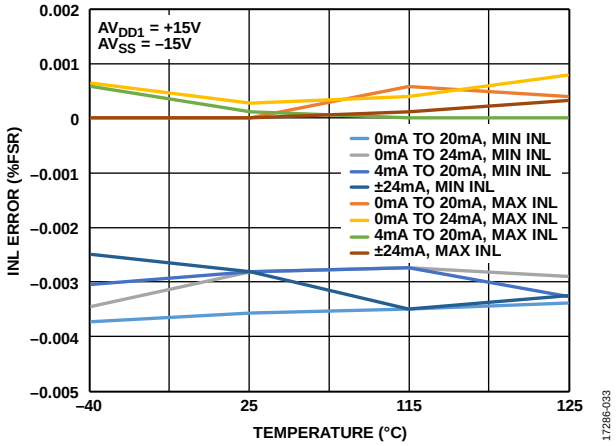


Figure 33. INL Error vs. Temperature, Internal R_{SET}

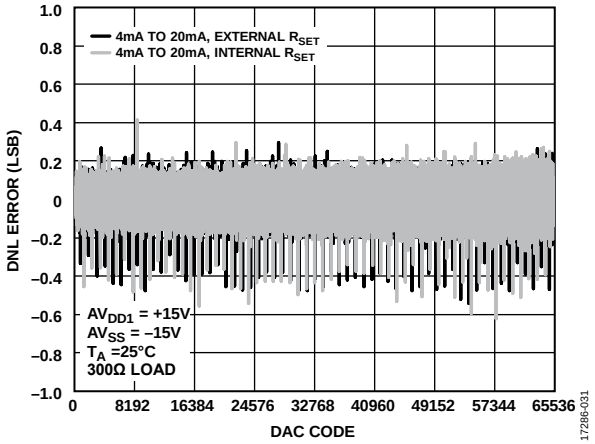


Figure 31. DNL Error vs. DAC Code

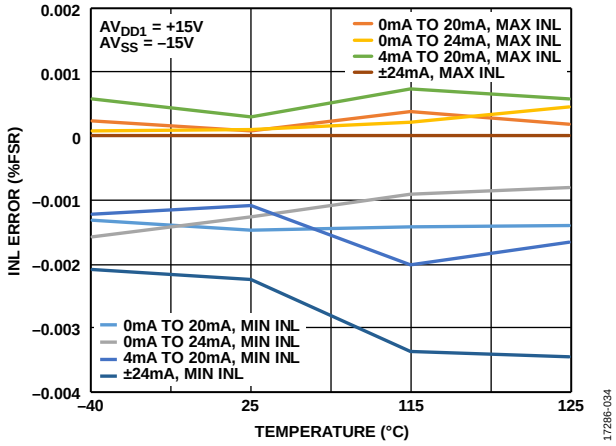


Figure 34. INL Error vs. Temperature, External R_{SET}

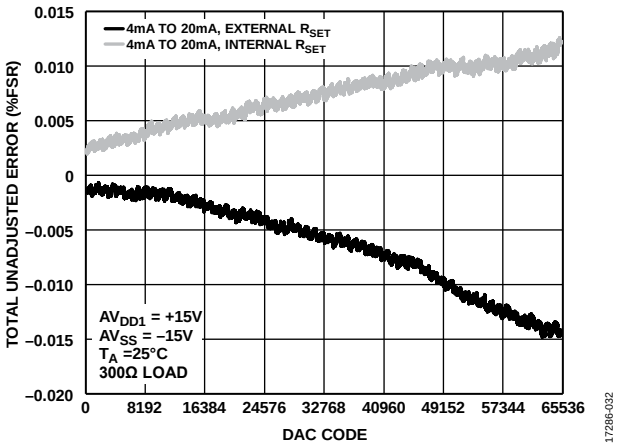


Figure 32. Total Unadjusted Error vs. DAC Code

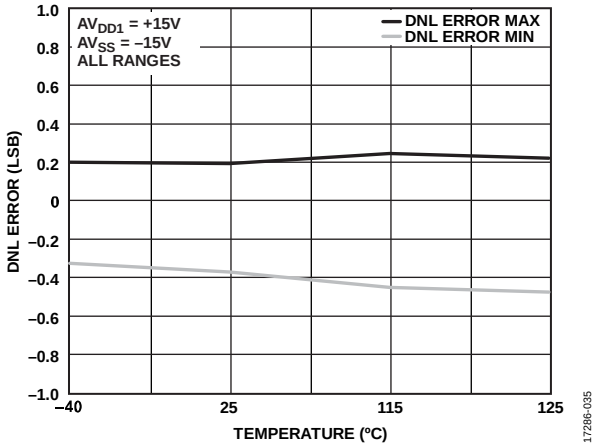


Figure 35. DNL Error vs. Temperature

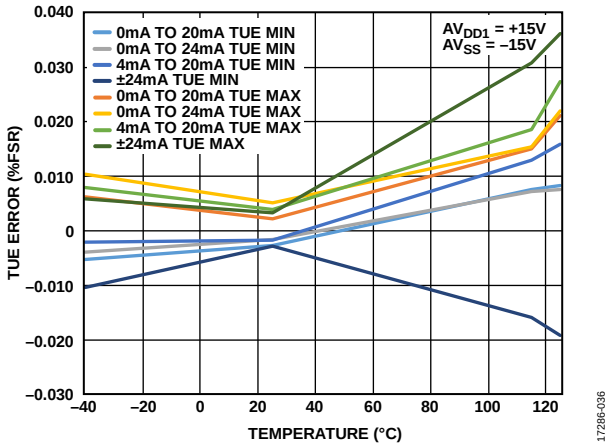


Figure 36. Total Unadjusted Error vs. Temperature, Internal R_{SET}

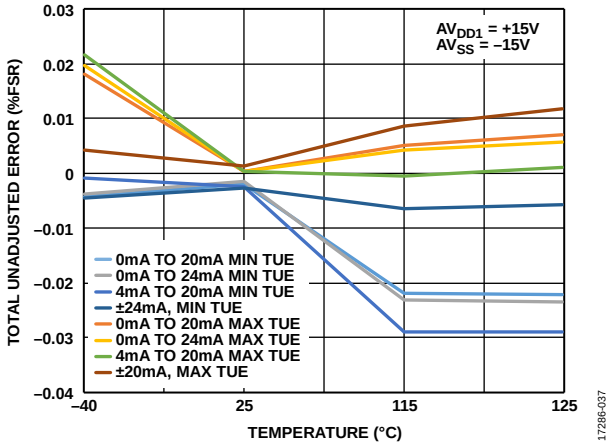


Figure 37. Total Unadjusted Error vs. Temperature, External R_{SET}

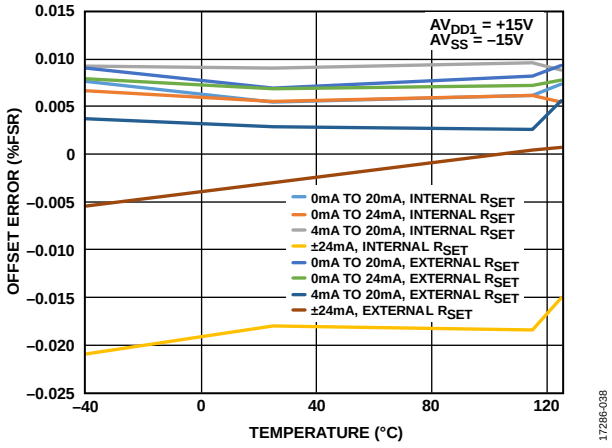


Figure 38. Offset Error vs. Temperature

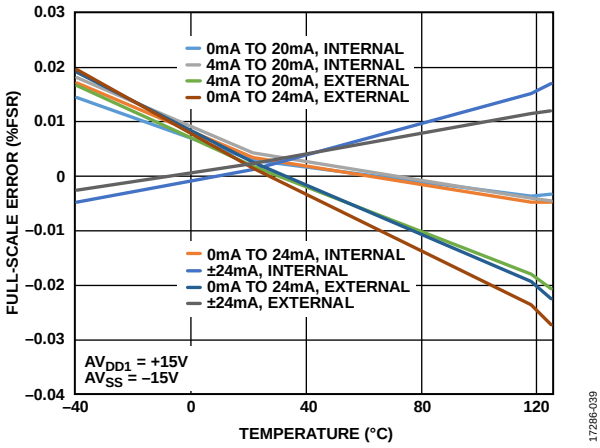


Figure 39. Full-Scale Error vs. Temperature

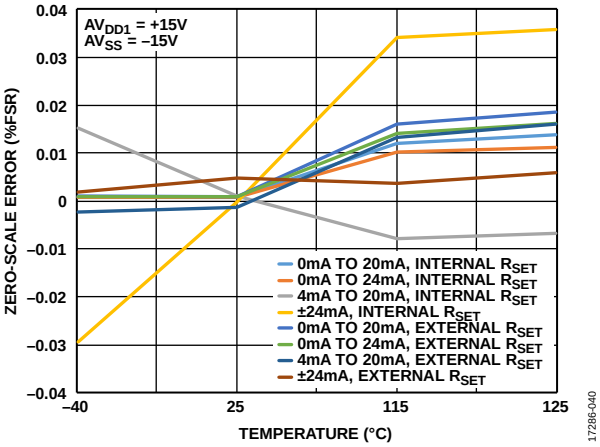


Figure 40. Zero-Scale Error vs. Temperature

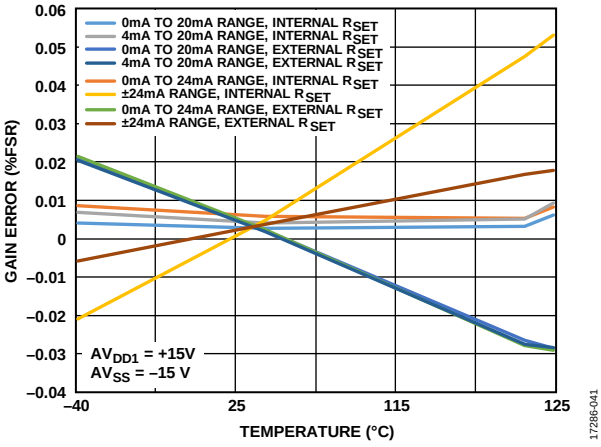


Figure 41. Gain Error vs. Temperature

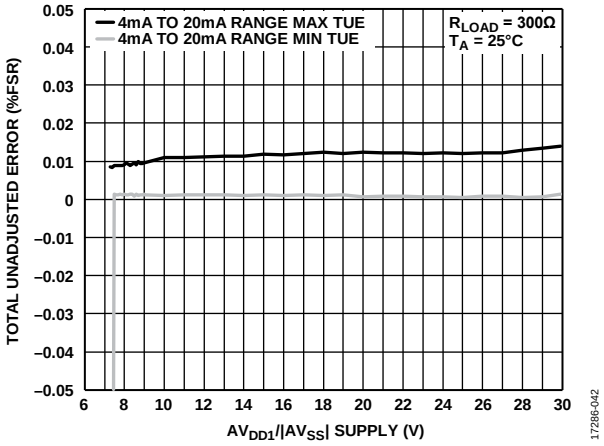


Figure 42. Total Unadjusted Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

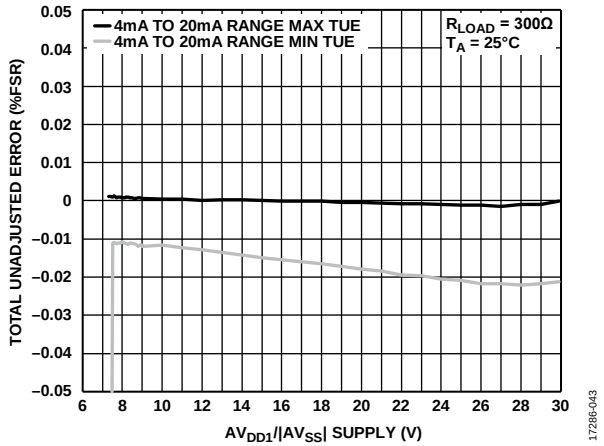


Figure 43. Total Unadjusted Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

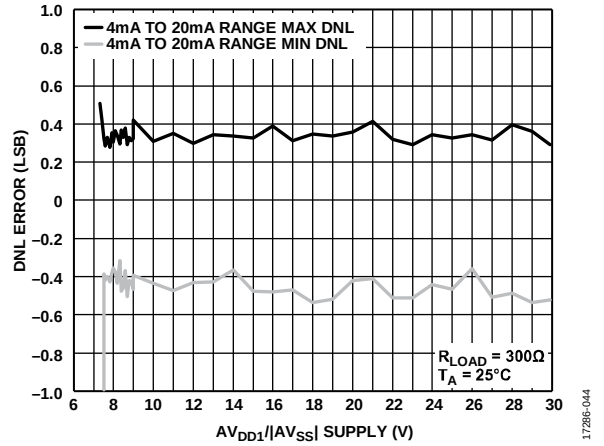


Figure 44. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

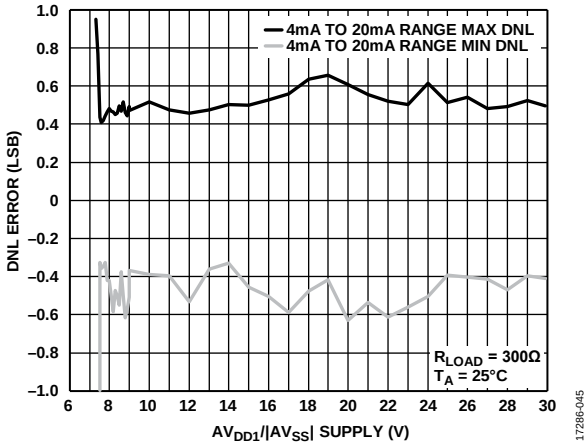


Figure 45. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

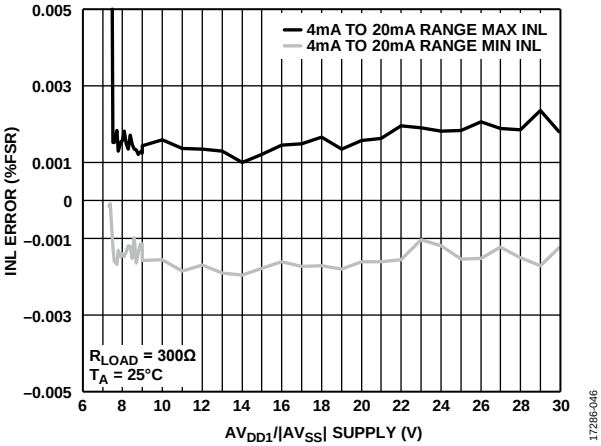


Figure 46. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

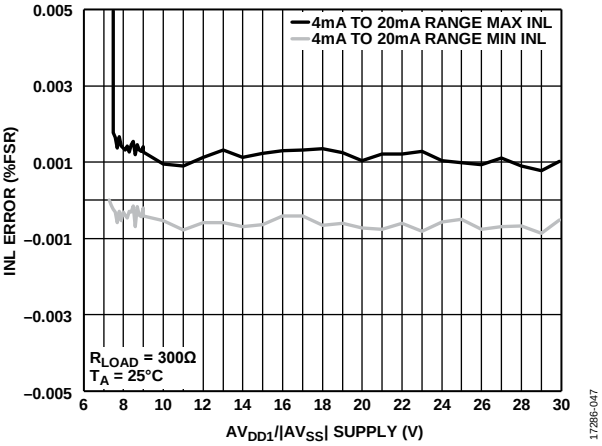


Figure 47. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

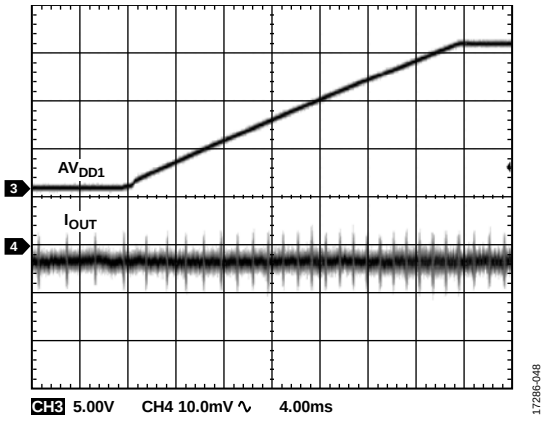


Figure 48. Output Current vs. Time on Power-Up

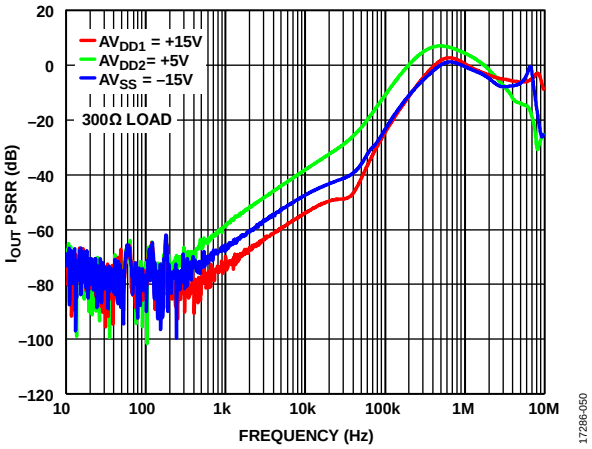


Figure 50. I_{OUT} PSRR vs. Frequency

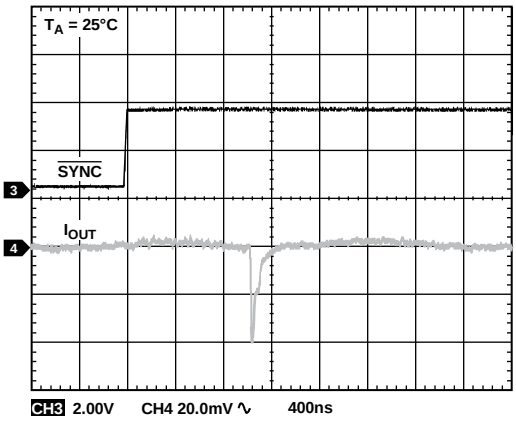


Figure 49. Output Current vs. Time on Output Enable

REFERENCE

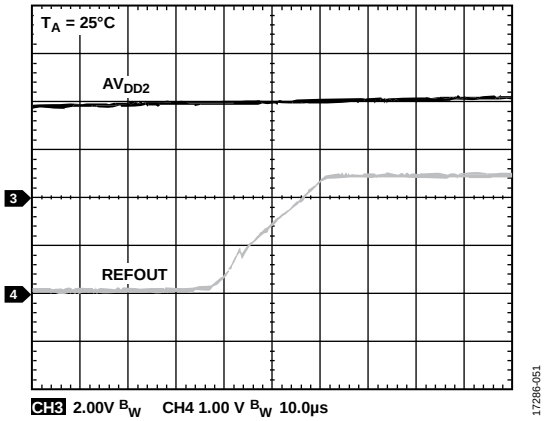


Figure 51. REFOUT Turn On Transient

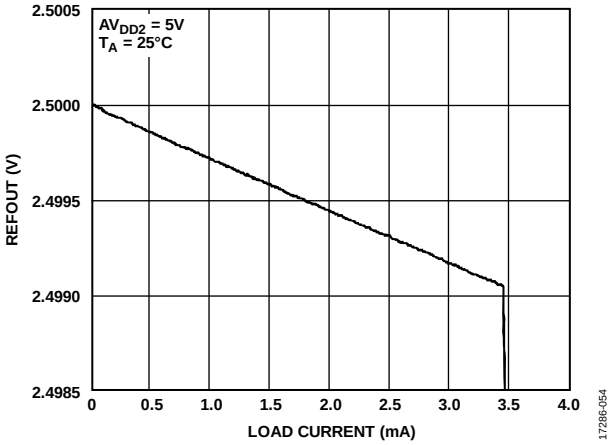


Figure 54. REFOUT vs. Load Current

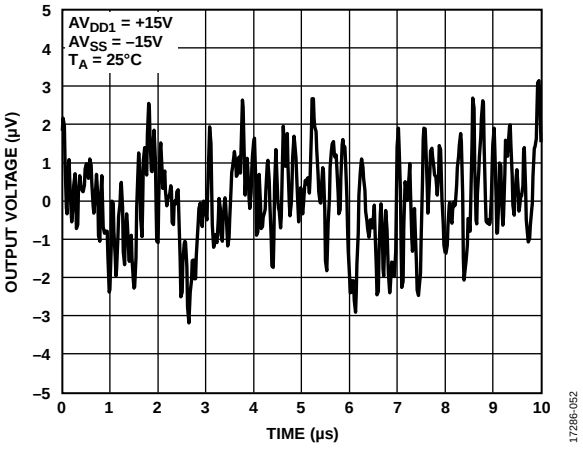


Figure 52. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

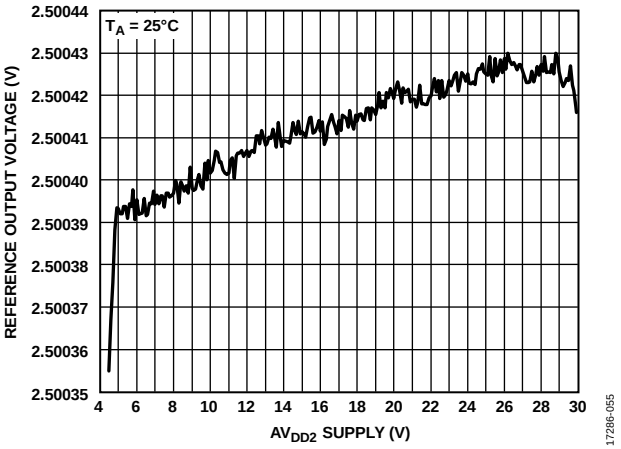


Figure 55. Reference Output Voltage vs. AV_{DD2} Supply

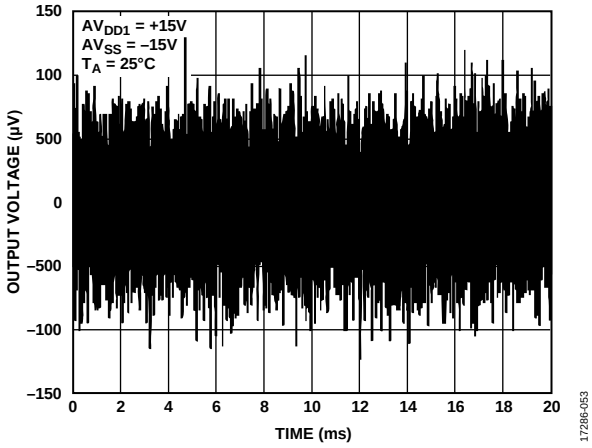


Figure 53. Peak-to-Peak Noise (100 kHz Bandwidth)

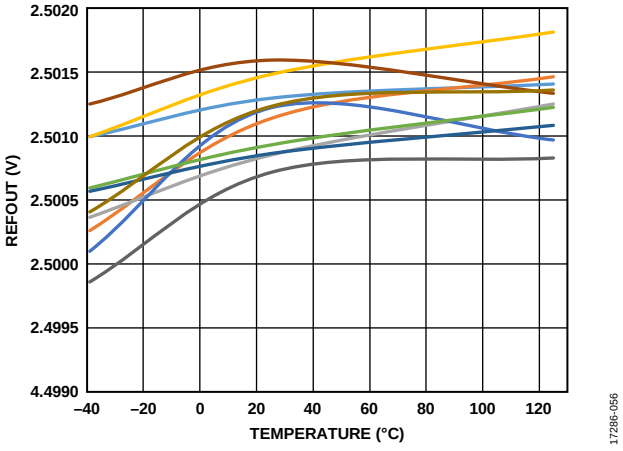


Figure 56. REFOUT vs. Temperature

GENERAL

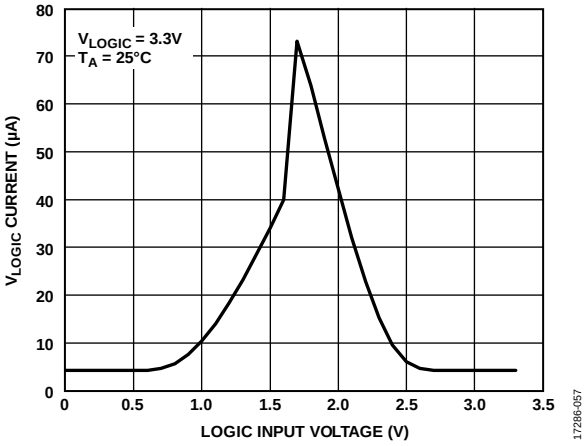


Figure 57. V_{LOGIC} Current vs. Logic Input Voltage

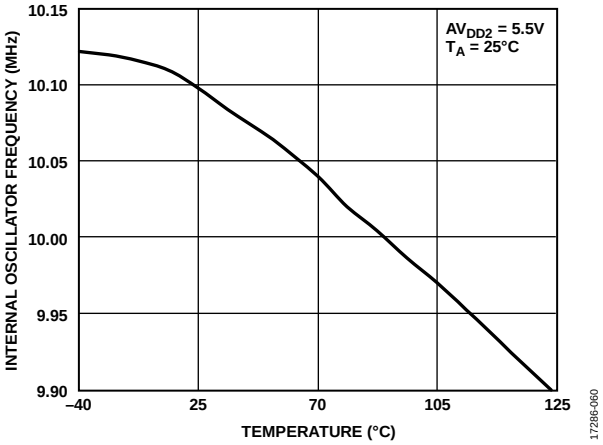


Figure 60. Internal Oscillator Frequency vs. Temperature

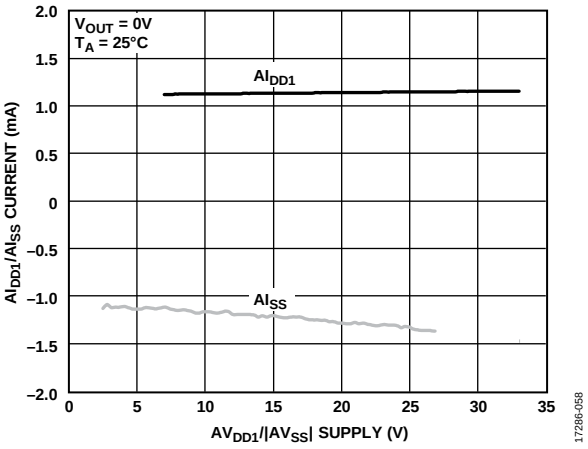


Figure 58. AI_{DD1}/AI_{SS} Current vs. $AV_{DD1}/|AV_{SS}|$ Supply

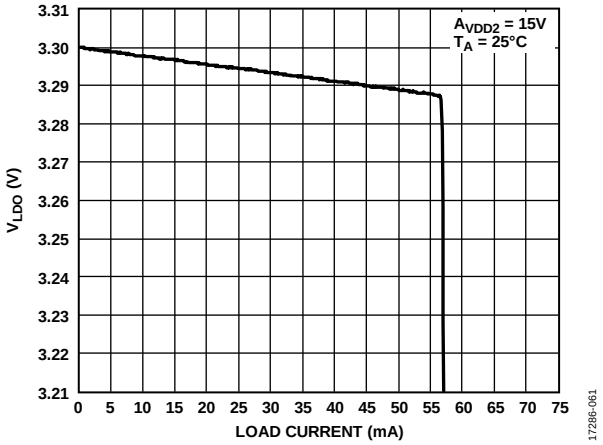


Figure 61. V_{LDO} vs. Load Current

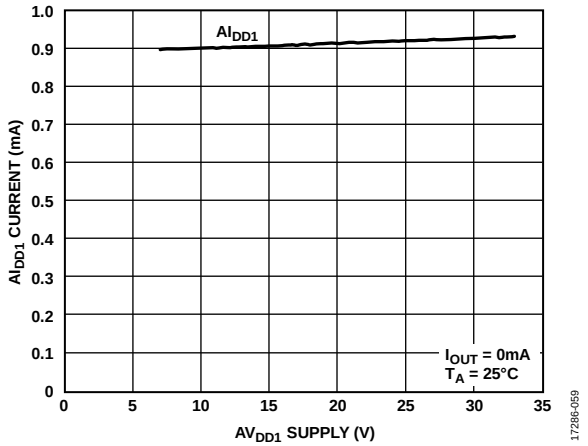


Figure 59. AI_{DD1} Current vs. AV_{DD1} Supply

TERMINOLOGY

Total Unadjusted Error (TUE)
TUE is a measure of the output error that takes into account various errors, such as INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, also known as INL, is a measure of the maximum deviation, either in LSBs or % FSR, from the best fit line passing through the DAC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5423 is monotonic over the full operating temperature range.

Zero-Scale or Negative Full-Scale Error
Zero-scale or negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC output register.

Zero-Scale Temperature Coefficient (TC)
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC output register is loaded with 0x8000 (straight binary coding).

Bipolar Zero TC
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. Bipolar zero TC is expressed in ppm FSR/°C.

Offset Error
Offset error is the deviation of the analog output from the ideal and is measured using ¼ scale and ¾ scale digital code measurements. Offset error is expressed in % FSR.

Offset Error TC
Offset error TC is a measure of the change in the offset error with a change in temperature. Offset error TC is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC. Gain error is the DAC transfer characteristic slope deviation from the ideal value expressed in % FSR.

Gain Error TC
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC output register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in % FSR.

V_{OUT} or $-V_{SENSE}$ Common-Mode Rejection Ratio (CMRR)
V_{OUT} or $-V_{SENSE}$ CMRR is the error in the V_{OUT} voltage that occurs due to changes in the $-V_{SENSE}$ voltage.

Current Loop Compliance Voltage
Current loop compliance voltage is the maximum voltage at the VI_{OUT} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +115°C and then back to +25°C.

Voltage Reference TC
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated by using the box method. This method defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C and is as follows:

$$TC = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF\_NOM} \times TemperatureRange} \right) \times 10^6$$

where:
V_{REF_MAX} is the maximum reference output measured over the total temperature range.
V_{REF_MIN} is the minimum reference output measured over the total temperature range.
V_{REF_NOM} is the nominal reference output voltage, 2.5 V.
Temperature Range is the specified temperature range, −40°C to +115°C.

Line Regulation
Line regulation is the change in reference output voltage due to a specified change in power supply voltage. Line regulation is expressed in ppm/V.

Load Regulation
Load regulation is the change in reference output voltage due to a specified change in reference load current. Load regulation is expressed in ppm/mA.

Output Voltage Settling Time
Output voltage settling time is the amount of time the output takes to settle to a specified level for a full-scale input change.

Slew Rate
The device slew rate is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output DAC is usually limited by the slew rate of the amplifier used at the output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/μs.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5423 is powered on. Power-on glitch energy is specified as the area of the glitch in nV-sec.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the energy of the impulse injected into the analog output when the input code in the DAC output register changes state. Digital-to-analog glitch energy is normally specified as the area of the glitch in nV-sec. The worst case of the glitch usually occurs when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC output register changes state. Glitch impulse peak amplitude is specified as the amplitude of the glitch in millivolts and the worst case of the glitch usually occurs when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the DAC analog output from the DAC digital inputs. However, the digital feedthrough is measured when the DAC output is not updated, which occurs when the $\overline{\text{LDAC}}$ pin is held high. The digital feedthrough is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

THEORY OF OPERATION

The AD5423 is a single-channel, precision voltage and current output DAC designed to meet the requirements of industrial factory automation and process control applications. The device provides a high precision, fully integrated, single-chip solution for generating a unipolar current, bipolar current, or voltage output.

DAC ARCHITECTURE

The DAC core architecture of the AD5423 consists of a voltage mode R-2R DAC ladder network. The voltage output of the DAC core is converted to either a current or voltage output at the VI_{OUT} pin. Only one mode can be enabled at any one time. Both the voltage and current output stages are supplied by the AV_{DD1} power rail and the AV_{SS} rail.

Current Output Mode

If current output mode is enabled, the voltage output from the DAC is converted to a current (see Figure 62), which is then mirrored to the supply rail so that the application only sees a current source output.

The available current ranges are 0 mA to 20 mA, 0 mA to 24 mA, 4 mA to 20 mA, ±20 mA, ±24 mA and −1 mA to +22 mA. An internal or external 13.7 kΩ R_{SET} resistor can be used for the voltage to current conversion.

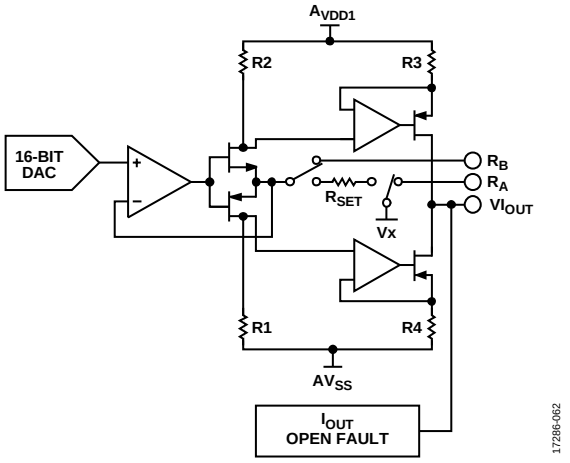


Figure 62. Voltage to Current Conversion Circuitry

Voltage Output Mode

If voltage output mode is enabled, the voltage output from the DAC is buffered and scaled to output a software-selectable unipolar or bipolar voltage range (see Figure 63).

The available voltage output ranges are 0 V to 5 V, ±5 V, 0 V to 10 V, and ±10 V. A 20% overrange feature is also available via the DAC_CONFIG register, as well as the feature to negatively offset the unipolar voltage ranges via the GP_CONFIG1 register (see the General-Purpose Configuration 1 Register section).

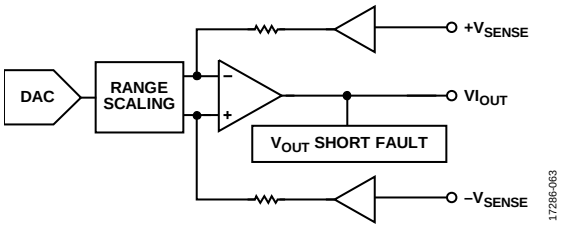


Figure 63. Voltage Output Architecture

Reference

The AD5423 can operate with either an external or internal reference. The reference input requires a 2.5 V reference for specified performance. This input voltage is then internally buffered before being applied to the DAC.

The AD5423 contains an integrated buffered 2.5 V voltage reference that is externally available for use elsewhere within the system. The internal reference drives the integrated 12-bit ADC. REFOUT must be connected to REFIN to use the internal reference to drive the DAC.

SERIAL INTERFACE

The AD5423 is controlled over a versatile 4-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

With the SPI CRC enabled (default state), the input shift register is 32 bits wide. Data is loaded to the device MSB first as a 32-bit word under the control of a serial clock input (SCLK). Data is clocked in on the falling edge of SCLK. If the CRC is disabled, the serial interface is reduced to 24 bits. A 32-bit frame is still accepted, but the last 8 bits are ignored. See the Register Map section for full details on the registers that can be addressed via the SPI interface.

Table 7. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip Bit	AD5423 address	Register address	Data	CRC

Transfer Function

Table 8 shows the input code to ideal output voltage relationship for the AD5423 for straight binary data coding of the ±5 V output range.

Table 8. Ideal Output Voltage to Input Code Relationship

Digital Input, Straight Binary Data Coding				Analog Output
MSB		LSB		V_{OUT}
1111	1111	1111	1111	$+2 \times V_{REF} \times (32{,}767/32{,}768)$
1111	1111	1111	1110	$+2 \times V_{REF} \times (32{,}766/32{,}768)$
1000	0000	0000	0000	0 V
0000	0000	0000	0001	$-2 \times V_{REF} \times (32{,}767/32{,}768)$
0000	0000	0000	0000	$-2 \times V_{REF}$

POWER-ON STATE OF THE AD5423

On initial power-on or a device reset of the AD5423, the voltage and current output channels are disabled. The switch connecting the VI_{OUT} via a 30 kΩ pull-down resistor to AGND is open. This switch can be enabled via the General-Purpose Configuration 1 Register section.

After device power-on, or a device reset, a calibration memory refresh command is required (see the Programming Sequence to Enable the Output section). It is recommended to wait a minimum of 500 µs after writing this command before writing further instructions to the device to allow time for internal calibrations to take place (see Figure 76).

Power-On Reset

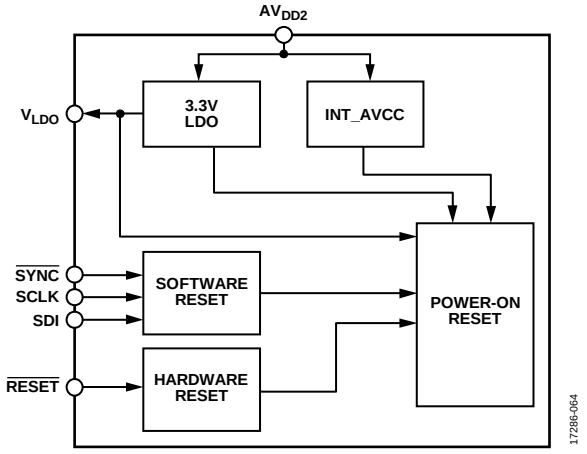


Figure 64. Power-On Reset Block Diagram

The AD5423 incorporates a power-on reset circuit that ensures that the AD5423 is held in reset if the power supplies are insufficient enough to allow reliable operation. The power-on reset circuit (see Figure 64) monitors the AV_{DD2} generated V_{LDO}, the INT_AVCC voltages, the $\overline{\text{RESET}}$ pin, and the SPI reset signal. The power-on reset circuit keeps the AD5423 in reset until the voltages on the V_{LDO} and the INT_AVCC nodes are sufficient for reliable operation. The AD5423 is reset if the power-on circuit receives a signal from the $\overline{\text{RESET}}$ pin or if a software reset is written to the AD5423 via the SPI interface. Do not write SPI commands to the device within 100 µs of a reset event.

POWER SUPPLY CONSIDERATIONS

The AD5423 has the following four supply rails: AV_{DD1}, AV_{DD2}, AV_{SS}, and V_{LOGIC}. See Table 1 for the voltage range of the four supply rails and the associated conditions.

AV_{DD1} Considerations

AV_{DD1} is the supply rail for the DAC and can range from 7 V to 33 V. Although the maximum value of AV_{DD1} is 33 V and the minimum value of AV_{SS} is −33 V, the maximum operating range of $|AV_{DD1}$ to $AV_{SS}|$ is 50 V. The minimum AV_{DD1} can be calculated as $(I_{OUT\_MAX} \times R_{LOAD}) + I_{OUT}$*_headroom*.

AV_{SS} Considerations

AV_{SS} is the negative supply rail and has a range of −33 V to 0 V. As in the case of AV_{DD1}, AV_{SS} must obey the maximum operating range of $|AV_{DD1}$ to $AV_{SS}|$ of 50 V. For the bipolar current output ranges, the maximum AV_{SS} can be calculated as $(I_{OUT\_MAX} \times R_{LOAD}) + I_{OUT}$*_footroom*.

AV_{DD2} Considerations

AV_{DD2} is the positive low voltage supply rail and has a range of 5 V to 33 V. If only one positive power rail is available, AV_{DD2} can be tied to AV_{DD1}. However, to optimize for reduced power dissipation, supply AV_{DD2} with a separate lower voltage supply.

V_{LOGIC} Considerations

V_{LOGIC} is the digital supply for the device and ranges from 1.71 V to 5.5 V. The 3.3 V V_{LDO} output voltage can be used to drive V_{LOGIC}.

DEVICE FEATURES AND DIAGNOSTICS

VOLTAGE OUTPUT

Voltage Output Amplifier and +V_{SENSE} Functionality

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. The amplifier is also capable of driving a 1 kΩ load in parallel with 2 µF with an external compensation capacitor to AGND.

Figure 65 shows the voltage output driving a load, R_{LOAD}, on top of a common-mode voltage (V_{CM}) of ±10 V. An integrated 2 MΩ resistor ensures that the amplifier loop is kept closed and prevents potentially large and destructive voltages on the VI_{OUT} due to the broken amplifier loop in applications where a cable can become disconnected from $+V_{SENSE}$. If remote sensing of the load is not required, connect $+V_{SENSE}$ directly to VI_{OUT} via the 1 kΩ series resistor and connect $-V_{SENSE}$ directly to AGND via the 1 kΩ series resistor.

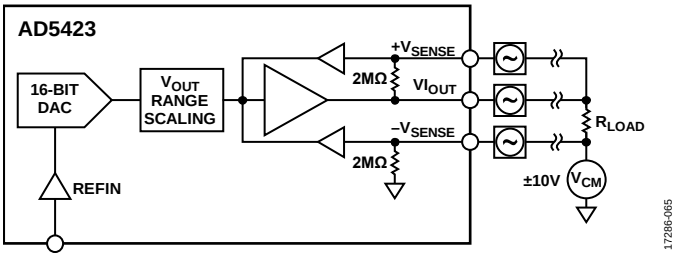


Figure 65. Voltage Output Load Connection

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 2 µF with the addition of a 220 pF nonpolarized compensation capacitor. This capacitor, though allowing the AD5423 to drive higher capacitive loads and reduce overshoot, increases the device settling time and, therefore, negatively affects the bandwidth of the system. Without the compensation capacitor, capacitive loads of up to 10 nF can be driven.

Voltage Output Short-Circuit Protection

Under normal operation, the voltage output sinks and sources up to 12 mA and maintains specified operation. The short-circuit current is typically 15 mA. If a short-circuit is detected, the $\overline{\text{FAULT}}$ pin goes low and the VOUT_SC_ERR bit in the ANALOG_DIAG_RESULTS register is set.

CURRENT OUTPUT

External Current Setting Resistor

As shown in Figure 62, R_{SET} is an internal sense resistor that forms part of the voltage to current conversion circuitry. The stability of the output current value overtemperature is dependent on the stability of the R_{SET} value. To improve the output current overtemperature stability, connect an external 13.7 kΩ, low drift resistor, instead of the internal resistor, between the R_A pin and R_B pin of the AD5423.

Table 1 shows the AD5423 performance specifications with both the internal R_{SET} resistor and an external 13.7 kΩ R_{SET} resistor. The external R_{SET} resistor specification assumes an ideal resistor. The actual performance depends on the absolute value and temperature coefficient of the resistor used. Therefore, the resistor specifications directly affect the gain error of the output and the TUE.

To arrive at the absolute worst case overall TUE of the output with a particular external R_{SET} resistor, add the percentage of the R_{SET} resistor absolute error (the absolute value of the error) to the TUE of the AD5423 that is using the RSET external resistor shown in Table 1 (expressed in % FSR). Consider the temperature coefficient as well as the specifications of the external reference if this is the option being used in the system.

The magnitude of the error, derived from summing the absolute error and the TC error of the external R_{SET} resistor and the external reference with the AD5423 TUE specification, is unlikely to occur because the TC values of the individual components are unlikely to exhibit the same drift polarity and, therefore, an element of cancelation occurs. For this reason, add the TC values with a root of squares method. A further improvement of the TUE specification is gained by performing a two point calibration at zero-scale and full-scale, thus reducing the absolute errors of the voltage reference and the R_{SET} resistor.

Current Output Open-Circuit Detection

When in current output mode, if the available headroom falls below the compliance range due to an open-loop circuit or an insufficient power supply voltage, the IOUT_OC_ERR bit flag in the ANALOG_DIAG_RESULTS register is asserted and the $\overline{\text{FAULT}}$ pin goes low.

HART CONNECTIVITY

The AD5423 has a C_{HART} pin on to which a HART signal can be coupled. The HART signal appears on the current output if the HART_EN bit in the GP_CONFIG1 register as well as the VI_{OUT} output are enabled.

Figure 66 shows the recommended circuit for attenuating and coupling the HART signal into the AD5423. To achieve 1 mA p-p at the VI_{OUT} pin, a signal of approximately 125 mV p-p is required at the C_{HART} pin. The HART signal on the VI_{OUT} pin is inverted relative to the signal input at the C_{HART} pin.

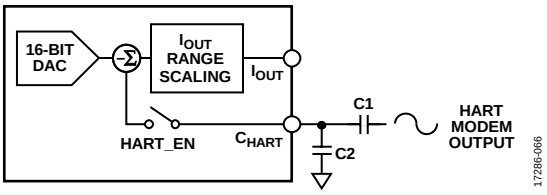


Figure 66. Coupling the HART Signal

As well as their use in attenuating the incoming HART modem signal, a minimum capacitance of the C1 and C2 capacitors is required to ensure that the bandwidth presented to the modem output signal allows the 1.2 kHz and 2.2 kHz frequencies through the capacitor. Assuming a HART signal of 500 mV p-p, the recommended values are C1 = 47 nF and C2 = 150 nF. Digitally controlling the output slew rate is necessary to meet the analog rate of change requirements for HART.

If the HART feature is not required, disable the HART_EN bit and leave the C_{HART} pin open circuit. However, if the DAC output signal must be slowed with a capacitor, the HART_EN bit must be enabled and the required C_{SLEW} capacitor must be connected to the C_{HART} pin.

DIGITAL SLEW RATE CONTROL

The AD5423 slew rate control feature allows the user to control the rate at which the output value changes. This feature is available in both current mode and voltage mode. Disabling the slew rate control feature changes the output value at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, enable the slew rate control feature. Enabling this feature causes the output to digitally step from one output value to the next at a rate defined by two parameters accessible via the DAC_CONFIG register. These two parameters are SR_CLOCK and SR_STEP. SR_CLOCK and the parameters define the rate at which the digital slew is updated. For example, if the selected update rate is 8 kHz, the output updates every 125 µs. In conjunction with SR_CLOCK, SR_STEP defines by how much the output value changes at each update. Together, both parameters define the rate of change of the output value. The following equation describes the slew rate as a function of the step size, the slew rate frequency, and the LSB size:

$$SlewTime = \frac{OutputChange}{StepSize \times SlewRateFrequency \times LSBSize}$$

where:
Slew Time is expressed in seconds.
Output Change is expressed in amps for current output mode or volts for voltage output mode.
Step Size is the change in output.
Slew Rate Frequency is SR_CLOCK.
LSB Size is SR_STEP.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate. For example, if the WDT times out and an automatic clear occurs, the output slews to the clear value at the programmed slew rate. However, setting the CLEAR_NOW_EN bit in the GP_CONFIG1 register overrides this default behavior and causes the output to immediately update to the clear code, rather than at the programmed slew rate.

The slew rate frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

AD5423 ADDRESS PINS

The AD5423 address pins (AD0 and AD1) are used in conjunction with the AD5423 address bits within the SPI frame (Table 9) to determine which AD5423 device is being addressed by the system controller. With the two address pins, up to four devices can be independently addressed on one board.

SPI INTERFACE AND DIAGNOSTICS

The AD5423 is controlled over a 4-wire serial interface with an 8-bit cyclic redundancy check (CRC-8) that is enabled by default. The input shift register is 32 bits wide and data is loaded into the device MSB first under the control of a serial clock input (SCLK). Data is clocked in on the falling edge of SCLK. If CRC is disabled, the serial interface is reduced to 24 bits. A 32-bit frame is still accepted, but the last 8 bits are ignored.

Table 9. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip Bit	AD5423 address	Register address	Data	CRC

As shown in Table 9, every SPI frame contains two AD5423 address bits. These bits must match the AD0 pin and AD1 pin for a particular device to accept the SPI frame on the bus.

SPI Cyclic Redundancy Check

To verify that data is correctly received in noisy environments, the AD5423 offers a CRC based on a CRC-8. The device, either a micro or a field-programmable gate array (FPGA), controlling the AD5423 generates an 8-bit frame check sequence by using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This 8-bit frame check sequence is added to the end of the data-word, and 32 bits are sent to the AD5423 before pulling $\overline{SYNC}$ high.

If the SPI_CRC_EN bit is set high (default state), the user must supply a frame that is exactly 32 bits wide that contains the 24 data bits and the 8-bit CRC. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the $\overline{FAULT}$ pin goes low, and the $\overline{FAULT}$ pin status bit and the

digital diagnostic status bit (DIG_DIAG_STATUS) in the status register are asserted. A subsequent readback of the DIGITAL_DIAG_RESULTS register shows that the SPI_CRC_ERR bit is also set. This register is per individual bits, a write one per bit clears the register (see the Sticky Diagnostic Results Bits section for more details). Therefore, the SPI_CRC_ERR bit is cleared by writing a 1 to Bit 0 of the DIGITAL_DIAG_RESULTS register. Writing a 1 clears the SPI_CRC_ERR bit and causes the $\overline{\text{FAULT}}$ pin to return high, assuming that there are no other active faults. When configuring the FAULT_PIN_CONFIG register, the user decides whether the SPI CRC error affects the $\overline{\text{FAULT}}$ pin. See the $\overline{\text{FAULT}}$ Pin Configuration Register section for further details. The SPI CRC feature is used for both transmitting and receiving data packets.

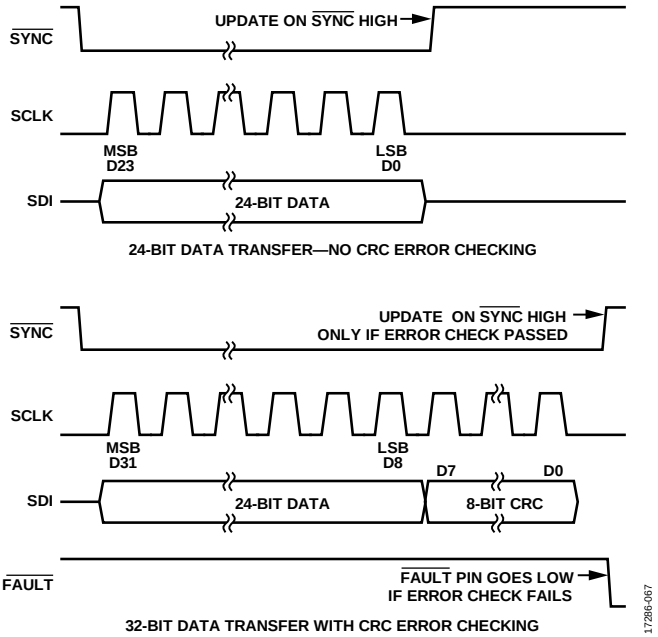


Figure 67. CRC Timing (Assume $\overline{\text{LDAC}}$ = 0)

SPI Interface Slip Bit

Adding the slip bit enhances the interface robustness. The MSB of the SPI frame must equal the inverse of MSB − 1 for the frame to be considered valid. If an incorrect slip bit is detected, the data is ignored and the SLIPBIT_ERR bit in the DIGITAL_DIAG_RESULTS register is asserted.

SPI Interface SCLK Count Feature

An SCLK count feature is also built into the SPI diagnostics, meaning that only SPI frames with exactly 32 SCLK falling edges (24 or 32 if SPI CRC is enabled) are accepted by the interface as a valid write. SPI frame lengths other than 32 are ignored and the SCLK_COUNT_ERR flag asserts in the DIGITAL_DIAG_RESULTS register.

Readback Modes

The AD5423 offers the following four readback modes:

- Two-stage readback mode
- Autostatus readback mode
- Shared $\overline{\text{SYNC}}$ autostatus readback mode
- Echo mode

The two-stage readback consists of a write to a dedicated register, TWO_STAGE_READBACK_SELECT, to select the register location to be read back. This write is followed by a no operation (NOP) command, during which the contents of the selected register are available on the SDO pin.

Table 10. SDO Contents for Read Operation

MSB				LSB
[D31:D30]	**D29**	**[D28:24]**	**[D23:D8]**	**[D7:D0]**
0b10	$\overline{\text{FAULT}}$ pin status	Register address	Data	CRC

Bits[D31:D30] = 0b10 are used for synchronization purposes during readback.

If autostatus readback mode is selected, the contents of the status register are available on the SDO line during every SPI transaction. This feature allows the user to continuously monitor the status register and to act quickly if a fault occurs. The AD5423 powers up with this feature disabled. When this feature is enabled, the normal two-stage readback feature is not available. Only the status register is available on the SDO when autostatus readback mode is selected. To read back other registers, first disable the automatic readback feature before following the two-stage readback sequence. The automatic status readback can be re-enabled after the register is read back.

The shared AD5423 $\overline{\text{SYNC}}$ autostatus readback is a special version of the autostatus readback mode used to avoid SDO bus contention when multiple devices share the same $\overline{\text{SYNC}}$ line. See the Shared $\overline{\text{SYNC}}$ Autostatus Readback Mode section for more details.

Echo mode behaves similarly to autostatus readback mode, except that every second readback consists of an echo of the previous command written to the AD5423 (see Figure 68). See the Reading from Registers section for further details on the readback modes.

Figure 68. SDO Contents, Echo Mode

WDT

The WDT feature ensures that communication is not lost between the system controller and the AD5423, and that the SPI datapath lines function as expected.

When enabled, the WDT alerts the system if the AD5423 has not received a specific SPI frame in the user programmable timeout period. When the specific SPI frame is received, the WDT resets the timer controlling the timeout alert. The SPI frame used to reset the WDT is configurable as one of the two following choices:

- A specific key code write to the key register (default).
- A valid SPI write to any register.

When a WDT timeout event occurs, a dedicated WDT_STATUS bit in the status register, as well as a WDT_ERR bit in the DIGITAL_DIAG_RESULTS register, alerts the user that the WDT is timed out. After a WDT timeout occurs, all writes to the DAC_INPUT register, as well as the hardware or software $\overline{\text{LDAC}}$ events, are ignored until the active WDT fault flag within the DIGITAL_DIAG_RESULTS register clears. After this flag clears, the WDT restarts by performing a subsequent WDT reset command.

On power-up, the WDT is disabled by default. The default timeout setting is 1 second. The default method to reset the WDT is to write one specific key. On timeout, the default action is to set the relevant WDT_ERR flag bits and the $\overline{\text{FAULT}}$ pin. See Table 34 for the specific register bit details to support the configurability of the WDT operation.

USER DIGITAL OFFSET AND GAIN CONTROL

The AD5423 has a USER_GAIN register and a USER_OFFSET register that trim the gain and offset errors from the entire signal chain. The USER_GAIN register allows the user to adjust the gain of the DAC channel in steps of 1 LSB. The USER_GAIN register coding is straight binary, as shown in Table 11. The default code in the USER_GAIN register is 0xFFFF, which results in a no gain factor applied to the programmed output. In theory, the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy.

Table 11. Gain Register Adjustment

Gain Adjustment Factor	D15	D14 to D1	D0
1	1	1	1
65,535/65,536	1	1	0
…	…	…	…
2/65,536	0	0	1
1/65,536	0	0	0

The USER_OFFSET register allows the user to adjust the offset of the DAC channel from −32,768 LSBs to +32,768 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary, as shown in Table 12. The default code in the USER_OFFSET register is 0x8000, which results in zero offset programmed to the output.

Table 12. Offset Register Adjustment

Gain Adjustment	D15	[D13 to D2]	D0
+32,768 LSBs	1	1	1
+32,767 LSBs	1	1	0
No Adjustment (Default)	1	0	0
−32,767 LSBs	0	0	1
−32,768 LSBs	0	0	0

The decimal value that is written to the internal DAC register, *DAC_Code*, is calculated with the following equation:

$$DAC\_Code = D \times \frac{(M+1)}{2^{16}} + C - 2^{15}$$

where:
D is the code loaded to the DAC_INPUT register.
M is the code in the USER_GAIN register (default code = $2^{16} - 1$).
C is the code in the USER_OFFSET register (default code = 2^{15}).

Data from the DAC_INPUT register is processed by a digital multiplier and adder and both are controlled by the contents of the USER_GAIN register and USER_OFFSET register respectively. The calibrated DAC data is then loaded to the DAC. The loading of the DAC data is dependent on the state of the $\overline{\text{LDAC}}$ pin.

Each time data is written to the USER_GAIN register or USER_OFFSET register, the DAC output is not automatically updated. Instead, the next write to the DAC_INPUT register uses these user gain and user offset values to perform a new calibration and to automatically update the output channel. The read only DAC_OUTPUT register represents the value currently available at the DAC output, except in the case of user gain and user offset calibration. In this case, the DAC_OUTPUT register contains the DAC data input by the user, on which the calibration is performed and not the result of the calibration.

Both the USER_GAIN register and the USER_OFFSET register have 16 bits of resolution. The correct method to calibrate the gain and offset is to first calibrate the gain and then calibrate the offset.

DAC OUTPUT UPDATE AND DATA INTEGRITY DIAGNOSTICS

Figure 69 shows a simplified version of the DAC input loading circuitry. If the gain and offset are used, the USER_GAIN register and USER_OFFSET register must be updated before writing to the DAC_INPUT register.

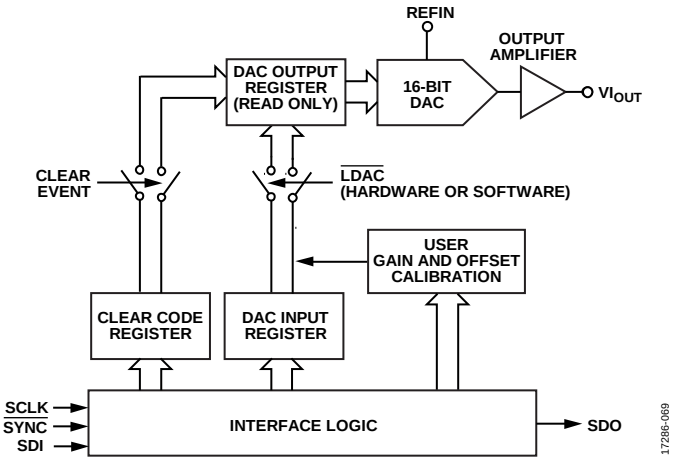


Figure 69. Simplified Serial Interface of Input Loading Circuitry

The DAC_OUTPUT register, and ultimately the DAC output, updates in any of the following cases:

- If a write is performed to the DAC_INPUT register with the hardware LDAC pin tied low, the DAC_OUTPUT register is updated on the rising edge of SYNC and is subject to the timing specifications in Table 2.
- If the hardware LDAC pin is tied high and the DAC_INPUT register is written to, the DAC_OUTPUT register does not update until a software LDAC instruction is issued or the hardware LDAC pin is pulsed low.
- If a WDT timeout occurs with the CLEAR_ON_WDT_FAIL bit set, the CLEAR_CODE register contents are loaded into the DAC_OUTPUT register.
- If the slew rate control feature is enabled, the DAC_OUTPUT register contains the dynamic value of the DAC as the register slews between values.

While a WDT fault is active, all writes to the DAC_INPUT register, as well as hardware or software LDAC events, are ignored. If the CLEAR_ON_WDT_FAIL bit is set such that the output is set to the clear code, after the WDT fault flag clears, the DAC_INPUT register must be written to before the DAC_OUTPUT register updates. The DAC_INPUT register must be written to because performing a software or hardware LDAC only reloads the DAC with the clear code. As described in the Programming Sequence to Enable the Output section, after configuring the DAC range via the DAC_CONFIG register, the DAC_INPUT register must be written to even if the contents of the DAC_INPUT register are not changing from the current value.

The GP_CONFIG2 register contains a bit to enable a global software, LDAC active low mode that ignores the AD5423 address bits of the SW_LDAC command, thus enabling multiple AD5423 devices to be simultaneously updated by using a single SW_LDAC command. This feature is useful if the hardware LDAC pin is not being used in a system containing multiple AD5423 devices.

DAC Data Integrity Diagnostics

To protect against transient changes to the internal digital circuitry, the digital block stores both the digital DAC value and an inverted copy of the digital DAC value. A check is completed to ensure that the two values correspond to each other before the DAC is strobed to update to the DAC code. This matching feature is enabled by default via the INVERSE_DAC_CHECK_EN bit in the DIGITAL_DIAG_CONFIG register.

Outside of the digital block, the DAC code is stored in latches, as shown in Figure 70. These latches are potentially vulnerable to the same transient events that affect the digital block. To protect the DAC latches against such transients, enable the DAC latch monitor feature via the DAC_LATCH_MON_EN bit within the DIGITAL_DIAG_CONFIG register. This latch monitor feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes sets the DAC_LATCH_MON_ERR bit flag in the DIGITAL_DIAG_RESULTS register.

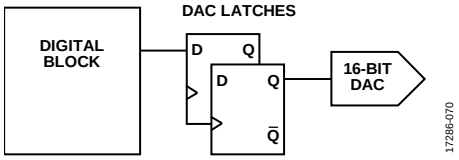


Figure 70. DAC Data Integrity

USE OF KEY CODES

Key codes are used via the key register for the following functions (see the Key Register section for full details):

- Initiating calibration memory refresh
- Initiating a software reset
- WDT reset key

Using specific keys to initiate actions such as a calibration memory refresh or a device reset provides extra system robustness because the keys reduce the probability of either task being initiated in error.

SOFTWARE RESET

A software reset requires two consecutive writes of 0x15FA and 0xAF51, respectively, to the key register. A device reset can be initiated via the hardware RESET pin, the software reset keys, or automatically after a WDT timeout (if configured to do so). The RESET_OCCURRED bit in the DIGITAL_DIAG_RESULTS register is set when the device is reset. This bit defaults to 1 on power-up. Both of the diagnostic results registers implement a write 1 to clear the function. That is, a 1 must be written to this bit to clear it (see the Sticky Diagnostic Results Bits section).

CALIBRATION MEMORY CRC

For every calibration memory refresh cycle, which is either initiated via a key code write to the key register or automatically initiated when the RANGE bits (Bits[3:0]) of the DAC_CONFIG register are changed, an automatic CRC is calculated on the contents of the calibration memory shadow registers. The result of this CRC is compared with the factory stored reference CRC value. If the CRC values match, the read of the entire calibration memory is considered valid. If the values do not match, the CAL_MEM_CRC_ERR bit in the DIGITAL_DIAG_RESULTS register is set to 1. This calibration memory CRC feature is enabled by default and can be disabled via the CAL_MEM_CRC_EN bit in the DIGITAL_DIAG_CONFIG register.

Two-stage readback commands are permitted while this calibration memory refresh cycle is active, but a write to any register other than the TWO_STAGE_READBACK_SELECT register or the NOP register sets the INVALID_SPI_ACCESS_ERR bit in the DIGITAL_DIAG_RESULTS register. As described in the Programming Sequence to Enable the Output section, a wait period of 500 µs is recommended after a calibration memory refresh cycle is initiated.

INTERNAL OSCILLATOR DIAGNOSTICS

An internal frequency monitor uses the internal oscillator (MCLK) to increment a 16-bit counter at a rate of 1 kHz (MCLK/10,000). The counter value can be read in the FREQ_MONITOR register. The user can poll this register periodically and use it as a diagnostic tool for the internal oscillator (to monitor that the oscillator is running) and to measure the oscillator frequency. This counter feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register.

If the MCLK oscillator stops, the AD5423 sends a specific code of 0x07DEAD to the SDO line for every SPI frame. This oscillator dead code feature is enabled by default and is disabled by clearing the OSC_STOP_DETECT_EN bit in the GP_CONFIG1 register. This feature is limited to the maximum readback timing specifications as described in Table 3.

STICKY DIAGNOSTIC RESULTS BITS

The AD5423 contains the following two diagnostic results registers: digital and analog (see Table 39 and Table 40, respectively, for the diagnostic error bits). The diagnostic results bits contained within these registers are sticky (R/W-1-C), that is, each bit needs a 1 to be written to it to clear the error bit. However, if the fault is still present, even after writing a 1 to the bit in question, the error bit does not clear to 0. Upon writing Logic 1 to the bit, the bit updates to the latest value, which is Logic 1 if the fault is still present and Logic 0 if the fault is no longer present.

These are the two following exceptions to this R/W-1-C access within the DIGITAL_DIAG_RESULTS register: CAL_MEM_UNREFRESHED and SLEW_BUSY. These bits automatically clear when the calibration memory refreshes or the output slew is complete.

The status register contains a DIG_DIAG_STATUS bit and ANA_DIAG_STATUS bit, and both bits are the result of a logical OR of the diagnostic results bits contained in each of the diagnostic results registers. All analog diagnostic flag bits are included in the logical OR of the ANA_DIAG_STATUS bit, and all digital diagnostic flag bits, with the exception of the SLEW_BUSY bit, are included in the logical OR of the DIG_DIAG_STATUS bit. The OR'ed bits within the status register are read only and not sticky (R/W-1-C).

BACKGROUND SUPPLY AND TEMPERATURE MONITORING

Excessive die temperature and overvoltage are known to be related to common cause failures. These conditions, therefore, can be monitored in a continuous fashion by using comparators, which eliminates the requirement to poll the ADC.

The die has a built-in temperature sensor with a ±5°C accuracy. The die temperature is monitored by a comparator and the background temperature comparators are permanently enabled. Programmable trip points corresponding to 142°C, 127°C, 112°C, and 97°C can be configured in the GP_CONFIG1 register. If the temperature of either die exceeds the programmed limit, the relevant status bit in the ANALOG_DIAG_RESULTS register is set and the $\overline{\text{FAULT}}$ pin is asserted low.

The low voltage supplies on the AD5423 are monitored via low power static comparators. This monitoring function is disabled by default and is enabled via the COMPARATOR_CONFIG bits in the GP_CONFIG2 register. The INT_EN bit in the DAC_CONFIG register must be set for the REFIN buffer to be powered up and for this node to be available to the REFIN comparator. The monitored nodes are REFIN, REFOUT, V_{LDO}, and an internal AV_{CC} voltage node (INT_AVCC). There is a status bit in the ANALOG_DIAG_RESULTS register that corresponds to each monitored node. If any of the monitored node supplies exceed the upper or lower threshold values (see Table 13 for the threshold values), the corresponding status bit is set. Note that if a REFOUT fault occurs, the REFOUT_ERR status bit is set. The INT_AVCC, V_{LDO}, and temperature comparator status bits can then also be set because REFOUT is used as the comparison voltage for these nodes. Like all the other status bits in the ANALOG_DIAG_RESULTS register, these bits are sticky and need a 1 to be written to them to clear them, assuming that the error condition is subsided. If the error condition is still present, the flag remains high even after a 1 is written to clear it.

Table 13. Comparator Supply Activation Thresholds

Supply	Lower Threshold (V)	Nominal Value/Range (V)	Upper Threshold (V)
INT_AVCC	3.8	4 to 5	5.2
VLDO	2.8	3 to 3.6	3.8
REFIN	2.24	2.5	2.83
REFOUT	2.24	2.5	2.83

OUTPUT FAULT

The AD5423 is equipped with a $\overline{\text{FAULT}}$ pin. This pin is an active low, open-drain output that connects several AD5423 devices together to one pull-up resistor for global fault detection. This pin is high impedance when no faults are detected and is asserted low when certain faults such as an open circuit in current mode, a short-circuit in voltage mode, a CRC error, or an overtemperature error are detected. Table 14 shows the fault conditions that automatically force the $\overline{\text{FAULT}}$ pin active and highlights the user-maskable fault bits available via the FAULT_PIN_CONFIG register (see Table 37). All registers contain a corresponding $\overline{\text{FAULT}}$ pin status bit, FAULT_PIN_STATUS, that mirrors the inverted current state of the $\overline{\text{FAULT}}$ pin.

Table 14. $\overline{\text{FAULT}}$ Pin Trigger Sources.

Fault Type	Mapped to $\overline{\text{FAULT}}$ Pin	Mask Ability
Digital Diagnostic Faults		
Oscillator Stop Detect	Yes	Yes
Calibration Memory Not Refreshed	No	N/A[2]
Reset Detected	No	N/A[2]
WDT Error	Yes	Yes
DAC Latch Monitor Error	Yes	Yes
Inverse DAC Check Error	Yes	Yes
Calibration Memory CRC Error	Yes	No
Invalid SPI Access	Yes	Yes
SCLK Count Error	Yes	No[1]
Slip Bit Error	Yes	Yes
SPI CRC Error	Yes	Yes
Analog Diagnostic Faults		
Current Output Open Circuit Error	Yes	Yes
Voltage Output Short Circuit Error	Yes	Yes
Die Temperature Error	Yes	Yes
REFOUT Comparator Error	Yes	No
REFIN Comparator Error	Yes	No
INT_AVCC Comparator Error	Yes	No
V_{LDO} Comparator Error	Yes	No

[1] Although the SCLK count error cannot be masked in the FAULT_PIN_CONFIG register, it can be excluded from the $\overline{\text{FAULT}}$ pin by enabling the SPI_DIAG_QUIET_EN bit (Bit 3) in the GP_CONFIG1 register).
[2] Not applicable.

The DIG_DIAG_STATUS bit, ANA_DIAG_STATUS bit, and WDT_STATUS bit of the status register are used in conjunction with the $\overline{\text{FAULT}}$ pin and the FAULT_PIN_STATUS bit to inform the user which fault condition is causing the $\overline{\text{FAULT}}$ pin to activate or a FAULT_PIN_STATUS bit to activate.

ADC MONITORING

The AD5423 incorporates a 12-bit ADC to provide diagnostic information on user-selectable inputs such as supplies, grounds, internal die temperatures, and references. See Table 15 for a full list of these selectable inputs. The ADC reference is derived from REFOUT and provides independence from the DAC reference (REFIN) if necessary. The ADC_CONFIG register configures the selection of the multiplexed ADC input channel via the ADC_IP_SELECT bits (see Table 36).

Summary of ADC Input Nodes

Table 15 contains a summary of all possible nodes that can be digitized by the ADC and their corresponding transfer function equations.

Table 15. ADC Input Node Summary

ADC_IP_SELECT	V_{IN} Node Description	ADC Transfer Function
00000	Die temperature	T (°C) = (−0.09369 × D) + 307
00001	Reserved	Reserved
00010	Reserved	Reserved
00011	REFIN	REFIN (V) = (D/2^{12}) × 2.75
00100	Internal 1.23 V reference voltage (REF2)	REF2 (V) = (D/2^{12}) × 2.5
00101	Reserved	Reserved
00110	Reserved	Reserved
01100	Reserved	Reserved
01101	Voltage on the $+V_{SENSE}$ buffer output	$+V_{SENSE}$ (V) = ((50 × D)/2^{12}) − 25
01110	Voltage on the $-V_{SENSE}$ buffer output	$-V_{SENSE}$ (V) = ((50 × D)/2^{12}) − 25
10000	Reserved	Reserved
10001	Reserved	Reserved
10010	Reserved	Reserved
10011	Reserved	Reserved
10100	INT_AVCC	INT_AVCC (V) = D/2^{12} × 10
10101	V_{LDO}	V_{LDO} (V) = D/2^{12} × 10
10110	V_{LOGIC}	V_{LOGIC} (V) = D/2^{12} × 10
11000	REFGND	REFGND (V) = D/2^{12} × 2.5
11001	AGND	AGND (V) = D/2^{12} × 2.5
11010	DGND	DGND (V) = D/2^{12} × 2.5
11011	AV_{DD1}	AV_{DD1} (V) = D/2^{12} × 37.5
11100	AV_{DD2}	AV_{DD2} (V) = D/2^{12} × 37.5
11101	AV_{SS}	AV_{SS} (V) = (15 × D/2^{12} − 14) × 2.5
11110	Reserved	Reserved
11111	REFOUT	REFOUT (V) = (D/2^{12}) × 2.5

ADC Configuration

The ADC muxed input is configured using the ADC_CONFIG register via the ADC_IP_SELECT bits (Bits[4:0]).

Table 16. ADC Configuration Register

D10 to D8	D7 to D5	D4 to D0
100	000	ADC input select

This write to the ADC configuration register initiates a single conversion on the node currently selected in the ADC input select bits of the ADC_CONFIG register.

When a conversion is complete, the ADC result is available in the status register.

ADC Conversion Timing

Figure 71 shows an example where autostatus readback mode is enabled. The status register always contains the last completed ADC conversion result together with the associated mux address that was selected in the ADC_IP_SELECT bits.

During the first ADC conversion command shown, the contents of the status register are available on the SDO line. The ADC portion of this data contains the conversion result of the previously converted ADC node (ADC Conversion Result 0), as well as the associated channel address. If another SPI frame is not received while the ADC is busy converting due to Command 1, the next data to appear on the SDO line contains the associated conversion result (ADC Conversion Result 1). However, if an SPI frame is received while the ADC is busy, the status register contents available on SDO still contain the previous conversion result and indicates that the ADC_BUSY flag is high. Any new ADC conversion instructions received while the ADC_BUSY bit is active are ignored.

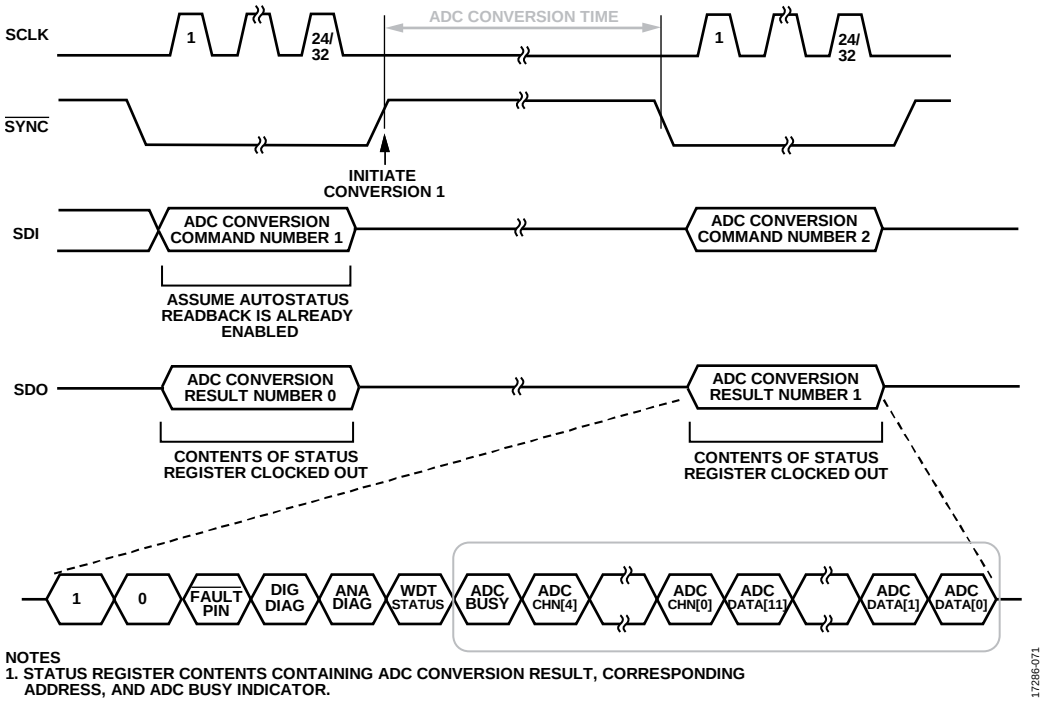


Figure 71. ADC Conversion Timing Example

REGISTER MAP

The AD5423 is controlled and configured via 22 on-chip registers described in the Register Details section. The four possible access permissions are as follows:

- R/W: read or write
- R: read only
- R/W-1-C: read or write 1 to clear
- R0/W: read zero or write

Reading from and writing to reserved registers is flagged as an invalid SPI access (see Table 39). When accessing registers with reserved bit fields, the default value of those bit fields must be written. These values are listed in the reset column of Table 23 to Table 44.

WRITING TO REGISTERS

Use the format data frame in Table 17 when writing to any register. By default, the SPI CRC is enabled and the input register is 32 bits wide, with the last eight bits corresponding to the CRC code. Only frames that are exactly 32 bits wide are accepted as valid. If the CRC is disabled, the input register is 24 bits wide, and 32-bit frames are also accepted with the final 8 bits ignored. Table 18 describes the bit names and functions of Bits[D23:D16]. Bits[D15:D0] depend on the register that is being addressed.

Table 17. Writing to a Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	[D15 to D0]
$\overline{AD1}$	AD1	AD0	REG_ADR4	REG_ADR3	REG_ADR2	REG_ADR1	REG_ADR0	Data

Table 18. Input Register Decode

Bit	Description
$\overline{AD1}$	Slip Bit. This bit must equal the inverse of Bit D22, that is, AD1.
AD1, AD0	Used in association with the external pins, AD1 and AD0, to determine which AD5423 device is being addressed by the system controller. Up to four unique devices can be addressed, corresponding to the AD1 and AD0 addresses of 0b00, 0b01, 0b10, and 0b11.
REG_ADR4, REG_ADR3, REG_ADR2, REG_ADR1, REG_ADR0	Selects which register is written to. See Table 22 for a summary of the available registers.

READING FROM REGISTERS

The AD5423 has four options for readback mode that can be configured in the TWO_STAGE_READBACK_SELECT register (see Table 38). These options are as follows:

- Two-stage readback
- Autostatus readback
- Shared $\overline{\text{SYNC}}$ autostatus readback
- Echo mode

Two-Stage Readback Mode

Two-stage readback mode consists of a write to the TWO_STAGE_READBACK_SELECT register to select the register location to be read back, followed by a NOP command. To perform a NOP command, write all zeros to Bits[D15:D0] of the NOP register. During the NOP command, the contents of the selected register are available on the SDO pin in the data frame format shown in Table 19. It is also possible to write a new two-stage readback command during the second frame, such that the corresponding new data is available on the SDO pin in the subsequent frame (see Figure 72). Bits[D31:D30] (or Bits[D23:D22], if SPI CRC is not enabled) = 0b10 are used as part of the synchronization during readback. The contents of the first write instruction to the TWO_STAGE_READBACK_SELECT register is shown in Table 20.

Table 19. SDO Contents for Read Operation

MSB **LSB**

[D23 to D22]	D21	[D20:16]	[D15 to D0]
0b10	$\overline{\text{FAULT}}$ pin status	Register address	Data

Table 20. Reading from a Register Using Two-Stage Readback Mode

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	[D15:D5]	D4	D3	D2	D1	D0
$\overline{\text{AD1}}$	AD1	AD0	0x13					Reserved	READBACK_SELECT[4:0]				

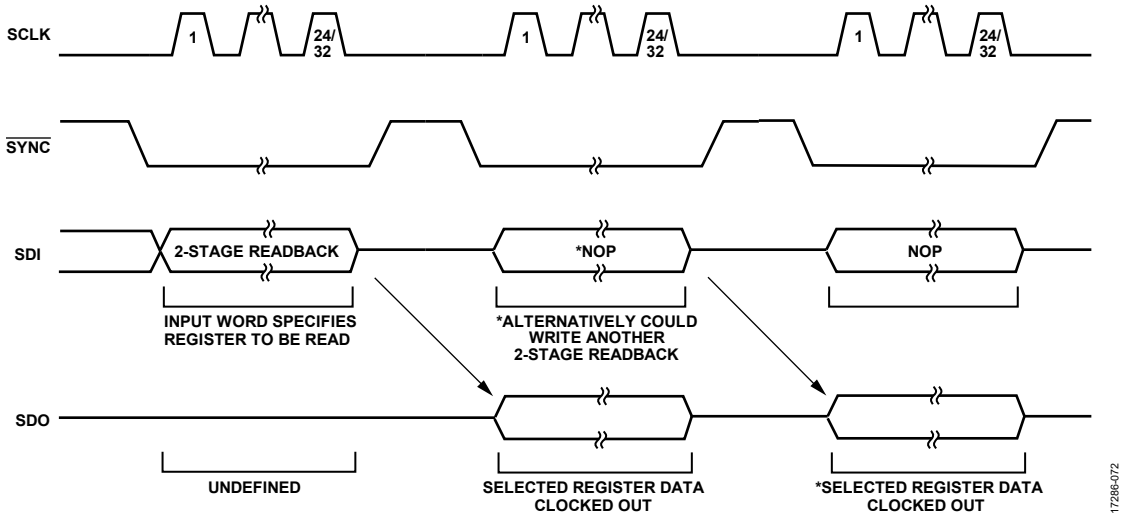


Figure 72. Two-Stage Readback Example

AUTOSTATUS READBACK MODE

If autostatus readback mode is selected, the contents of the status register are available on the SDO line during every SPI transaction. When reading back the status register, the SDO contents differ from the data frame format shown in Table 19. The contents of the status register are shown in Table 21.

The autostatus readback mode can be configured via the READBACK_MODE bits in the TWO_STAGE_READBACK_SELECT register (see the Two-Stage Readback Select Register section).

Table 21. SDO Contents for a Read Operation on the Status Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	[D16:D12]	[D11:D0]
1	0	FAULT_PIN_STATUS	DIG_DIAG_STATUS	ANA_DIAG_STATUS	WDT_STATUS	ADC_BUSY	ADC_CH	ADC_DATA

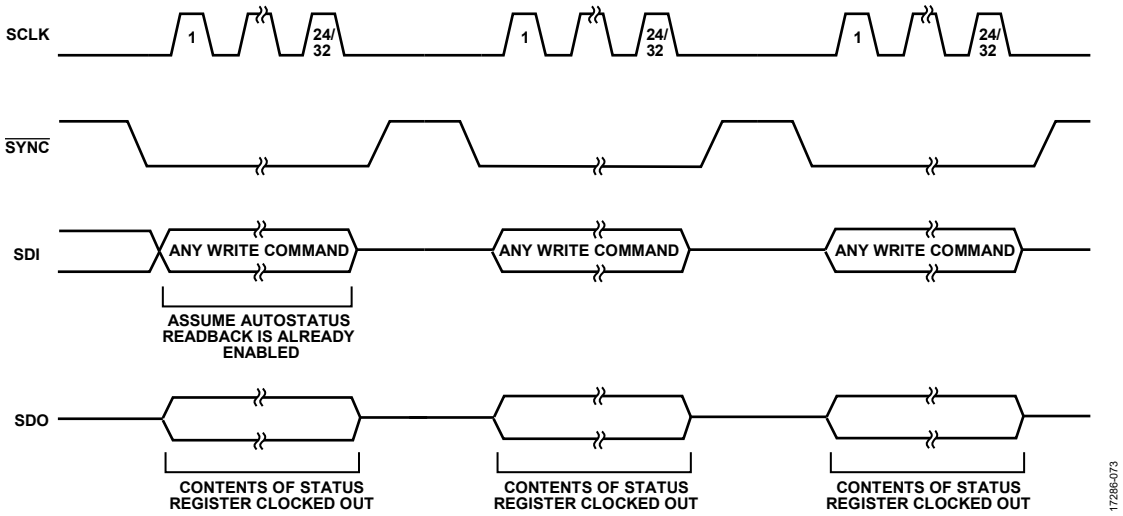


Figure 73. Autostatus Readback Example

Shared $\overline{\text{SYNC}}$ Autostatus Readback Mode

The shared $\overline{\text{SYNC}}$ autostatus readback is a special version of the autostatus readback mode that is used to avoid SDO bus contention when multiple AD5423 devices are sharing the same $\overline{\text{SYNC}}$ line. If this occurs, the AD5423 devices are distinguished from each other using the hardware address pins. An internal flag is set after each valid write to a device and the flag is cleared on the subsequent falling edge of $\overline{\text{SYNC}}$. The shared $\overline{\text{SYNC}}$ autostatus readback mode behaves in a similar manner to the normal autostatus readback mode, except the device does not output the status register contents on SDO when $\overline{\text{SYNC}}$ goes low, unless the internal flag is set, which occurs when the previous SPI write is valid. Refer to the example shown in Figure 74.

Echo Mode

Echo mode behaves in a similar manner to the autostatus readback mode, except that every second readback consists of an echo of the previous command written to the AD5423. Echo mode is useful for checking which SPI instruction is received in the previous SPI frame.

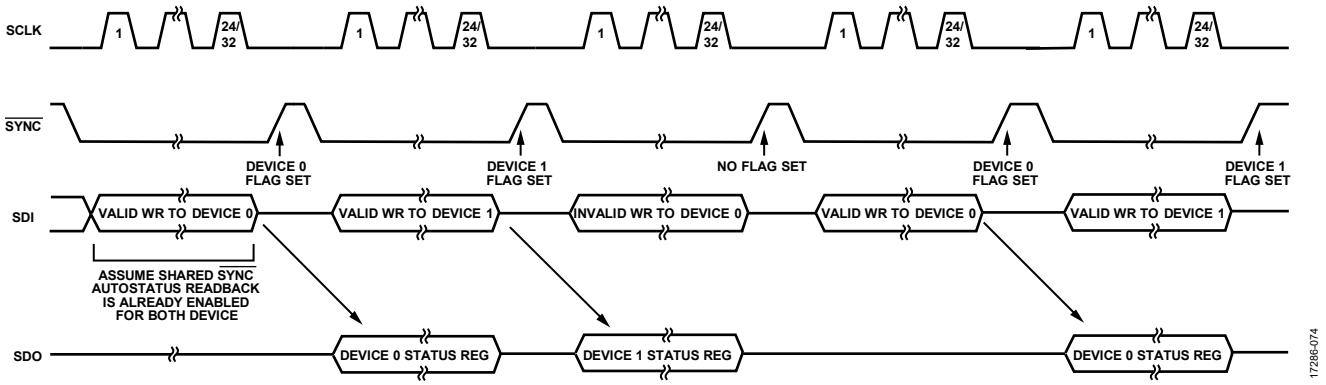


Figure 74. Shared $\overline{\text{SYNC}}$ Autostatus Readback Example

Figure 75. SDO Contents, Echo Mode

PROGRAMMING SEQUENCE TO ENABLE THE OUTPUT

To write to and set up the AD5423 device from a power-on or reset condition, take the following steps:

1. Perform a hardware or software reset and wait 100 µs.
2. Perform a calibration memory refresh by writing 0xFCBA to the key register. Wait a minimum of 500 µs before proceeding to Step 3 to allow time for the internal calibrations to complete. As an alternative to waiting 500 µs for the refresh cycle to complete, poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until it is 0.
3. Write 1 to Bit 13 in the DIGITAL_DIAG_RESULTS register to clear the RESET_OCCURRED flag.
4. Write to the DAC_CONFIG register to set the INT_EN bit, which powers up the DAC and internal amplifiers without enabling the channel output, and configure the output range, internal or external RSET, and slew rate. Keep the OUT_EN bit disabled at this point. Wait a minimum of 500 µs before proceeding to Step 6 to allow the internal calibrations to complete. As an alternative to waiting 500 µs for the refresh cycle to complete, poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until it reads 0.
5. Write a zero-scale DAC code to the DAC_INPUT register. If a bipolar range is selected in Step 7, then a DAC code that represents a 0 mA/0 V output must be written to the DAC_INPUT register. It is important that this step be completed even if the contents of the DAC_INPUT register are not changing.
6. If the LDAC functionality is being used, perform either a software or hardware LDAC command.
7. Rewrite the same word used in Step 4 to the DAC_CONFIG register except with the OUT_EN bit enabled.
8. Write the required DAC code to the DAC_INPUT register.

An example configuration is shown in Figure 76.

Changing and Reprogramming the Range

After the output is enabled, take the following steps to change the output range:

1. Write to the DAC_INPUT register. Set the output to 0 mA or 0 V.
2. Write to the DAC_CONFIG register. Disable the output (OUT_EN = 0), and set the new output range. Keep the INT_EN bit set. Wait 500 µs minimum before proceeding to Step 3 to allow time for internal calibrations to complete.
3. Write Code 0x0000, or in the case of bipolar ranges, write Code 0x8000, to the DAC_INPUT register. It is important that this step be completed even if the contents of the DAC_INPUT register do not change.
4. Reload the DAC_CONFIG register word from Step 2 and set the OUT_EN bit to 1 to enable the output.
5. Write the required DAC code to the DAC_INPUT register.

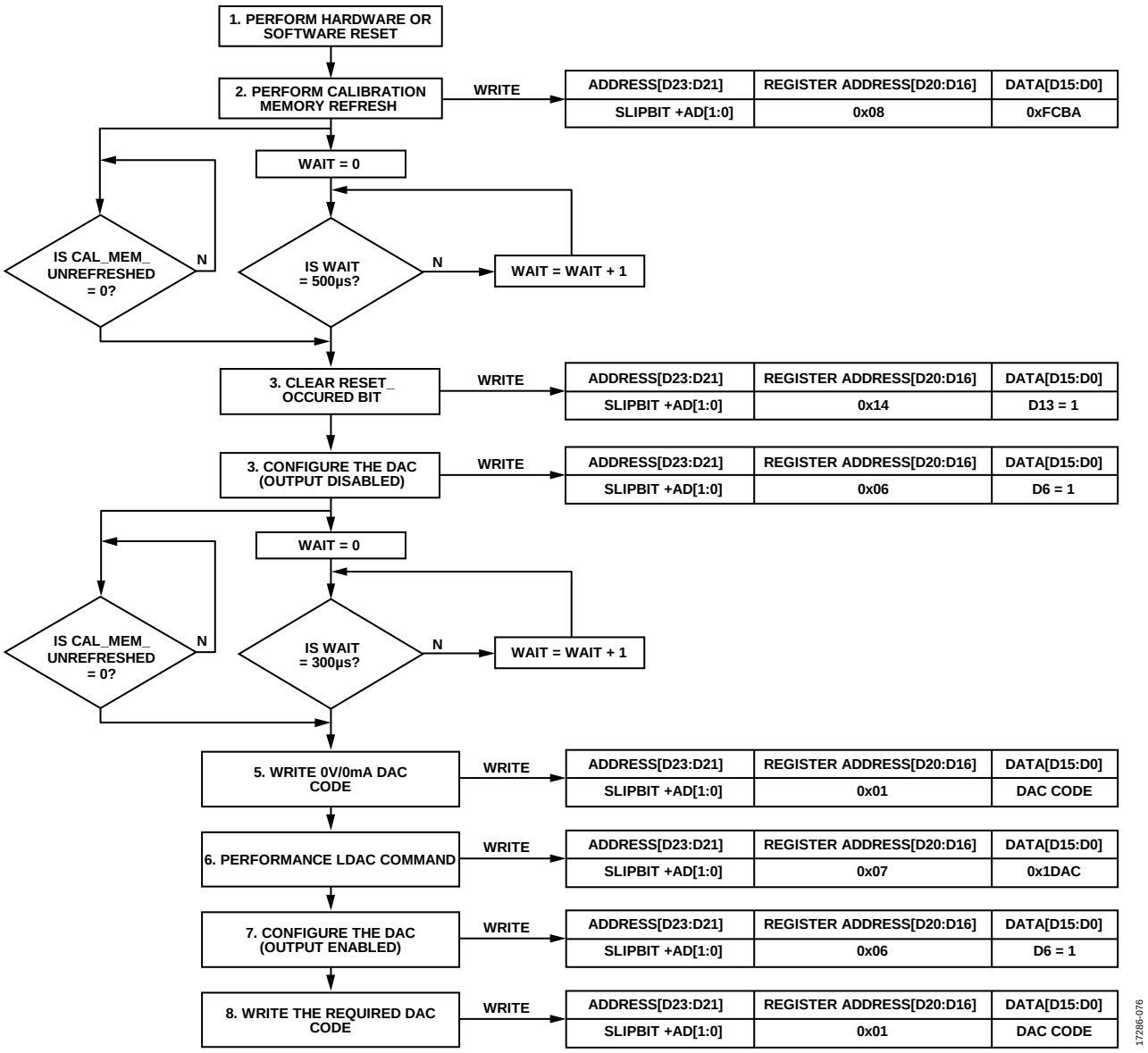


Figure 76. Example Configuration to Enable the Output Correctly (CRC Disabled for Simplicity)

REGISTER DETAILS

Table 22. Register Summary

Address	Name	Description	Reset	Access
0x00	NOP	NOP register.	0x000000	R
0x01	DAC_INPUT	DAC input register.	0x010000	R/W
0x02	DAC_OUTPUT	DAC output register.	0x020000	R
0x03	CLEAR_CODE	Clear code register.	0x030000	R/W
0x04	USER_GAIN	User gain register.	0x04FFFF	R/W
0x05	USER_OFFSET	User offset register.	0x058000	R/W
0x06	DAC_CONFIG	DAC configuration register.	0x060C00	R/W
0x07	SW_LDAC	Software LDAC register.	0x070000	R/W
0x08	KEY	Key register.	0x080000	R/W
0x09	GP_CONFIG1	General-Purpose Configuration 1 register.	0x090204	R/W
0x0A	GP_CONFIG2	General-Purpose Configuration 2 register.	0x0A0200	R/W
0x0B	RESERVED	Reserved.	0x0B0000	R/W
0x0C	RESERVED	Reserved.	0x0C0100	R/W
0x0D	RESERVED	Reserved.	0x0D0000	R/W
0x0E	RESERVED	Reserved.	0x0E0000	R/W
0x0F	WDT_CONFIG	Watchdog timer configuration register.	0x0F0009	R/W
0x10	DIGITAL_DIAG_CONFIG	Digital diagnostic configuration register.	0x10005D	R/W
0x11	ADC_CONFIG	ADC configuration register.	0x110000	R/W
0x12	FAULT_PIN_CONFIG	$\overline{\text{FAULT}}$ pin configuration register.	0x120000	R/W
0x13	TWO_STAGE_READBACK_SELECT	Two-stage readback select register.	0x130000	R/W
0x14	DIGITAL_DIAG_RESULTS	Digital diagnostic results register.	0x14A000	R
0x15	ANALOG_DIAG_RESULTS	Analog diagnostic results register.	0x150000	R
0x16	STATUS	Status register.	0x160000	R
0x17	CHIP_ID	Chip ID register.	0x170101	R
0x18	FREQ_MONITOR	Frequency monitor register.	0x180000	R
0x19	RESERVED	Reserved.	0x190000	R
0x1A	RESERVED	Reserved.	0x1A0000	R
0x1B	RESERVED	Reserved.	0x1B0000	R
0x1C	DEVICE_ID_3	Generic ID register.	0x1C0000	R

NOP Register

Address: 0x00, Reset: 0x000000, Name: NOP

Write 0x0000 to Bits[15: 0] at this address to perform a no operation (NOP) command. Bits[15:0] of this register always read back as 0x0000.

Table 23. Bit Descriptions for NOP

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	NOP command	Write 0x0000 to perform a NOP command.	0x0	R0/W

DAC Input Register

Address: 0x01, Reset: 0x010000, Name: DAC_INPUT

Bits[15:0] consist of the 16-bit data to be written to the DAC. If the $\overline{\text{LDAC}}$ pin is tied low (active), the DAC_INPUT register contents are written directly to the DAC_OUTPUT register without any $\overline{\text{LDAC}}$ functionality dependence. If the $\overline{\text{LDAC}}$ pin is tied high, the contents of the DAC_INPUT register are written to the DAC_OUTPUT register when the $\overline{\text{LDAC}}$ pin is brought low or when the software $\overline{\text{LDAC}}$ command is written.

Table 24. Bit Descriptions for DAC_INPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	DAC_INPUT_DATA	DAC input data.	0x0	R/W

DAC Output Register

Address: 0x02, Reset: 0x020000, Name: DAC_OUTPUT

DAC_OUTPUT is a read only register and contains the latest calibrated 16-bit DAC output value. If a clear event occurs due to a WDT fault, this register contains the clear code until the DAC is updated to another code.

Table 25. Bit Descriptions for DAC_OUTPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	DAC_OUTPUT_DATA	DAC output data. For example, the last calibrated 16-bit DAC output value.	0x0	R

Clear Code Register

Address: 0x03, Reset: 0x030000, Name: CLEAR_CODE

When writing to the CLEAR_CODE register, Bits[15:0] consist of the clear code that clears the DAC when a clear event occurs (for example, a WDT fault). After a clear event, the DAC_INPUT register must be rewritten to with the 16-bit data to be written to the DAC, even if it is the same data as previously written before the clear event. Performing an LDAC write to the hardware or software does not update the DAC_OUTPUT register to a new code until the DAC_INPUT register is written to first.

Table 26. Bit Descriptions for CLEAR_CODE

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	CLEAR_CODE	Clear code. The DAC clears to this code upon a clear event, for example, a WDT fault.	0x0	R/W

User Gain Register

Address: 0x04, Reset: 0x04FFFF, Name: USER_GAIN

The 16-bit USER_GAIN bits allow the user to adjust the gain of the DAC channel in steps of 1 LSB. The USER_GAIN bits coding is straight binary. The default code is 0xFFFF. Theoretically, the gain can be tuned across the full range of the output. However, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy.

Table 27. Bit Descriptions for USER_GAIN

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	USER_GAIN	User gain correction code.	0xFFFF	R/W

User Offset Register

Address: 0x05, Reset: 0x058000, Name: USER_OFFSET

The USER_OFFSET register allows the user to adjust the offset of the DAC channel by −32,768 LSBs to +32,768 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary. The default code is 0x8000, which results in zero offset programmed to the output.

Table 28. Bit Descriptions for USER_OFFSET

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	USER_OFFSET	User offset correction code.	0x8000	R/W

DAC Configuration Register

Address: 0x06, Reset: 0x060C00, Name: DAC_CONFIG

The DAC_CONFIG register configures the DAC (range, internal or external R_{SET}, and output enable), enables the output stage circuitry, and configures the slew rate control function.

Table 29. Bit Descriptions for DAC_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:13]	SR_STEP	Slew rate step. In conjunction with the slew rate clock, the slew rate step defines how much the output value changes at each update. Together, both parameters define the rate of change of the output value. 000: 4 LSB (default). 001: 12 LSB. 010: 64 LSB. 011: 120 LSB. 100: 256 LSB. 101: 500 LSB. 110: 1820 LSB. 111: 2048 LSB.	0x0	R/W
[12:9]	SR_CLOCK	Slew rate clock. Slew rate clock defines the rate at which the digital slew is updated. 0000: 240 kHz. 0001: 200 kHz. 0010: 150 kHz. 0011: 128 kHz. 0100: 64 kHz. 0101: 32 kHz. 0110: 16 kHz (default). 0111: 8 kHz. 1000: 4 kHz. 1001: 2 kHz. 1010: 1 kHz. 1011: 512 Hz. 1100: 256 Hz. 1101: 128 Hz. 1110: 64 Hz. 1111: 16 Hz.	0x6	R/W
8	SR_EN	Enables slew rate control. 0: disable (default). 1: enable.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	RSET_EXT_EN	Enables external current setting resistor. 0: select internal R_{SET} resistor (default). 1: select external R_{SET} resistor.	0x0	R/W
6	OUT_EN	Enables VI_{OUT}. 0: disable VI_{OUT} output (default). 1: enable VI_{OUT} output.	0x0	R/W
5	INT_EN	Enables internal buffers. 0: disable (default). 1: enable. Setting this bit powers up the DAC and internal amplifiers. It does not enable the output. It is recommended to set this bit and allow a >200 µs delay before enabling the output. This delay results in a reduced output enable glitch.	0x0	R/W
4	OVRNG_EN	Enables 20% voltage overrange. 0: disable (default). 1: enable.	0x0	R/W
[3:0]	RANGE	Selects output range. Note that changing the contents of these bits initiates an internal calibration memory refresh and, therefore, a subsequent SPI write must not be performed until the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register returns to 0. Writes to invalid Bits[3:0] codes are ignored. 0000: 0 V to 5 V voltage range (default). 0001: 0 V to 10 V voltage range. 0010: ±5 V voltage range. 0011: ±10 V voltage range. 1000: 0 mA to 20 mA current range. 1001: 0 mA to 24 mA current range. 1010: 4 mA to 20 mA current range. 1011: ±20 mA current range. 1100: ±24 mA current range. 1101: −1 mA to +22 mA current range.	0x0	R/W

Software LDAC Register

Address: 0x07, Reset: 0x070000, Name: SW_LDAC

Writing 0x1DAC to the SW_LDAC register performs a software LDAC mode update on the device matching the address bits within the SPI frame. If the GLOBAL_SW_LDAC bit in the GP_CONFIG2 register is set, Bit 21 and Bit 22 are ignored and all devices sharing the same SPI bus are updated via the SW_LDAC command. Bits[15:0] of this register always read back as 0x0000.

Table 30. Bit Descriptions for SW_LDAC

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	LDAC_COMMAND	Software LDAC Command. Write 0x1DAC to this register to perform a software LDAC instruction.	0x0	R0/W

Key Register

Address: 0x08, Reset: 0x080000, Name: KEY

The KEY register accepts specific key codes to perform tasks such as calibration memory refresh and software reset. Bits[15:0] of this register always read back as 0x0000. All unlisted key codes are reserved.

Table 31. Bit Descriptions for KEY

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	KEY_CODE	Key code. 0x15FA: first of two keys to initiate a software reset. 0xAF51: second of two keys to initiate a software reset. 0x0D06: key to reset the WDT. 0xFCBA: key to initiate a calibration memory refresh to the shadow registers. This key is only valid the first time it is run and has no effect if subsequent writes occur within a given system reset cycle.	0x0	R0/W

General-Purpose Configuration 1 Register

Address: 0x09, Reset: 0x090204, Name: GP_CONFIG1

This register is used to configure functions such as the temperature comparator threshold as well as enabling other miscellaneous features.

Table 32. Bit Descriptions for GP_CONFIG1

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:14]	RESERVED	Reserved.	0x0	R
[13:12]	SET_TEMP_THRESHOLD	Sets the temperature comparator threshold value. 00: 142°C (default). 01: 127°C. 10: 112°C. 11: 97°C.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R/W
[9:7]	RESERVED	Reserved.	0x4	R/W
6	HART_EN	Enables the path to the C_{HART} pin. 0: output of the DAC drives the output stage directly (default). 1: C_{HART} path is coupled to the DAC output to allow a HART modem connection or connection of a slew capacitor.	0x0	R/W
5	NEG_OFFSET_EN	Enables negative offset in unipolar V_{OUT} mode. When set, this bit offsets the currently enabled unipolar output range. This bit is only applicable to the 0 V to 6 V range and the 0 V to 12 V range. The 0 V to 6 V range becomes −300 mV to +5.7 V. The 0 V to 12 V range becomes −400 mV to +11.6 V. 0: disable (default). 1: enable.	0x0	R/W
4	CLEAR_NOW_EN	Enables the clear code to update the DAC immediately, even if the output slew feature is currently enabled. 0: disable (default). 1: enable.	0x0	R/W

3	SPI_DIAG_QUIET_EN	Enables SPI diagnostic quiet mode. When this bit is enabled, SPI_CRC_ERR, SLIPBIT_ERR, and SCLK_COUNT_ERR are not included in the logical OR calculation, which creates the DIG_DIAG_STATUS bit in the status register. They are also masked from affecting the $\overline{\text{FAULT}}$ pin if this bit is set. 0: disable (default). 1: enable.	0x0	R/W
2	OSC_STOP_DETECT_EN	Enables automatic 0x07DEAD code on SDO if the MCLK stops. 0: disable. 1: enable (default).	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	VIOUT_PULLDOWN_EN	Enables VI_{OUT} 30 kΩ pull-down resistor to AGND. 0: disable (default). 1: enable.	0x0	R/W

General-Purpose Configuration 2 Register

Address: 0x0A, Reset: 0x0A0200, Name: GP_CONFIG2

This register is used to configure and enable functions such as the voltage comparators and the global software LDAC command.

Table 33. Bit Descriptions for GP_CONFIG2

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	RESERVED	Reserved.	0x0	R0
[14:13]	COMPARATOR_CONFIG	Enables or disables the voltage comparator inputs for test purposes. The temperature comparator is permanently enabled. See the Background Supply and Temperature Monitoring section. 00: disables voltage comparators (default). 01: reserved. 10: reserved. 11: enables voltage comparators. The INT_EN bit in the DAC_CONFIG register must be set to power up the REFIN buffer and make the REFIN buffer available to the REFIN comparator.	0x0	R/W
12	RESERVED	Reserved.	0x0	R/W
11	RESERVED	Reserved.	0x0	R/W
10	GLOBAL_SW_LDAC	When enabled, the AD5423 address bits are ignored when performing a software LDAC command, enabling multiple devices to be simultaneously updated using one SW_LDAC command. 0: disable (default). 1: enable.	0x0	R/W
9	FAULT_TIMEOUT	Enables reduced fault detect timeout. This bit configures the delay from when the analog block indicates a VI_{OUT} fault has been detected to the associated change of the relevant bit in the ANALOG_DIAG_RESULTS register. This feature provides flexibility to accommodate a variety of output load values. 0: fault detect timeout 25 ms. 1: fault detect timeout 6.5 ms (default).	0x1	R/W
[8:0]	RESERVED	Reserved.	0x0	R/W

Watchdog Timer Configuration Register

Address: 0x0F, Reset: 0x0F0009, Name: WDT_CONFIG

The WDT_CONFIG register configures the WDT timeout value. This register also configures the acceptable resets for WDT setup and configures the resulting response to a WDT fault, for example, clearing the output or resetting the device.

Table 34. Bit Descriptions for WDT_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:11]	RESERVED	Reserved.	0x0	R
10	CLEAR_ON_WDT_FAIL	Enables a clear event to occur on WDT fault. If the WDT times out, a clear event occurs, whereby the output is loaded with the clear code stored in the CLEAR_CODE register. 0: disable (default). 1: enable.	0x0	R/W
9	RESET_ON_WDT_FAIL	Enables a software reset to automatically occur if the WDT times out. 0: disable (default). 1: enable.	0x0	R/W
8	KICK_ON_VALID_WRITE	Enables any valid SPI command to reset the WDT. Any active WDT error flags need to be cleared before the WDT can be restarted. 0: disable (default). 1: enable.	0x0	R/W
7	RESERVED	Reserved.	0x0	R/W
6	WDT_EN	Enables the WDT assuming there are no active WDT fault flags. Once enabled, the WDT will start immediately. 0: disable (default). 1: enable.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R/W
[3:0]	WDT_TIMEOUT	Sets the WDT timeout value. Setting WDT_TIMEOUT to a binary value beyond 0b1010 results in the default setting of 1 sec. 0000: 1 ms. 0001: 5 ms. 0010: 10 ms. 0011: 25 ms. 0100: 50 ms. 0101: 100 ms. 0110: 250 ms. 0111: 500 ms. 1000: 750 ms. 1001: 1 sec (default). 1010: 2 sec.	0x9	R/W

Digital Diagnostic Configuration Register

Address: 0x10, Reset: 0x10005D, Name: DIGITAL_DIAG_CONFIG

The DIGITAL_DIAG_CONFIG register configures various digital diagnostic features of interest for a particular application.

Table 35. Bit Descriptions for DIGITAL_DIAG_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:7]	RESERVED	Reserved.	0x0	R0
6	DAC_LATCH_MON_EN	Enables a diagnostic monitor on the DAC latches. This feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes causes the DAC_LATCH_MON_ERR flag bit to be set in the DIGITAL_DIAG_RESULTS register. 0: disable. 1: enable (default).	0x1	R/W
5	RESERVED	Reserved.	0x0	R/W
4	INVERSE_DAC_CHECK_EN	Enables check for DAC code vs. inverse DAC code error. 0: disable. 1: enable (default).	0x1	R/W
3	CAL_MEM_CRC_EN	Enables CRC of calibration memory on a calibration memory refresh. 0: disable. 1: enable (default).	0x1	R/W
2	FREQ_MON_EN	Enables the internal frequency monitor on the MCLK. 0: disable. 1: enable (default).	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	SPI_CRC_EN	Enables the SPI CRC function. 0: disable. 1: enable (default).	0x1	R/W

ADC Configuration Register

Address: 0x11, Reset: 0x110000, Name: ADC_CONFIG

The ADC_CONFIG register configures the ADC to one of the following four modes of operation: key sequencing, automatic sequencing, single immediate conversion of the currently selected ADC_IP_SELECT node, and single-key conversion.

Table 36. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:11]	RESERVED	Reserved.	0x0	R/W
[10:8]	SEQUENCE_COMMAND	ADC sequence command bits. 000: reserved (do not select this option). 001: reserved (do not select this option). 010: reserved (do not select this option). 011: reserved (do not select this option). 100: initiate a single conversion on the ADC_IP_SELECT (Bits[4:0]) input. 101: reserved (do not select this option). 110: reserved (do not select this option). 111: reserved (do not select this option).	0x0	R/W
[7:5]	SEQUENCE_DATA	Reserved (do not alter the default value of these bits).	0x0	R/W
[4:0]	ADC_IP_SELECT	Selects which node to multiplex to the ADC. All unlisted 5-bit codes are reserved and return an ADC result of zero. 00000: die temperature. 00001: Reserved (do not select this option). 00010: Reserved (do not select this option). 00011: REFIN. The INT_EN bit in the DAC_CONFIG register must be set for the REFIN buffer to be powered up and this node to be available to the ADC. 00100: REF2; internal 1.23 V reference voltage. 00101: reserved (do not select this option). 00110: reserved (do not select this option). 01100: reserved (do not select this option). 01101: voltage on the $+V_{SENSE}$ buffer output. 01110: voltage on the $-V_{SENSE}$ buffer output. 10000: reserved (do not select this option). 10001: reserved (do not select this option). 10010: reserved (do not select this option). 10011: reserved (do not select this option). 10100: INT_AVCC. 10101: VLDO. 10110: V_{LOGIC}. 11000: REFGND. 11001: AGND. 11010: DGND. 11011: AV_{DD1}. 11100: AV_{DD2}. 11101: AV_{SS}. 11110: reserved (do not select this option). 11111: REFOUT.	0x0	R/W

$\overline{\text{FAULT}}$ Pin Configuration Register

Address: 0x12, Reset: 0x120000, Name: FAULT_PIN_CONFIG

The FAULT_PIN_CONFIG register is used to mask particular fault bits from the $\overline{\text{FAULT}}$ pin, if so desired.

Table 37. Bit Descriptions for FAULT_PIN_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	INVALID_SPI_ACCESS_ERR	If this bit is set, do not map the INVALID_SPI_ACCESS_ERR fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
14	RESERVED	Reserved.	0x0	R/W
13	RESERVED	Reserved.	0x0	R/W
12	INVERSE_DAC_CHECK_ERR	If this bit is set, do not map the INVERSE_DAC_CHECK_ERR flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
11	RESERVED	Reserved.	0x0	R/W
10	OSCILLATOR_STOP_DETECT	If this bit is set, do not map the clock stop error to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
9	DAC_LATCH_MON_ERR	If this bit is set, do not map the DAC_LATCH_MON_ERR fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
8	WDT_ERR	If this bit is set, do not map the WDT_ERR flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
7	SLIPBIT_ERR	If this bit is set, do not map the SLIPBIT_ERR error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
6	SPI_CRC_ERR	If this bit is set, do not map the SPI_CRC_ERR error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R/W
3	IOUT_OC_ERR	If this bit is set, do not map the current output open circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
2	VOUT_SC_ERR	If this bit is set, do not map the voltage output short-circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
1	RESERVED	Reserved.	0x0	R/W
0	DIE_TEMP_ERR	If this bit is set, do not map the die temperature error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W

Two-Stage Readback Select Register

Address: 0x13, Reset: 0x130000, Name: TWO_STAGE_READBACK_SELECT

The TWO_STAGE_READBACK_SELECT register selects the address of the register required for a two-stage readback operation. The address of the register selected for readback is stored in Bits[4:0].

Table 38. Bit Descriptions for TWO_STAGE_READBACK_SELECT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:7]	RESERVED	Reserved.	0x0	R
[6:5]	READBACK_MODE	These bits control the SPI readback mode. 0: two-stage SPI readback mode (default). 01: autostatus readback mode. The status register contents are shifted out on SDO for every SPI frame. 10: shared $\overline{\text{SYNC}}$ autostatus readback mode. This mode allows the use of a shared $\overline{\text{SYNC}}$ line on multiple devices (distinguished using the hardware address pins). After each valid write to a device, a flag is set. This mode behaves similar to the normal autostatus readback mode, except that the device does not output the status register contents on SDO as $\overline{\text{SYNC}}$ goes low, unless the internal flag is set (that is, the previous SPI write is valid). 11: the status register contents and the previous SPI frame instruction are alternately available on SDO.	0x0	R/W
[4:0]	READBACK_SELECT	Selects readback address for a two-stage readback. 0x00: NOP register (default). 0x01: DAC_INPUT register. 0x02: DAC_OUTPUT register. 0x03: CLEAR_CODE register. 0x04: USER_GAIN register. 0x05: USER_OFFSET register. 0x06: DAC_CONFIG register. 0x07: SW_LDAC register. 0x08: KEY register. 0x09: GP_CONFIG1 register. 0x0A: GP_CONFIG2 register. 0x0B: RESERVED (do not select this option). 0x0C: RESERVED (do not select this option). 0x0D: RESERVED (do not select this option). 0x0E: RESERVED (do not select this option). 0x0F: WDT_CONFIG register. 0x10: DIGITAL_DIAG_CONFIG register. 0x11: ADC_CONFIG register. 0x12: FAULT_PIN_CONFIG register. 0x13: TWO_STAGE_READBACK_SELECT register. 0x14: DIGITAL_DIAG_RESULTS register. 0x15: ANALOG_DIAG_RESULTS register. 0x16: STATUS register. 0x17: CHIP_ID register. 0x18: FREQ_MONITOR register. 0x19: RESERVED (do not select this option). 0x1A: RESERVED (do not select this option). 0x1B: RESERVED (do not select this option). 0x1C: DEVICE_ID_3 register.	0x0	R/W

Digital Diagnostic Results Register

Address: 0x14, Reset: 0x14A000, Name: DIGITAL_DIAG_RESULTS

The DIGITAL_DIAG_RESULTS register contains an error flag for the on-chip digital diagnostic features, most of which are configurable using the digital diagnostic configuration register. This register also contains a flag to indicate that a reset occurred, as well as a flag to indicate that the calibration memory has not refreshed or an invalid SPI access was attempted. With the exception of the CAL_MEM_UNREFRESHED and SLEW_BUSY flags, all of these flags require a 1 to be written to them to update them to their current value. The CAL_MEM_UNREFRESHED and SLEW_BUSY flags automatically clear when the calibration memory refresh or output slew, respectively, is complete. When the corresponding enable bits in the DIGITAL_DIAG_CONFIG register are not enabled, the respective flag bits are read as zero.

Table 39. Bit Descriptions for DIGITAL_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	CAL_MEM_UNREFRESHED	Calibration memory unrefreshed flag. Modifying the RANGE bits in the DAC_CONFIG register also initiates a calibration memory refresh, which asserts this bit. Unlike the R/W-1-C bits in this register, this bit is automatically cleared after the calibration memory refresh completes. 0: calibration memory is refreshed. 1: calibration memory is unrefreshed (default on power-up). This bit asserts if the RANGE bits are modified in the DAC_CONFIG register.	0x1	R
14	SLEW_BUSY	This flag is set to 1 when the DAC is actively slewing. Unlike the R/W-1-C bits in this register, this bit is automatically cleared when slewing completes.	0x0	R
13	RESET_OCCURRED	This bit flags that a reset occurred (default on power-up is therefore Logic 1).	0x1	R/W-1-C
12	RESERVED	Reserved.	0x0	R/W-1-C
11	WDT_ERR	This bit flags a WDT fault.	0x0	R/W-1-C
[10:9]	RESERVED	Reserved.	0x0	R/W-1-C
8	DAC_LATCH_MON_ERR	This bit flags if the output of the DAC latches does not match the input.	0x0	R/W-1-C
7	RESERVED	Reserved.	0x0	R/W-1-C
6	INVERSE_DAC_CHECK_ERR	This bit flags if a fault is detected between the DAC code driven by the digital core and an inverted copy.	0x0	R/W-1-C
5	CAL_MEM_CRC_ERR	This bit flags a CRC error for the CRC calculation of the calibration memory upon refresh.	0x0	R/W-1-C
4	INVALID_SPI_ACCESS_ERR	This bit flags if an invalid SPI access is attempted, such as writing to or reading from an invalid or reserved address. This bit also flags if an SPI write is attempted directly after powering up but before a calibration memory refresh is performed, or if an SPI write is attempted while a calibration memory refresh is in progress. Performing a two-stage readback is permitted during a calibration memory refresh and does not cause this flag to set. Attempting to write to a read only register also causes this bit to assert.	0x0	R/W-1-C
3	RESERVED	Reserved.	0x0	R/W-1-C
2	SCLK_COUNT_ERR	This bit flags an SCLK falling edge count error. Thirty-two clocks are required if SPI CRC is enabled and 24 clocks or 32 clocks are required if SPI CRC is not enabled.	0x0	R/W-1-C
1	SLIPBIT_ERR	This bit flags an SPI frame slip bit error, that is, the MSB of the SPI word is not equal to the inverse of MSB − 1.	0x0	R/W-1-C
0	SPI_CRC_ERR	This bit flags an SPI CRC error.	0x0	R/W-1-C

Analog Diagnostic Results Register

Address: 0x15, Reset: 0x150000, Name: ANALOG_DIAG_RESULTS

The ANALOG_DIAG_RESULTS register contains an error flag corresponding to the four voltage nodes (V_{LDO}, INT_AVCC, REFIN, and REFOUT) monitored in the background by comparators, as well as a flag for the die temperature, which is also monitored by comparators. Voltage output short circuit and current output open circuit are contained in this register. Like the DIGITAL_DIAG_RESULTS register, all of the flags contained in this register require a 1 to be written to them to update or clear them. When the corresponding diagnostic features are not enabled, the respective error flags are read as zero.

Table 40. Bit Descriptions for ANALOG_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:8]	RESERVED	Reserved.	0x0	R0
7	IOUT_OC_ERR	This bit flags a current output open circuit error. This error bit is set in the case of a current output open circuit and in the case where there is insufficient headroom available to the internal current output driver circuitry to provide the programmed output current.	0x0	R/W-1-C
6	VOUT_SC_ERR	This bit flags a voltage output short-circuit error.	0x0	R/W-1-C
5	RESERVED	Reserved.	0x0	R0
4	DIE_TEMP_ERR	This bit flags an overtemperature error for the die.	0x0	R/W-1-C
3	REFOUT_ERR	This bit flags that the REFOUT node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C
2	REFIN_ERR	This bit flags that the REFIN node is outside of the comparator threshold levels.	0x0	R/W-1-C
1	INT_AVCC_ERR	This bit flags that the INT_AVCC node is outside of the comparator threshold levels.	0x0	R/W-1-C
0	VLDO_ERR	This bit flags that the VLDO node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C

Status Register

Address: 0x16, Reset: 0x160000, Name: STATUS

The STAUS register contains ADC data and status bits, as well as the WDT, OR'd analog and digital diagnostics, and the $\overline{\text{FAULT}}$ pin status bits.

Table 41. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
20	DIG_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[15:0] in the DIGITAL_DIAG_RESULTS register, with the exception of the SLEW_BUSY bit. Therefore, if any of these bits are high, the DIG_DIAG_STATUS bit is high. Note that this bit is high on power-up due to the active RESET_OCCURRED flag bit. A quiet mode is also available (SPI_DIAG_QUIET_EN in the GP_CONFIG1 register), such that the logical OR function only incorporates Bits[15:3] of the DIGITAL_DIAG_ RESULTS register (with the exception of the SLEW_BUSY bit). If an SPI CRC, SPI slip bit, or SCLK count error occurs, the DIG_DIAG_STATUS bit is not set high.	0x1	R
19	ANA_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[13:0] in the ANALOG_DIAG_RESULTS register. Therefore, if any bit in the ANALOG_DIAG_RESULTS register is high, the ANA_DIAG_STATUS bit is high.	0x0	R
18	WDT_STATUS	WDT status bit.	0x0	R
17	ADC_BUSY	ADC busy status bit.	0x0	R
[16:12]	ADC_CH	Address of the ADC channel represented by the ADC_DATA bits in the status register.	0x0	R
[11:0]	ADC_DATA	Twelve bits of ADC data representing the converted signal addressed by the ADC_CH bits, Bits[16:12].	0x0	R

Chip ID Register

Address: 0x17, Reset: 0x170101, Name: CHIP_ID

The CHIP_ID register contains the chip ID of the die.

Table 42. Bit Descriptions for CHIP_ID

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:11]	RESERVED	Reserved.	0x0	R0
[10:8]	RESERVED	Reserved.	0x0	R0
[7:0]	DIE_CHIP_ID	These bits reflect the revision number of the die.	0x2	R

Frequency Monitor Register

Address: 0x18, Reset: 0x180000, Name: FREQ_MONITOR

An internal frequency monitor uses the MCLK to create a pulse at a frequency of 1 kHz (MCLK/10,000). This pulse is used to increment a 16-bit counter. The value of the counter is available to read in the FREQ_MONITOR register. The user can poll this register periodically and use it both as a diagnostic tool for the internal oscillator (to monitor that the oscillator is running) and to measure the frequency. This feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register and allows a robustness check of the internal oscillator.

Table 43. Bit Descriptions for FREQ_MONITOR

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	FREQ_MONITOR	Internal clock counter value.	0x0	R

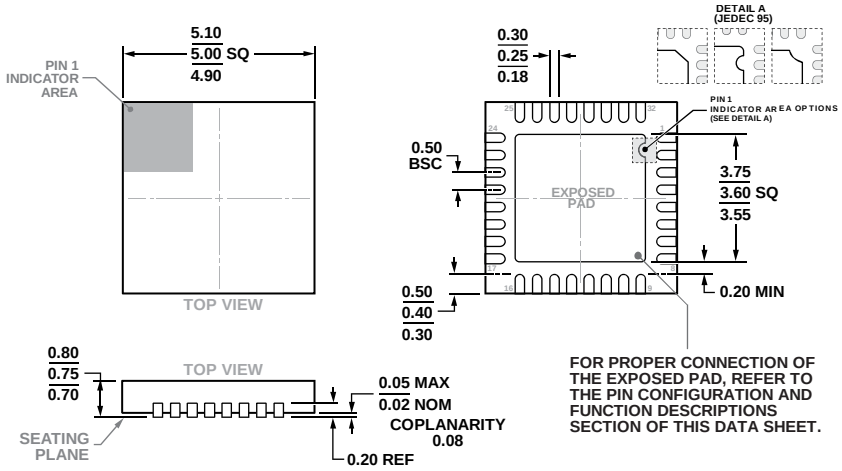
Generic ID Register

Address: 0x1C, Reset: 0x1C0000, Name: DEVICE_ID_3

Table 44. Bit Descriptions for DEVICE_ID_3

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:8]	RESERVED	Reserved.	0x0	R
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	GENERIC ID	Generic ID.	0x0	R
		000: AD5423.	0x0	R
		001: reserved.	0x0	R
		010: reserved.	0x0	R
		011: reserved.	0x0	R
		100: reserved.	0x0	R
		101: reserved.	0x0	R
		110: reserved.	0x0	R
		111: reserved.	0x0	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 77. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD5423BCPZ-RL7	−40°C to +115°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EVAL-AD5423SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-SDP-CS1Z is required to interface with EVAL-AD5423SDZ.

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