MULTI-INNO TECHNOLOGY CO., LTD.

www.multi-inno.com

OLED MODULE SPECIFICATION

Model : MI12864L1O-W

This module uses RoHS material

For Customer's Acceptance:

Customer	
Approved	
Comment	

The standard product specification may change without prior notice in order to improve performance or quality. Please contact Multi-Inno for updated specification and product status before design for the standard product or release of the order.	Revision	1.1
	Engineering	
	Date	2018-01-12
	Our Reference	

REVISION RECORD

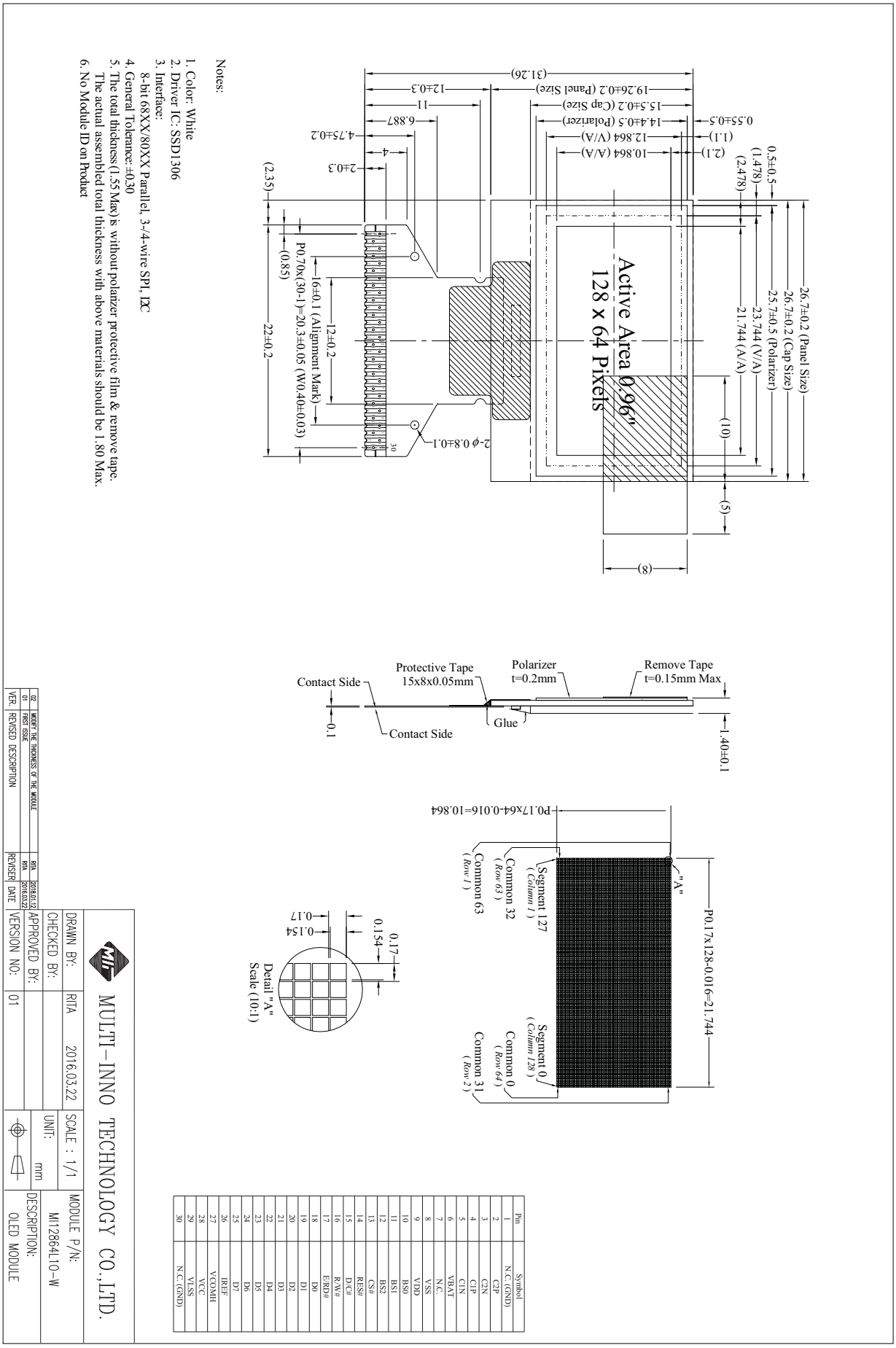
REV NO.	REV DATE	CONTENTS	REVISED PAGE NO.
1.0	2016-03-22	First Release	
1.1	2018-01-12	1. Modify the outline dimension from 26.70x19.26x1.45mm to 26.70x19.26x1.40mm.	P.4, P.5
		2. Modify supply voltage for DC/DC from 3.5V(MIN.) 4.2V(MAX.) to 3.0V(MIN.), 4.2V(MAX.).	P.8
		3. Modify supply voltage for Display from 7.0V(MIN.) 7.5V(MAX.) to 7.5V(TYP.).	P.8

CONTENT

■ PHYSICAL DATA

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (White)	-
3	Duty	1/64	-
4	Resolution	128(H) x 64 (V)	Pixel
5	Active Area	21.744 (W) x 10.864 (H)	mm
6	Outline Dimension	26.70 (W) x 19.26 (H) x 1.40 (D)	mm
7	Pixel Pitch	0.17 (W) x 0.17 (H)	mm
8	Pixel Size	0.154 (W) x 0.154 (H)	mm
9	Driver IC	SSD1306	-
10	Interface	8-bit parallel,3-/4-wire SPI,I2C	-
11	Weight	1.54	g

■ EXTERNAL DIMENSIONS



Pin	Symbol
1	N.C. (GND)
2	C2P
3	C2N
4	C1P
5	C1N
6	VBAT
7	N.C.
8	VSS
9	VDD
10	BS0
11	BS1
12	BS2
13	RES#
14	CS#
15	D/C#
16	R/W#
17	E/RD#
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	VCOMH
28	VCC
29	VLSS
30	N.C. (GND)

Notes:

1. Color: White
2. Driver IC: SSD1306
3. Interface:
   8-bit 68XX/80XX Parallel, 3-/4-wire SPI, I2C
4. General Tolerance: ±0.30
5. The total thickness (1.55 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.80 Max.
6. No Module ID on Product

VER.	REVISED DESCRIPTION	REVISER	DATE
02	MODIFY THE THICKNESS OF THE MODULE	RITA	2016.03.22
01	FIRST ISSUE	RITA	2016.01.12

MULTI-INNO TECHNOLOGY CO.,LTD.

DRAWN BY:	RITA	2016.03.22	SCALE : 1/1
CHECKED BY:			UNIT: mm
APPROVED BY:			
VERSION NO:	01		

MODULE P/N: MI12864L1O-W

DESCRIPTION: OLED MODULE

■ ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Typ.	Max	Unit	Notes
Supply voltage for logic	V_{DD}	-0.3	-	4	V	1,2
Supply voltage for display	V_{CC}	0	-	11.0	V	1,2
Supply voltage for DC/DC	V_{DDB}	-0.3	-	5.0	V	1,2
Operating temperature	T_{OP}	-40	-	70	℃	-
Storage temperature	T_{ST}	-40	-	85	℃	3
Life time(120cd/m²)	-	10,000	-	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.Also,for normal operations,it is desirable to use this module under the conditions according to electro-optical characteristics .If this module is used beyond these conditions,malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached.The reference average operating life time at room temperature is estimated by the accelerated at high temperature conditions.

■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Vcc Supplied Externally:

Items	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage for logic	V_{DD}		1.65	2.8	3.3	V
Supply voltage for display (Supplied externally)	V_{CC}	Note 5 (Internal DC/DC disable)	8.5	9.0	9.5	V
High level input	V_{IH}		0.8 x V_{DD}	-	V_{DD}	V
Low level input	V_{IL}		0	-	0.2 x V_{DD}	V
High level output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9 x V_{DD}	-	V_{DD}	V
Low level output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1x V_{DD}	V
Operating current for V_{DD}	I_{DD}		-	180	300	μA
Operating current for V_{CC} (V_{CC} Supplied externally)	I_{CC}	Note 6	-	5.1	6.4	mA
		Note 7	-	7.3	9.1	mA
		Note 8	-	12.3	15.4	mA
Sleep mode current for V_{DD}	$I_{DD,SLEEP}$		-	1	5	μA
Sleep mode current for V_{CC}	$I_{CC,SLEEP}$		-	2	10	μA

Note 5: Brightness(Lbr) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customers request.

Note 6: V_{DD} = 2.8V, V_{CC} = 9V, 30% Display Area Turn on.

Note 7: V_{DD} = 2.8V, V_{CC} = 9V, 50% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 9V, 100% Display Area Turn on.

* Software configuration follows Actual Application Example .

■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Vcc Generated by internal DC/DC Circuit:

Items	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage for logic	V_{DD}		1.65	2.8	3.3	V
Supply voltage for DC/DC	V_{DDB}	Internal DC/DC enable	3.0	-	4.2	V
Supply voltage for display (Generated by internal DC/DC)	V_{CC}	Note 9 (Internal DC/DC enable)	-	7.5	-	V
High level input	V_{IH}		0.8 x V_{DD}	-	V_{DD}	V
Low level input	V_{IL}		0	-	0.2 x V_{DD}	V
High level output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9 x V_{DD}	-	V_{DD}	V
Low level output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1x V_{DD}	V
Operating current for V_{DD}	I_{DD}		-	180	300	μA
Operating current for V_{DDB} (V_{CC} Generated by internal DC/DC)	I_{DDB}	Note 10	-	13.0	16.3	mA
		Note 11	-	18.8	23.5	mA
		Note 12	-	25.6	32.0	mA
Sleep mode current for V_{DD}	$I_{DD,SLEEP}$		-	1	5	μA
Sleep mode current for V_{CC}	$I_{CC,SLEEP}$		-	2	10	μA

Note 9: Brightness(Lbr) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customers request.

Note 10: V_{DD} = 2.8V, V_{DDB} = 3.5V, 30% Display Area Turn on.

Note 11: V_{DD} = 2.8V, V_{DDB} = 3.5V, 50% Display Area Turn on.

Note 12: V_{DD} = 2.8V, V_{DDB} = 3.5V, 100% Display Area Turn on.

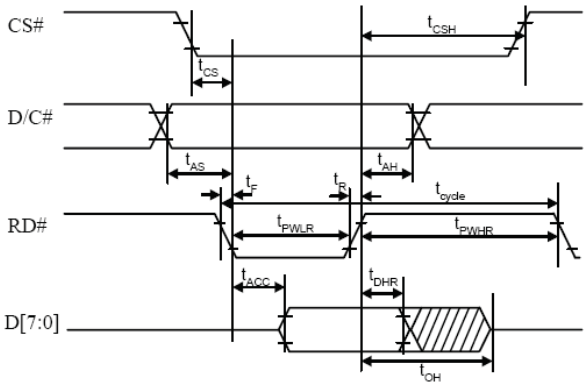
* Software configuration follows Actual Application Example .

◆AC Characteristics

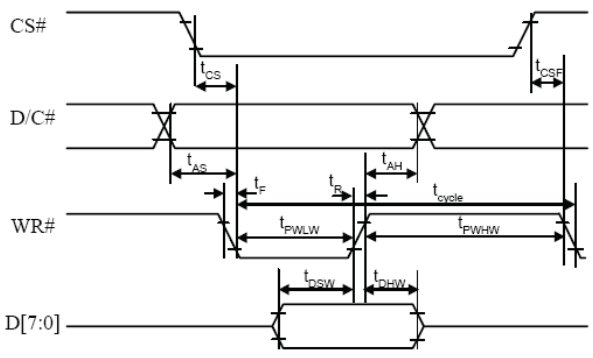
1. 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(***Read Timing***)

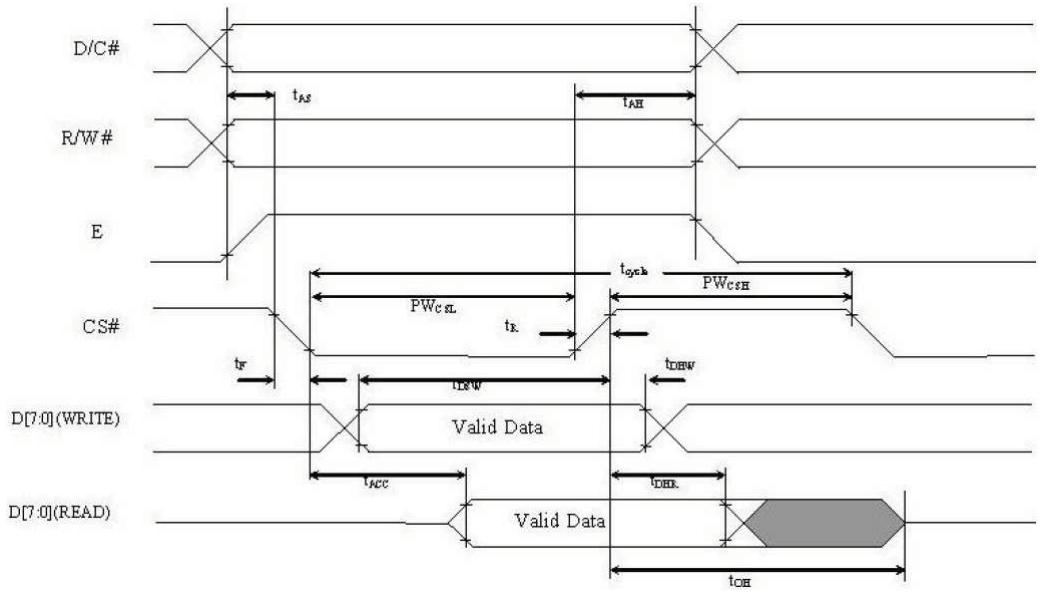


(***Write Timing***)

2. 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	5	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t	Fall Time	-	40	ns

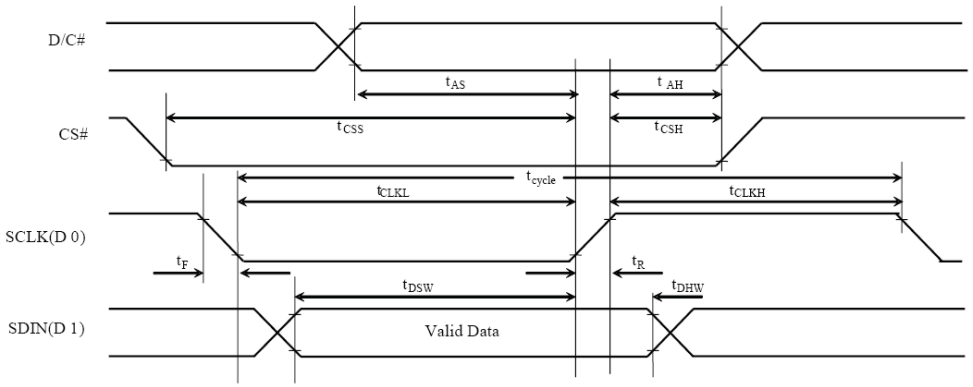
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

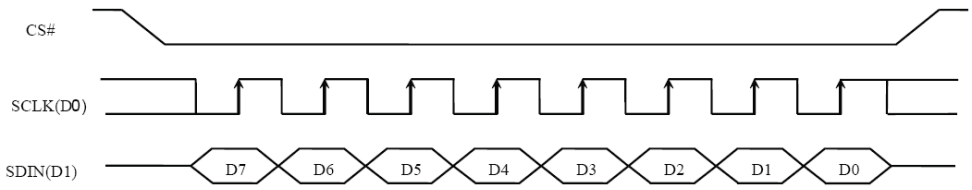


3. Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

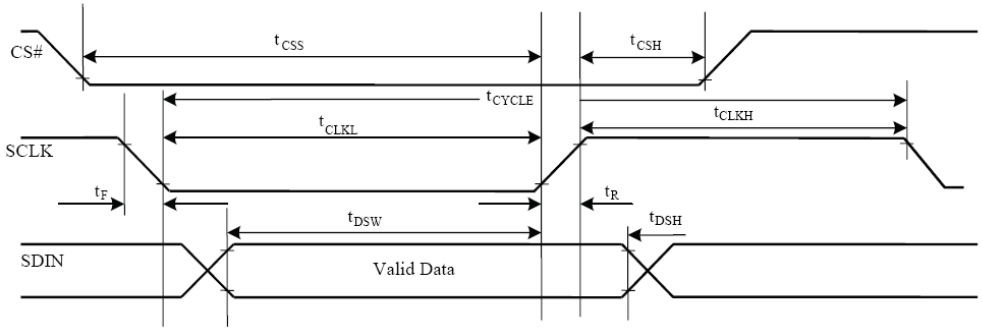


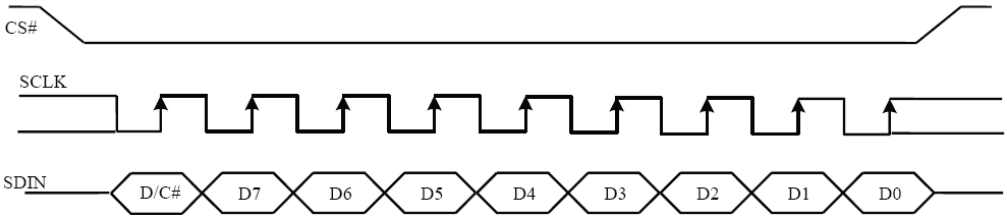


4. Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

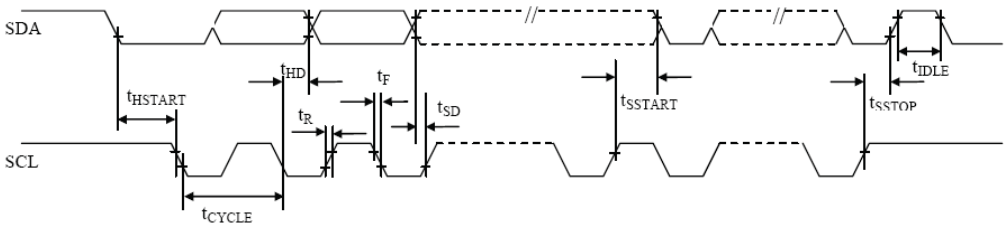




5. I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



■ TIMING OF POWER SUPPLY

1. Commands

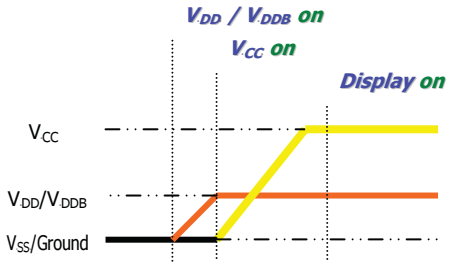
Refer to the Technical Manual for the SSD1306

2. Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

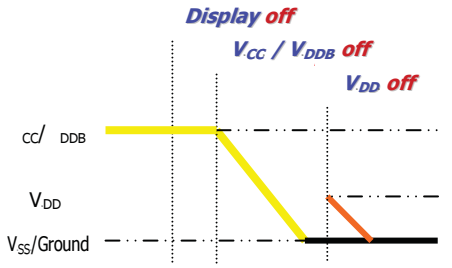
2.1 Power up Sequence:

1. Power up V_{DD} / V_{DDB}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



2.2 Power down Sequence:

1. Send Display off command
2. Power down V
3. Delay 100ms
   (When V_{CC} / V_{DDB} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 8:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{DDB} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{DDB}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{DDB} power down.

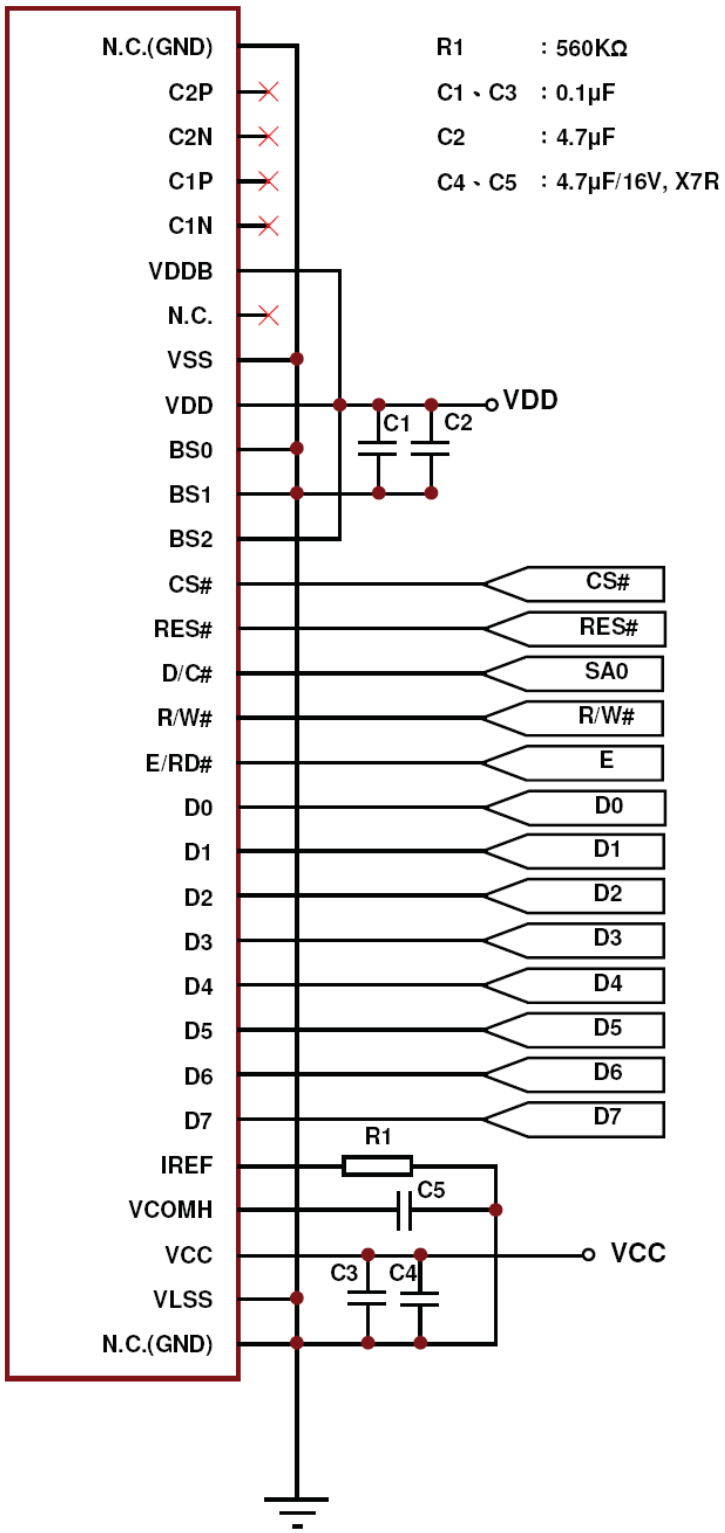
3. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

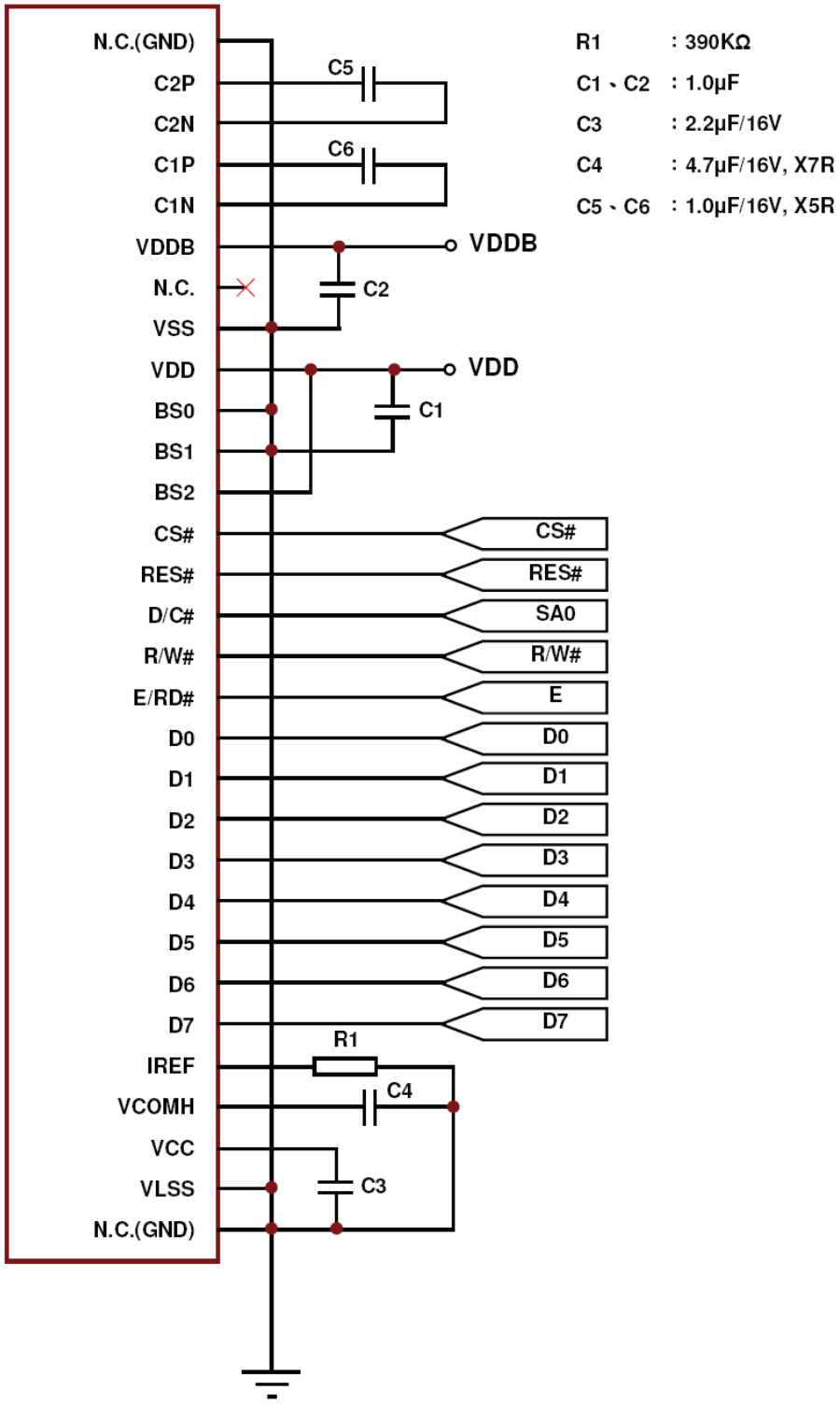
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4. Application circuit

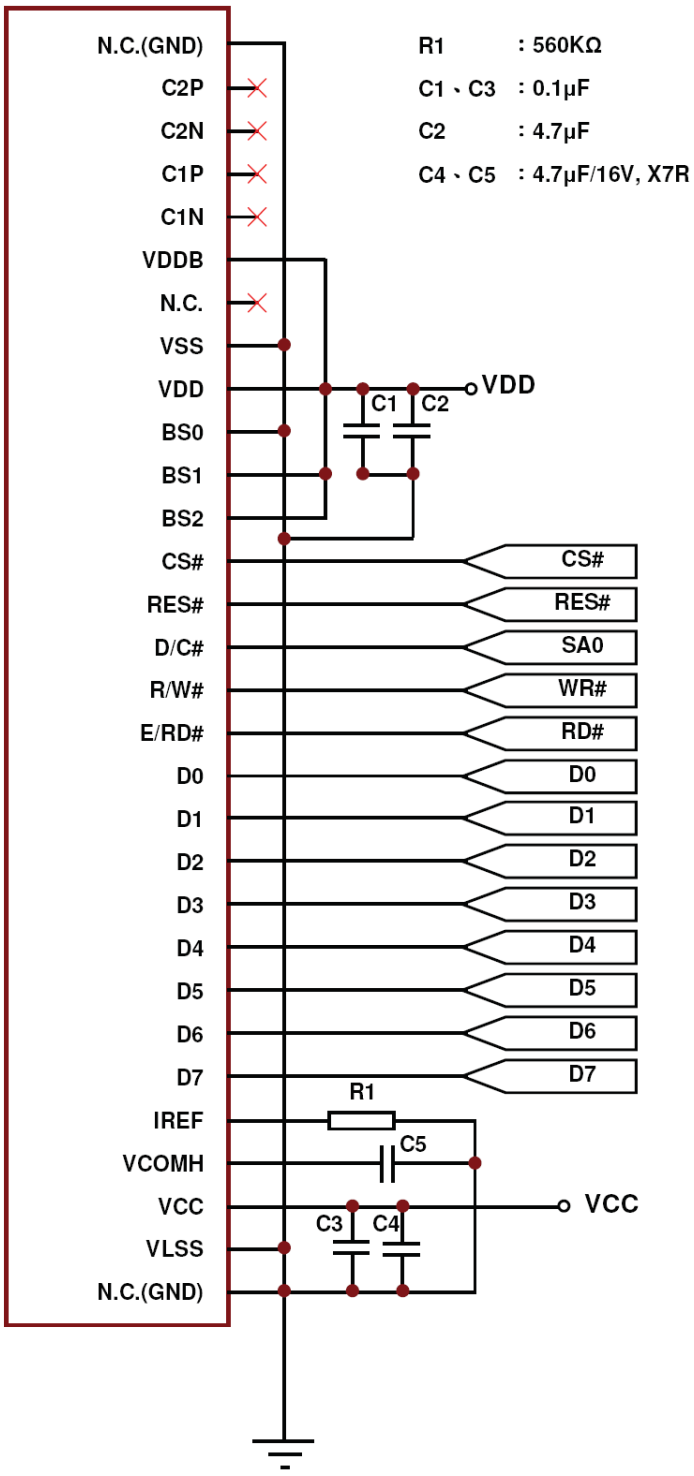
4.1 6800 parallel interface with V_{CC} Supplied Externally



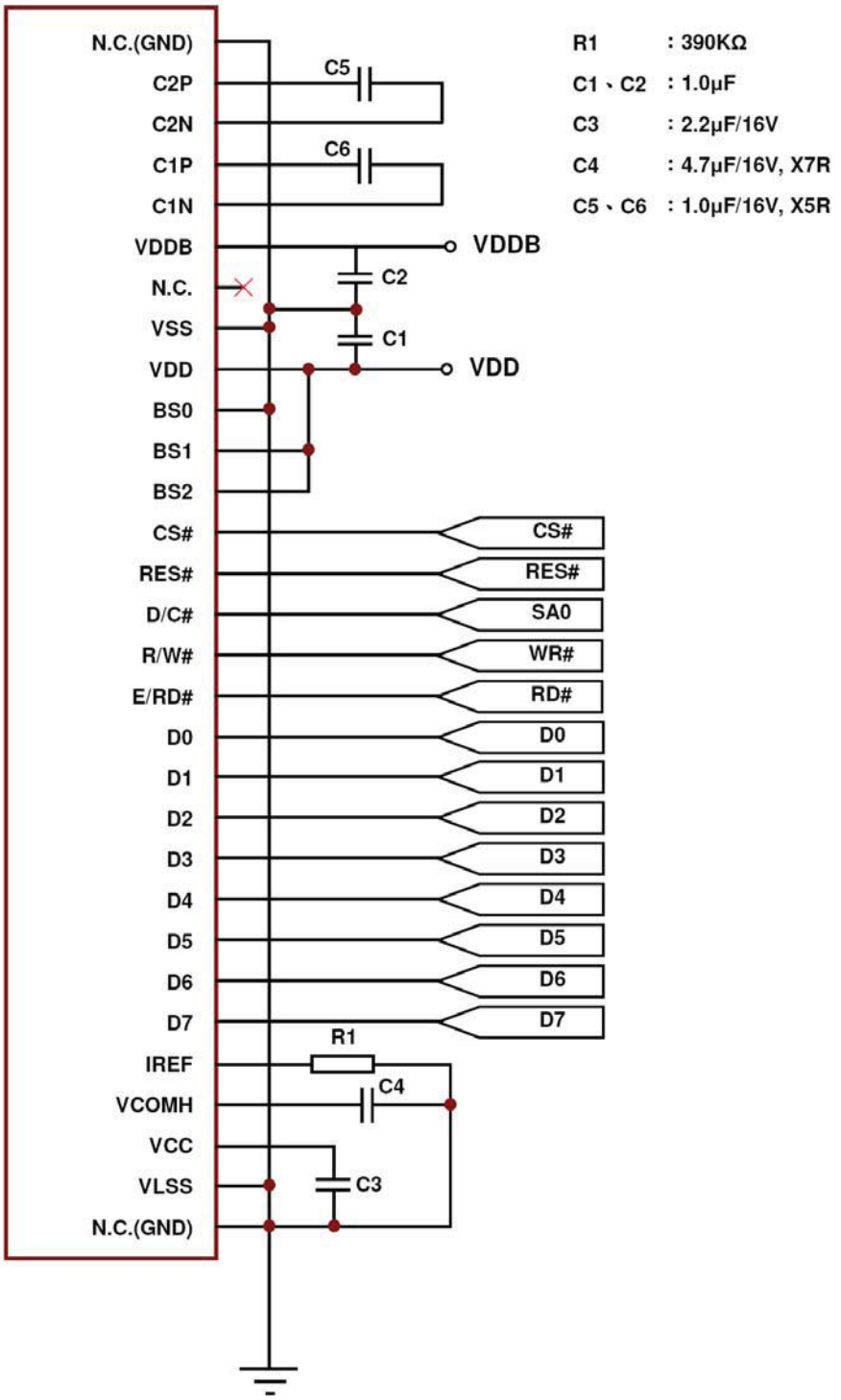
4.2 6800 parallelinterface with V_{CC} Generated by Internal DC/DC Circuit



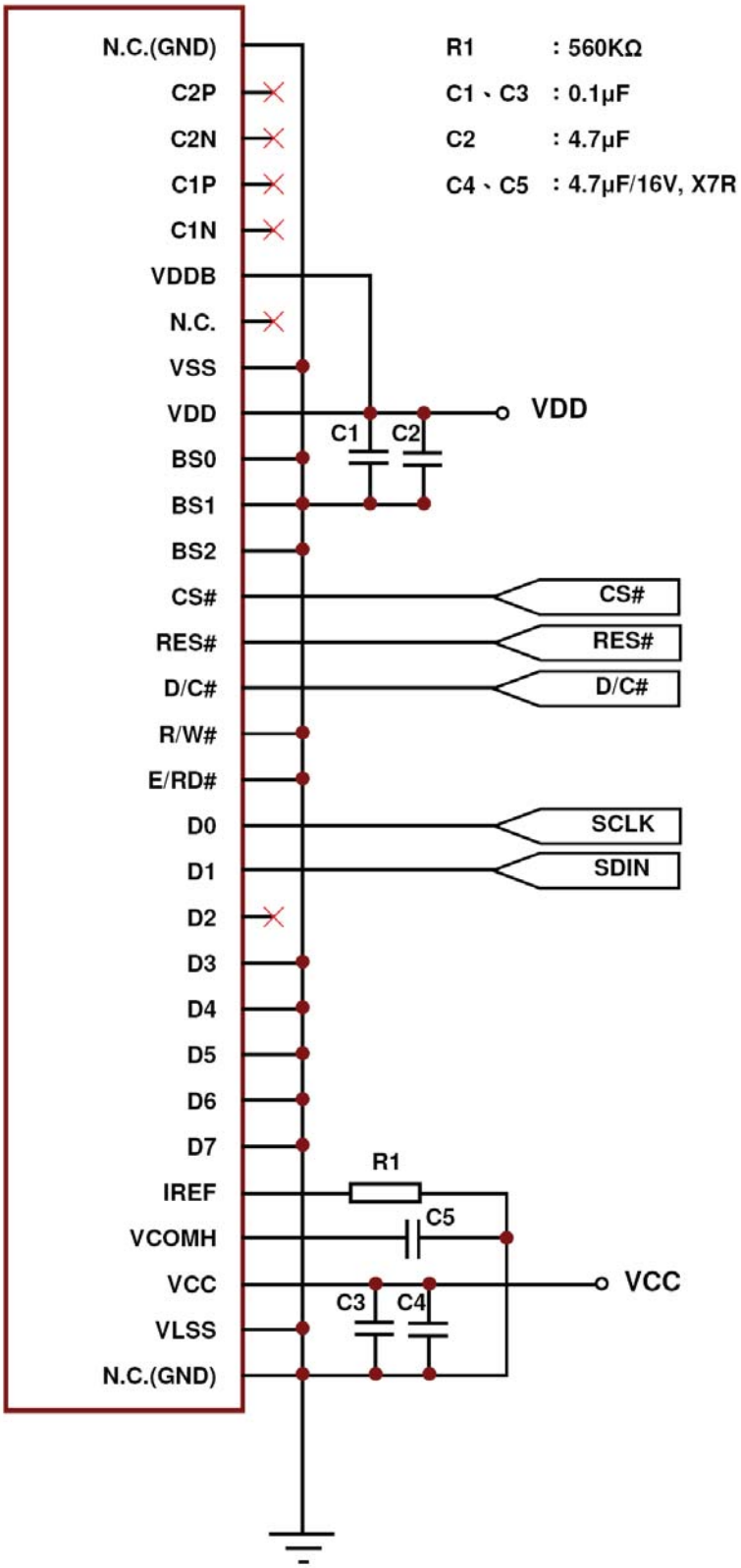
4.3 8080 parallel interface with V_{CC} Supplied Externally



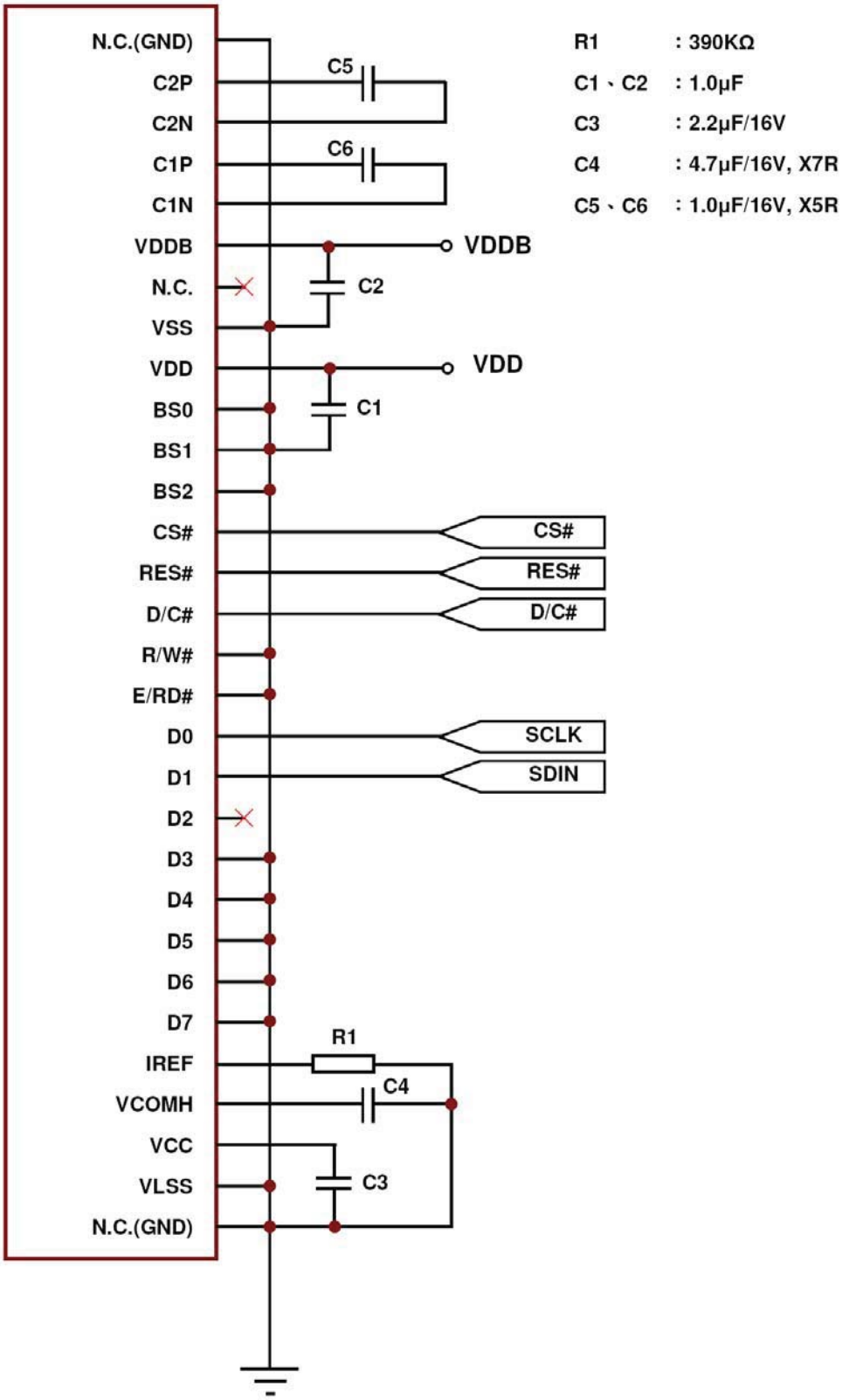
4.4 8080 parallel interface with V_{CC} Generated by Internal DC/DC Circuit



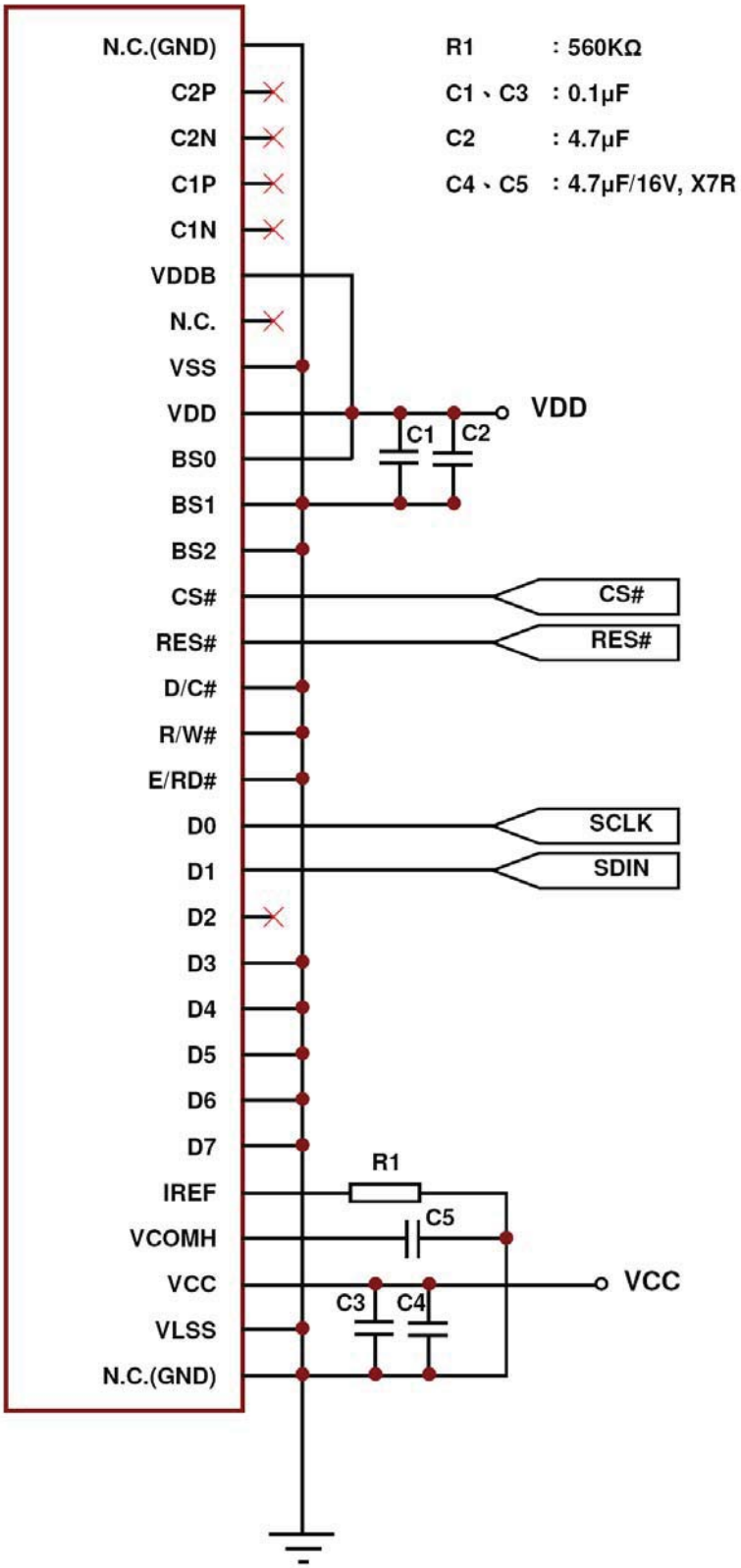
4.5 4-wire SPI interface with V_{CC} Supplied Externally



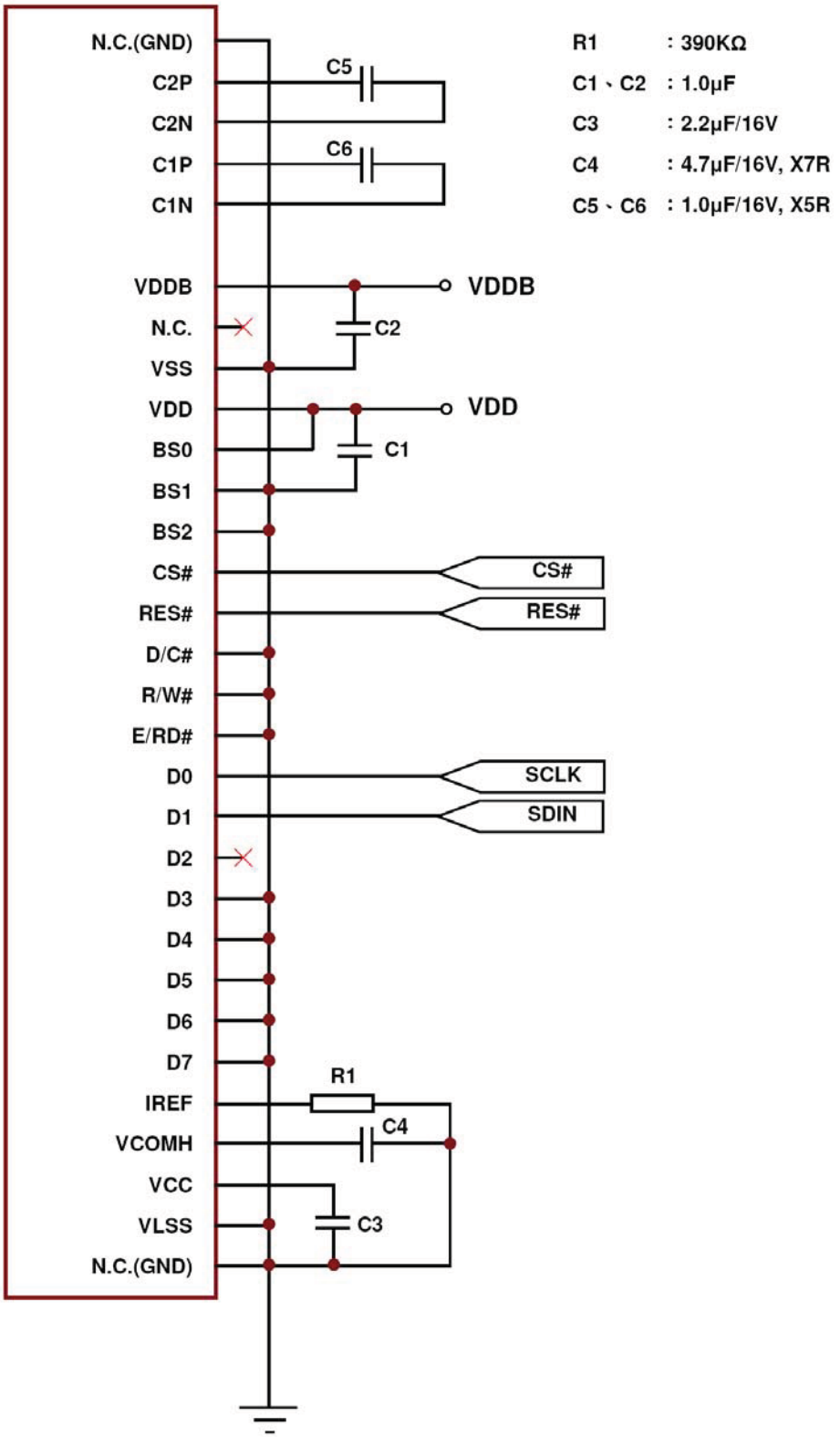
4.6 4-wire SPI interface with V_{CC} Generated by Internal DC/DC Circuit



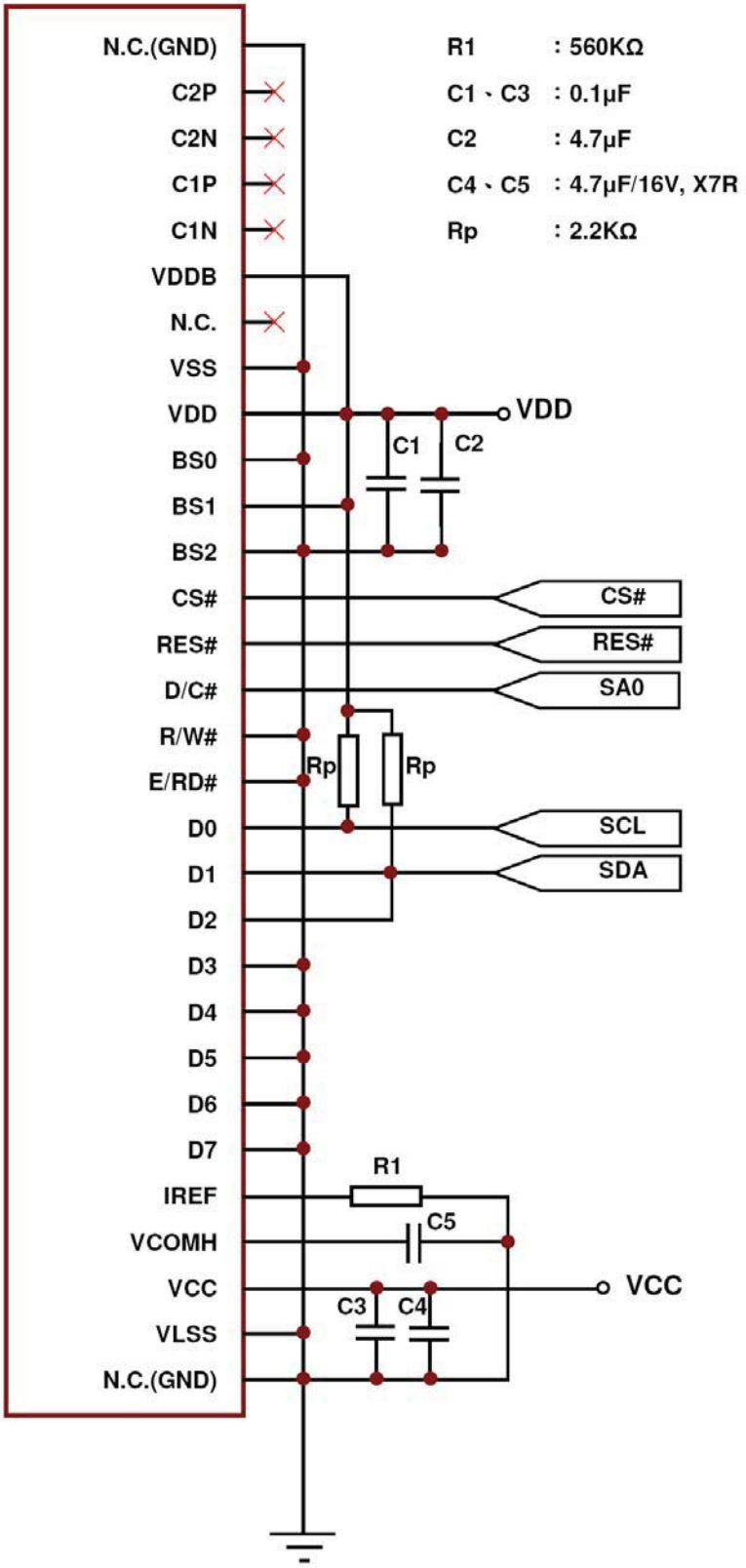
4.7 3-wire SPI interface with V_{CC} Supplied Externally



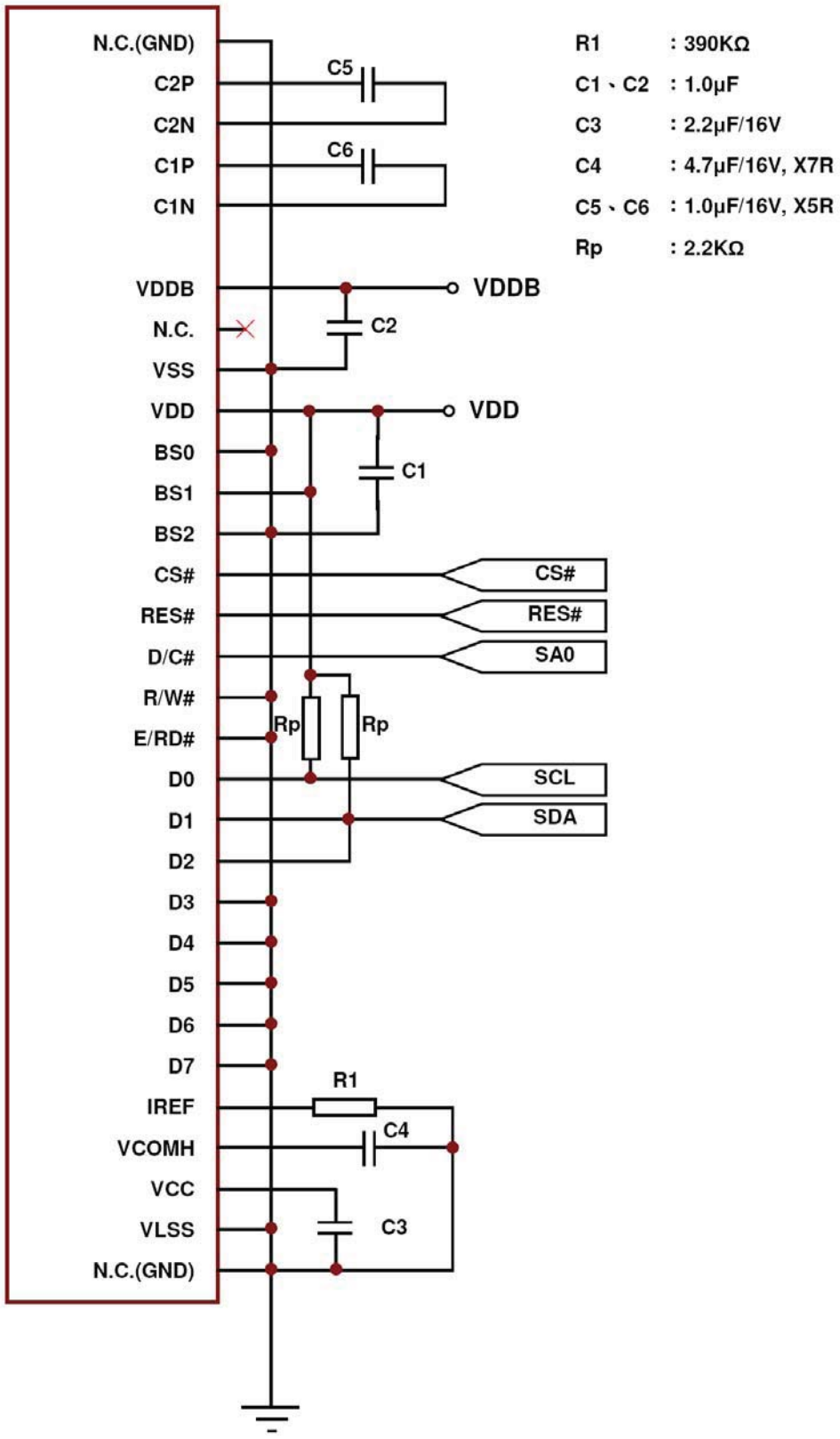
4.8 3-wire SPI interface with V_{CC} Generated by Internal DC/DC Circuit



4.9 I^2C interface with V_{CC} Supplied Externally



4.10 I²C interface with V_{CC} Generated by Internal DC/DC Circuit

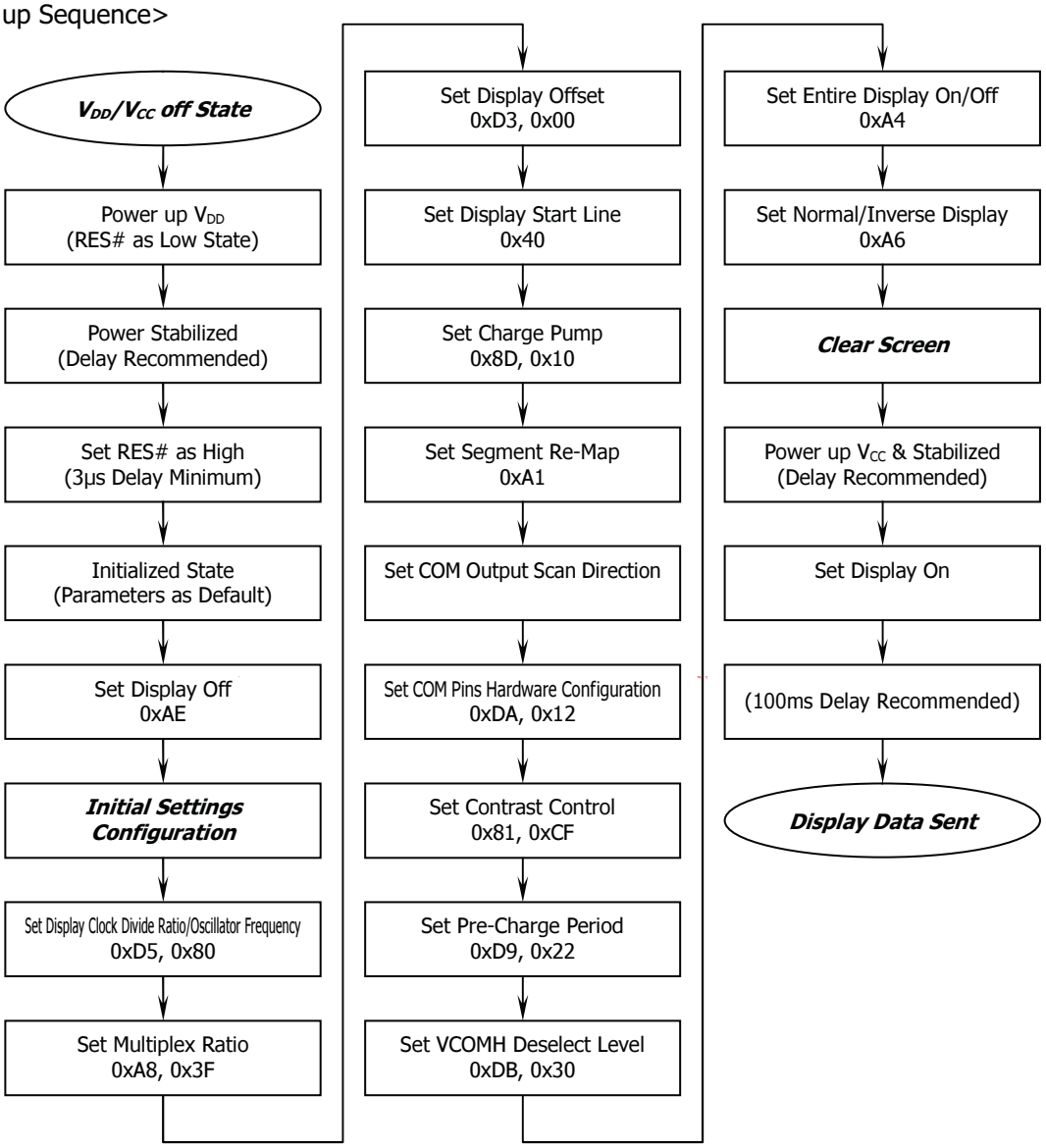


5. Actual Application Example

Command usage and explanation of an actual example

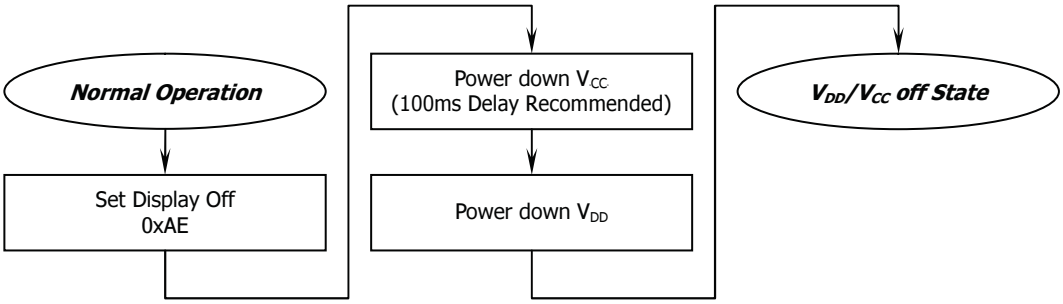
5.1 V_{CC} Supplied Externally

<Power up Sequence>

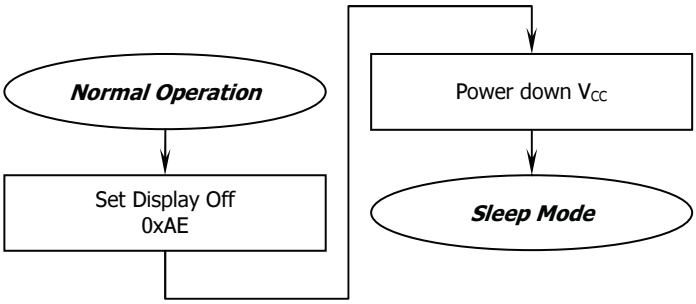


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

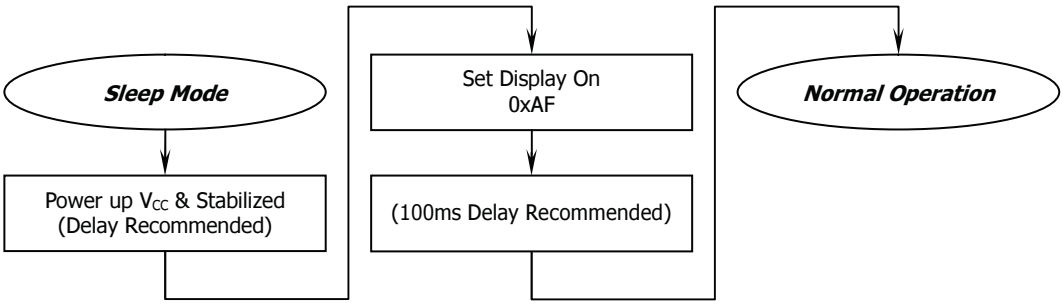
<Power down Sequence>



<Entering Sleep Mode>

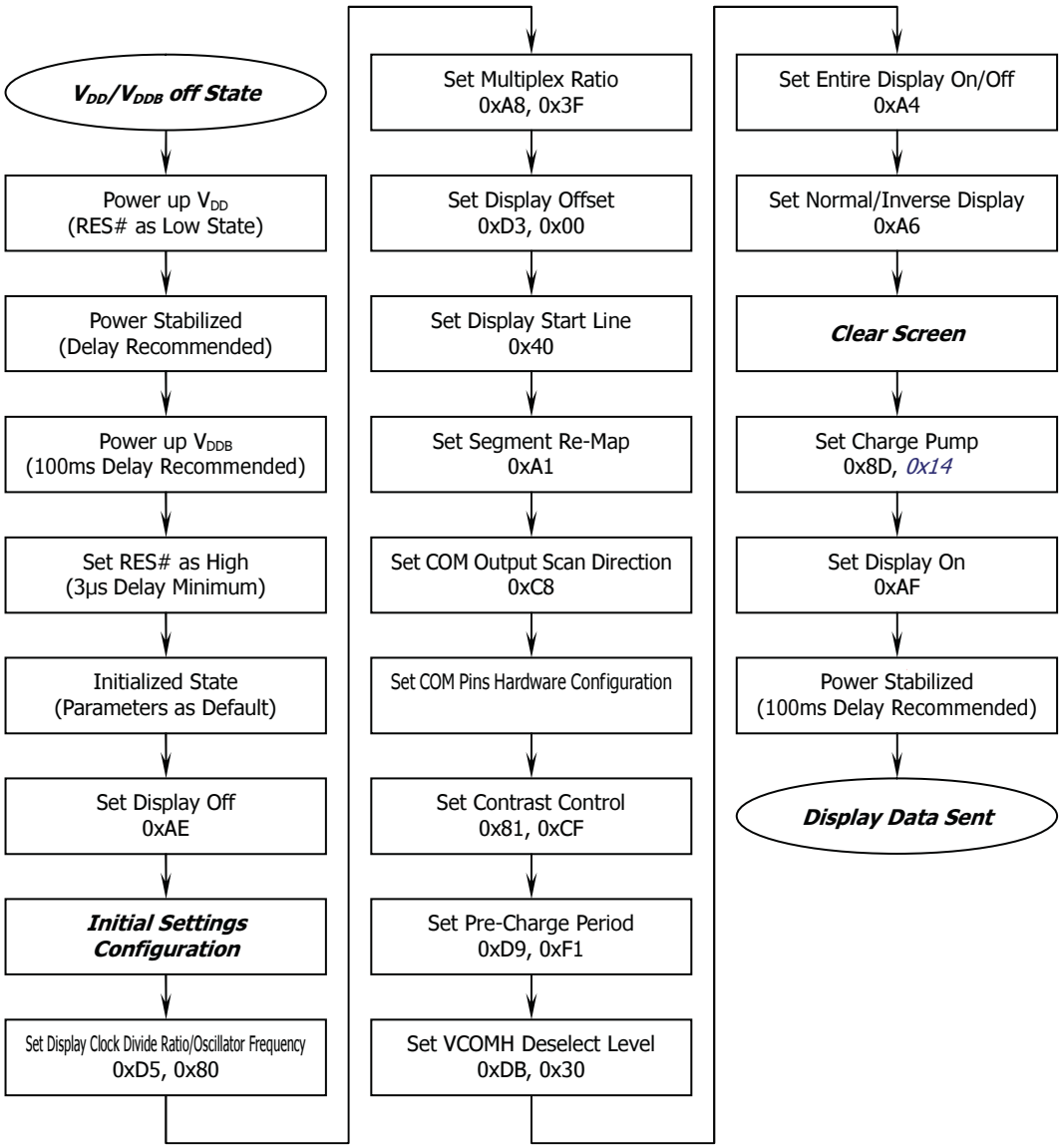


<Exiting Sleep Mode>



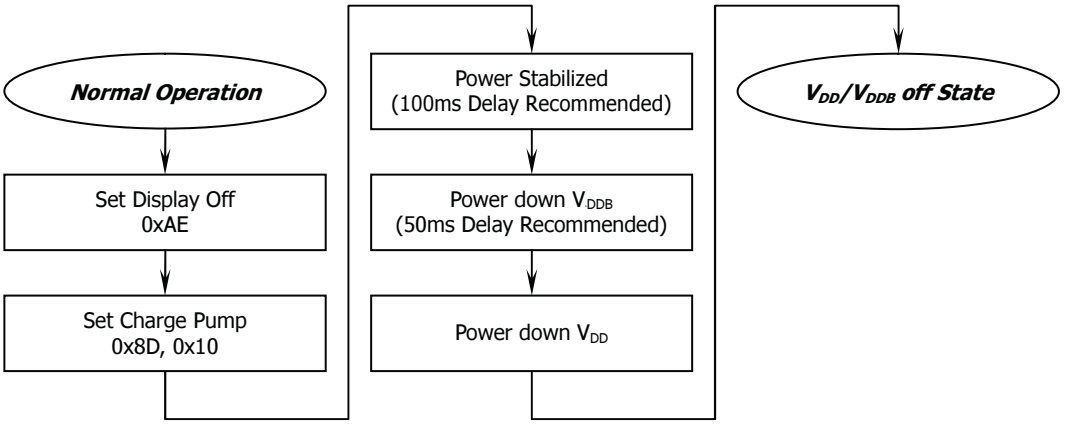
5.2 V_{CC} Generated by Internal DC/DC Circuit

<Power up Sequence>

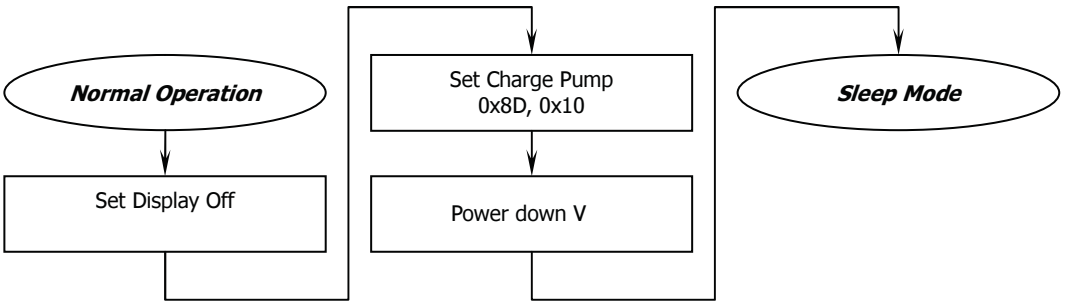


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

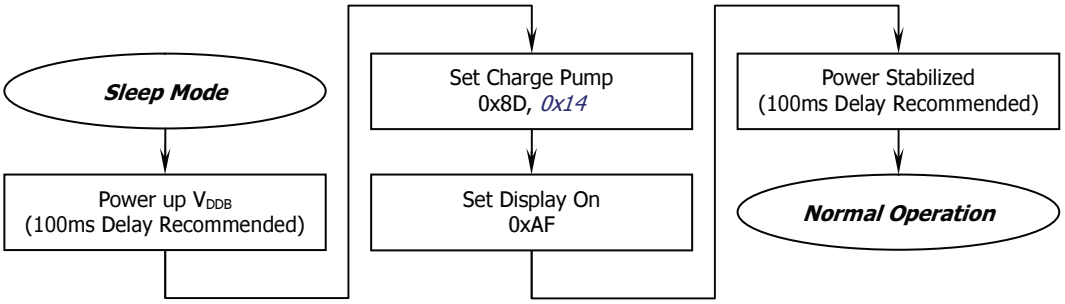
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Brightness(Vcc supplied externally)		Lbr	100	120	-	cd /m^2	Whtie
Brightness(Vcc generated by internal DC/DC)		Lbr	70	90	-	cd /m^2	White
Color Coordinate	White	CIE x	0.25	0.29	0.30	-	Without Polarizer
		CIE y	0.27	0.31	0.35		
Contrast Ratio*		Cr	-	>10000:1	-		Darkroom
Viewing Angle Uniformity		△ θ	-	Free	-	Degree	-

Note : Brightness (L_{br}) is subject to the change of the panel characteristics and the customer' s request.

* Optical measurement taken at V_{DD} = 2.8V, V_{CC}= 9.0V&7.5V.

Software configuration follows Actual Application Example .

2. Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>9</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>8</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>28</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.</td></tr>
<tr><td>29</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to V_{SS} externally.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>26</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.</td></tr>
<tr><td>27</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td colspan="4">DC/DC Converter</td></tr>
<tr><td>6</td><td>VDDB</td><td>P</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V_{DD} when the converter is not used.</td></tr>
<tr><td>4 / 5
2 / 3</td><td>C1P / C1N
C2P / C2N</td><td>I</td><td>Positive Terminal of the Flying Inverting Capacitor
Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>10
11
12</td><td>BS0
BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I^2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>17</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Number	Symbol	I/O	Function
Interface(Continued)			
16	R/W#	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I^2C mode is selected, this pin must be connected to V_{SS}.
18~25	D0~D7	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2 & D1 should be tired together and serve as SDA_{out} & SDA_{in} in application and D0 is the serial clock input SCL. Unused pins must be connected to V_{SS} except for D2 in serial mode.
Reserve			
7	N.C.	-	**Reserved Pin** The N.C. pin between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

■ RELIABILITY TESTS

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

■OUTGOING QUALITY CONTROL SPECIFICATION

1. Environ ment R equired

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

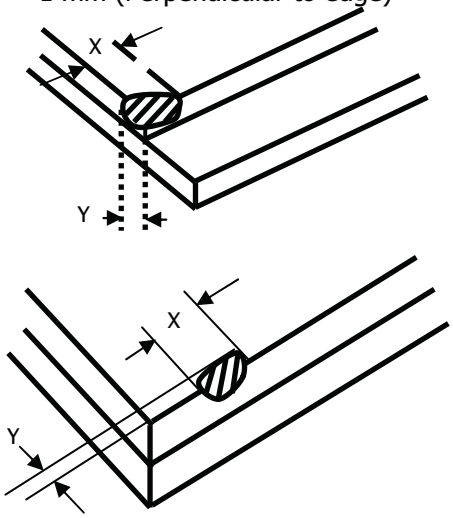
2. Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

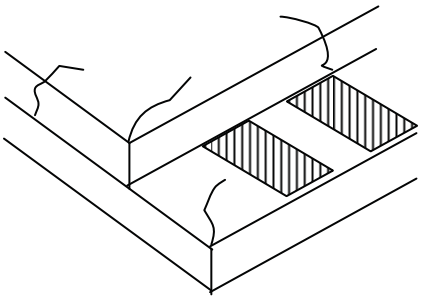
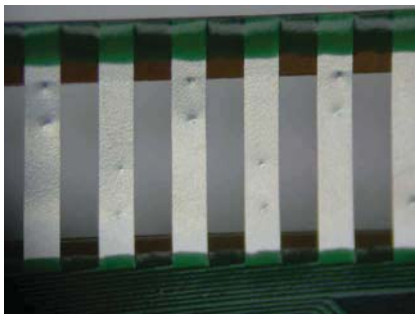
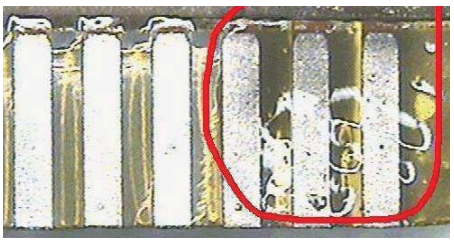
3. Criteria & Accep table Quanlity Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

3.1 Cosmetic Check (Display Off)in Non-Active Area

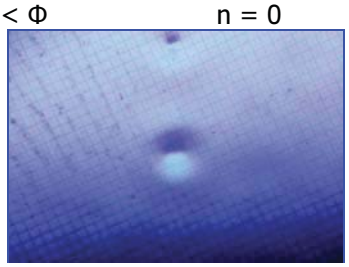
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

3.1 Cosmetic Check (Display Off) inNon-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

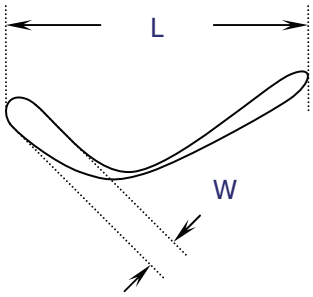
3.2 Cosmetic Check (Display Off) in Active Area

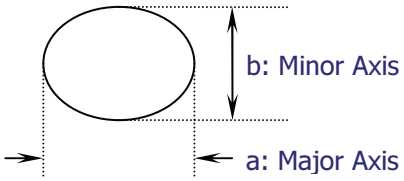
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

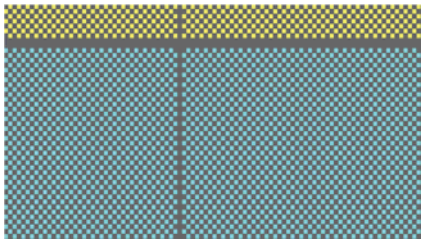
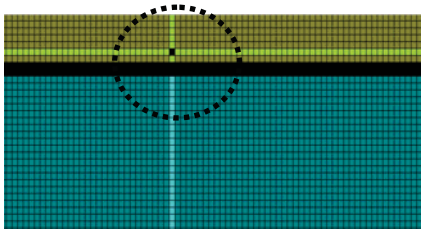
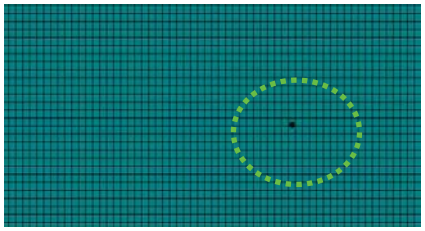
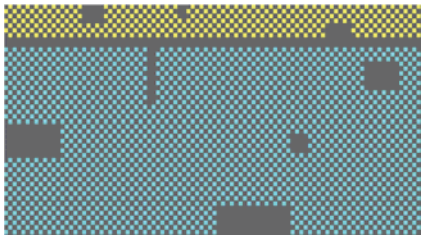
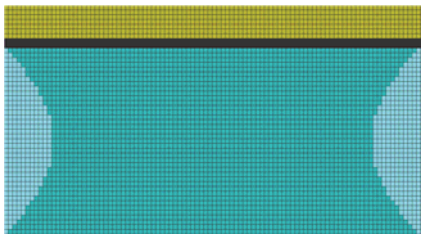
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





3.3 Pattern Check (Display On)inActive Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: V_{DD}(logic voltage) → V_{CC} (driving voltage), and power off sequence: V_{CC} (driving voltage) → V_{DD} (logic voltage).
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC

controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. If the module can not be used up in 3 months,make sure to seal the module in the vacuum bag with dessicant.
2. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
3. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
4. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless agreed between Multi-Inno and customer, Multi-Inno will replace or repair any of its OLED modules which are found to be functionally defective when inspected in accordance with Multi-Inno OLED acceptance standards(copies available upon request)for a period of one year from date of production. Cosmetic/visual defects must be returned to Multi-Inno within 90 days of shipment. Confirmation of such date shall be based on data code on product.The warranty liability of Multi-Inno limited to repair and/or replacement on the terms set forth above. Multi-Inno will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

No warranty can be granted if the precautions stated above have been disregarded.The typical examples of violations are:

-Broken OLED glass.
-PCB eyelet is damaged or modified.
-PCB conductors damaged.
-Circuit modified in any way,including addition of components.
-PCB tampered with by grinding,engraving or painting varnish.
-Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement.Modules must be returned with sufficient description of the failures or defects.Any connectors or cable installed by the customer must be removed completely.

■ PRIOR CONSULT MATTER

1. ① For Multi-Inno standard products,we keep the right to change material,process ... for

   ② For OEM products,if any change needed which may affect the product property,we will consult with our customer in advance.

2. If you have special requirement about reliability condition,please let us know before you start the test on our samples.