

28V, 3A, 500KHz Synchronous Step-Down DC/DC Converter

DESCRIPTION

The BL8036 is a fully integrated synchronous rectified step-down converter that provides wide 4.2V to 28V input voltage range and 3A continuous load current capability. The BL8036 can operate at PFM mode to achieve high efficiency and reduce power loss at light load. In shutdown mode, the Max supply current is about 3 μ A.

The BL8036 protection function includes cycle-by-cycle current limit, UVLO and thermal shutdown. Besides, internal soft-start prevents inrush current at fast power-on. This device uses slope compensated current mode control which provides fast load transient response. Internal loop compensation function reduces the external compensator components and simplifies the design process.

The BL8036 requires a minimum number of readily available standard external components and is available in ESOP-8 (Exposed Pad) package and provides good thermal conductance.

FEATURES

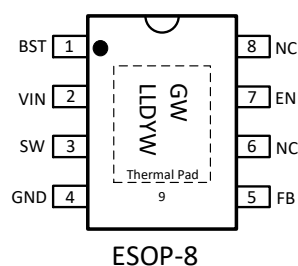
- Wide input voltage range: 4.2V to 28V
- 3A output current
- 0.8V reference voltage
- Low $R_{DS(ON)}$ integrated power MOSFET (150/90m Ω)
- 3 μ A(Max) shutdown current
- Integrated internal compensation
- High efficiency at light load
- Internal 1ms soft-start
- Cycle-by-cycle current limit
- Over-temperature protection with auto recovery
- Under-voltage lockout (UVLO)
- Hiccup short circuit protection
- Available in ESOP-8 package
- RoHS compliant

APPLICATIONS

- Distributed power system
- Flat panel television and monitors
- STB (Set-top-box)
- Networking, XDSL modem

PIN OUT & MARKING

GW: Product Code
LL: Lot No.
D: Fab code
YW: Date code



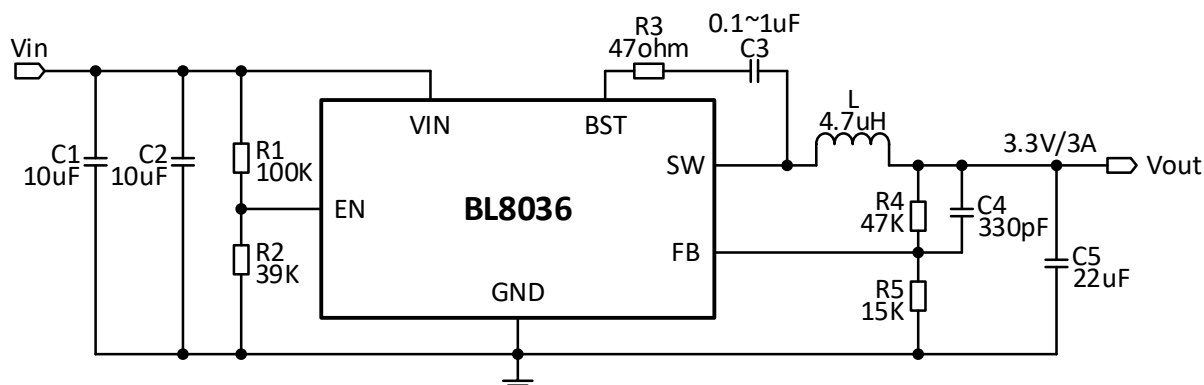
Note:

- 1) The thermal pad must be connected to GND Pin.
- 2) The Thermal Pad is GND Pin. It must be electrically connected to the exposed pad on the printed circuit board for proper operation.

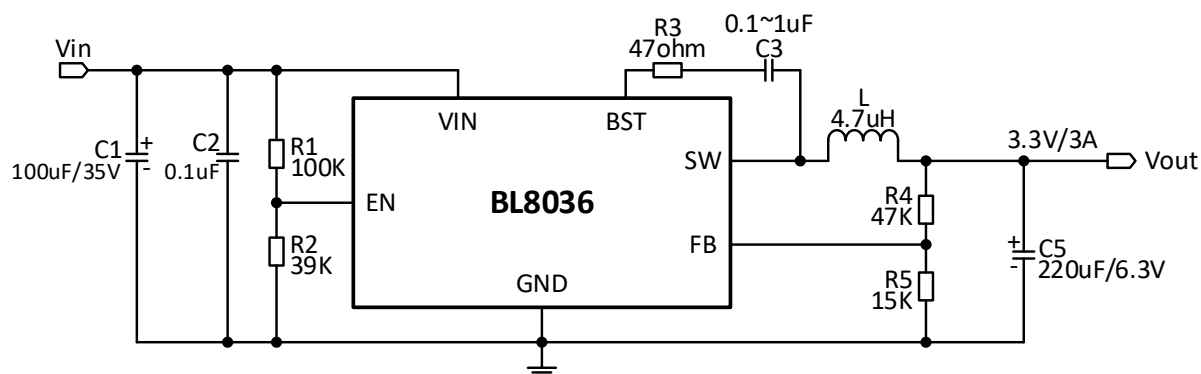
ORDERING INFORMATION

Part No.	BL8036CS8TR
Package	ESOP-8
Tape&Reel	2500/Reel

TYPICAL APPLICATION



C_{IN} & C_{OUT} use ceramic capacitors application circuit



C_{IN} & C_{OUT} use electrolytic capacitors application circuit

Note:

- 1) When Vin is greater than 12V, if EN is directly connected to VIN, the resistance R1 needs to be greater than 1MΩ.
- 2) If Vin<19V, R3 can be replaced by a 0ohm resistor.

Table 1. Recommended component values

V_{IN}=12V, the recommended BOM list is shown as below.

Vout	C1	C2	L	R3	R4	R5	C4	C5
5V	10uF/MLCC	10uF/MLCC	4.7uH-6.8uH	47ohm	68K	13K	100pF-330pF	22uF/MLCC
3.3V			2.2uH-4.7uH	47ohm	47K	15K	100pF-330pF	
2.8V			2.2uH-4.7uH	47ohm	30K	12K	100pF-330pF	
2.5V			2.2uH-4.7uH	47ohm	39K	18K	100pF-330pF	
1.8V			2.2uH-4.7uH	47ohm	15K	12K	100pF-330pF	
1.2V			2.2uH-3.3uH	47ohm	7.5K	15K	100pF-330pF	
5V	100uF/35V/ECL	0.1uF/MLCC	4.7uH-6.8uH	47ohm	68K	13K	-	220uF/6.3V/ECL
3.3V			2.2uH-4.7uH	47ohm	47K	15K	-	
2.8V			2.2uH-4.7uH	47ohm	30K	12K	-	
2.5V			2.2uH-4.7uH	47ohm	39K	18K	-	
1.8V			2.2uH-3.3uH	47ohm	15K	12K	-	
1.2V			2.2uH-3.3uH	47ohm	7.5K	15K	-	

ABSOLUTE MAXIMUM RATING

Parameter		Value
Supply voltage V _{IN}		-0.3V to 30V
Switch node voltage V _{SW}		-0.3V to (V _{IN} +0.5V)
Boost voltage V _{BST}		(V _{SW} -0.3V) to (V _{SW} +5V)
Enable voltage V _{EN}		-0.3V to 12V
Feedback input voltage V _{FB}		-0.3V to 6V
Package thermal resistance (θ _{JC})	ESOP-8	10°C/W
Package thermal resistance (θ _{JA})		50°C/W
Operating junction temperature (T _J)		-40°C to 150°C
Storage temperature range		-65°C to 150°C
Lead temperature (soldering, 10s)		260°C

Note: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

RECOMMENDED WORK CONDITIONS

Item	Min	Max	Units
Supply voltage V_{IN}	4.2	28	V
Ambient temperature (T_A)	-40	85	°C
Operating junction temperature (T_J)	-40	125	°C

ELECTRICAL CHARACTERISTICS

($V_{IN}=12V$, $T_A=25^\circ C$, unless otherwise stated.)

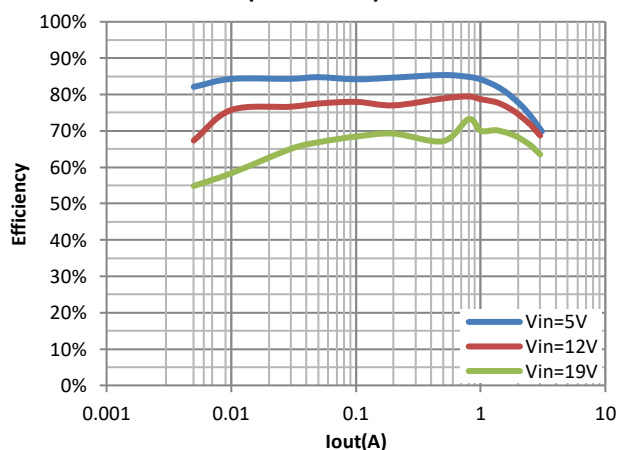
Parameter	Conditions	Min	Typ	Max	Units
Input voltage range		4.2		28	V
UVLO threshold	V_{IN} rising		3.8		V
UVLO hysteresis	V_{IN} falling		200		mV
Supply current in operation	$V_{EN}=5V$, $V_{FB}=1V$		150	200	uA
Supply current in shutdown	$V_{EN}=0V$		1		uA
Regulated feedback voltage	$3.8V \leq V_{IN} \leq 28V$	0.784	0.8	0.816	V
High-side switch on resistance	$V_{BST-SW}=5V$		150		mΩ
Low-side switch on resistance	$V_{IN}=5V$		90		mΩ
High-side switch leakage current	$V_{IN}=30V$, $V_{EN}=5V$, $V_{SW}=0V$, $V_{FB}=1V$		0.1	10	uA
Upper switch current limit	$V_{OUT}=5.0V$, V_{OUT} shorted to GND		5		A
Oscillation frequency		300	500	700	KHz
Maximum duty cycle			93		%
Minimum on time			100		ns
Soft start time			1		ms
EN input voltage "H"		1.5			V
EN input voltage "L"				0.6	V
Thermal shutdown			150		°C

PIN DESCRIPTION

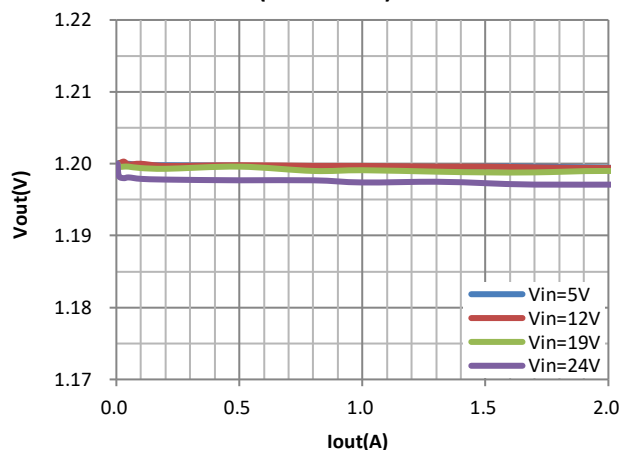
Pin #	Name	Description
1	BST	High side power transistor gate drive boost input.
2	VIN	Power input. Bypass with a 20uF ceramic capacitor to GND.
3	SW	Power switching node to connect inductor.
4	GND	Ground.
5	FB	Feedback input with reference voltage set to 0.8V.
6	NC	No connection.
7	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
8	NC	No connection.
9	Thermal PAD	The Thermal Pad is GND Pin which must be electrically connected to the exposed pad on the printed circuit board and connect to the foot of GND for proper operation.

ELECTRICAL PERFORMANCE

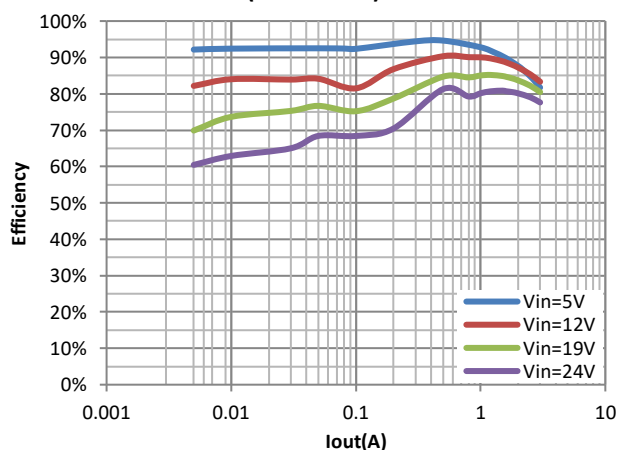
Efficiency
(Vout=1.2V)



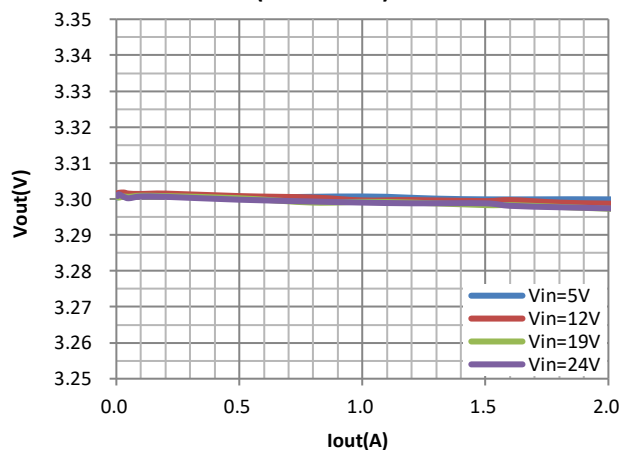
Load Regulation
(Vout=1.2V)



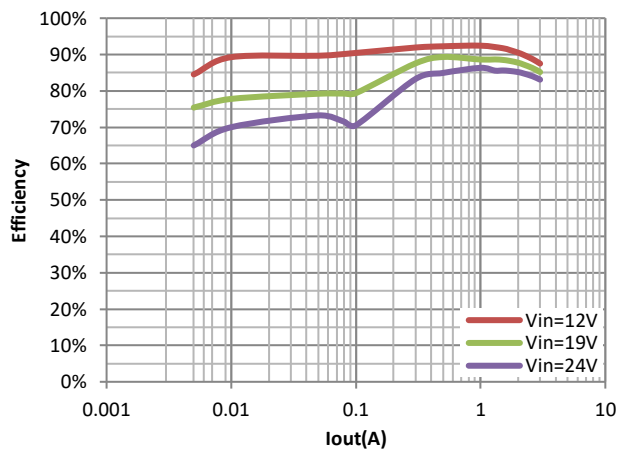
Efficiency
(Vout=3.3V)



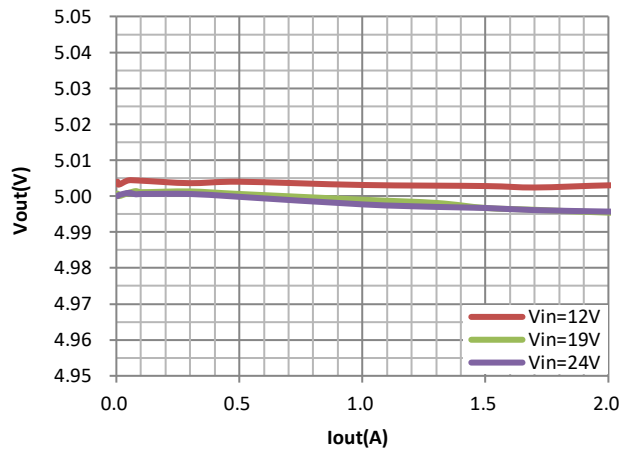
Load Regulation
(Vout=3.3V)



Efficiency (Vout=5.0V)

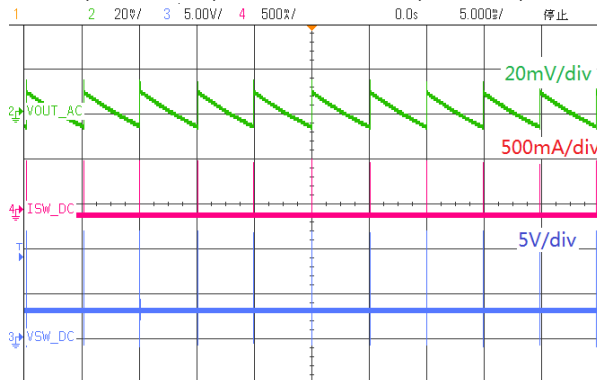


Load Regulation (Vout=5.0V)



Steady State Waveform

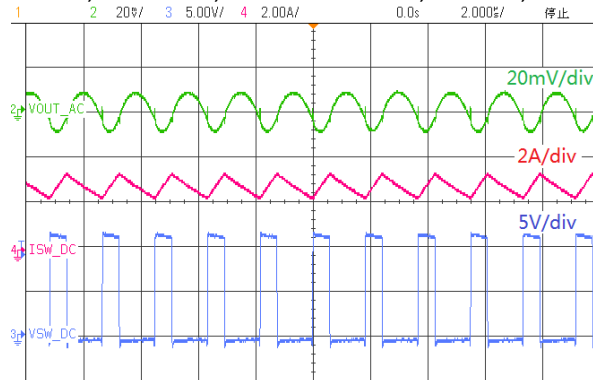
Vin=12V, Vout=3.3V, Cin=Cout=10uF*2, L=4.7uH, Iout=0A



Ch2—Vout, Ch3—Vsw, Ch4—Isw

Steady State Waveform

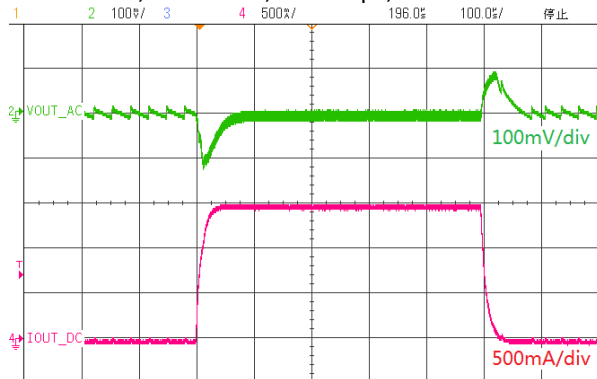
Vin=12V, Vout=3.3V, Cin=Cout=10uF*2, L=4.7uH, Iout=3A



Ch2—Vout, Ch3—Vsw, Ch4—Isw

Load Transient

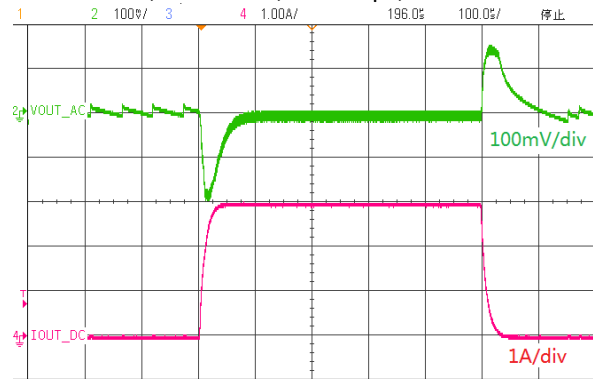
Vin=12V, Vout=3.3V, C4=330pF, Iout=0.01~1.5A



Ch2—Vout, Ch4—Iout

Load Transient

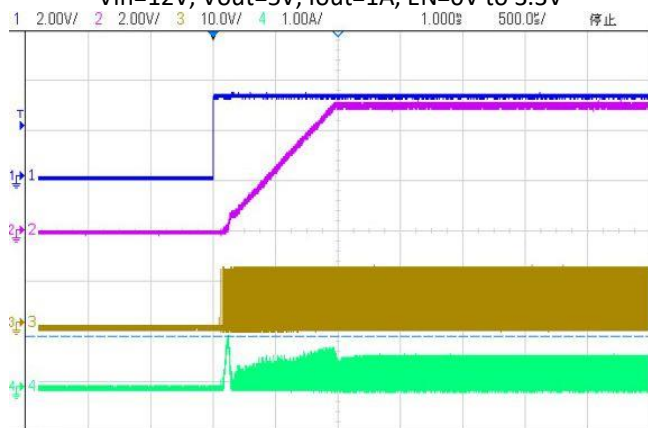
Vin=12V, Vout=3.3V, C4=330pF, Iout=0.01~3A



Ch2—Vout, Ch4—Iout

EN Power On

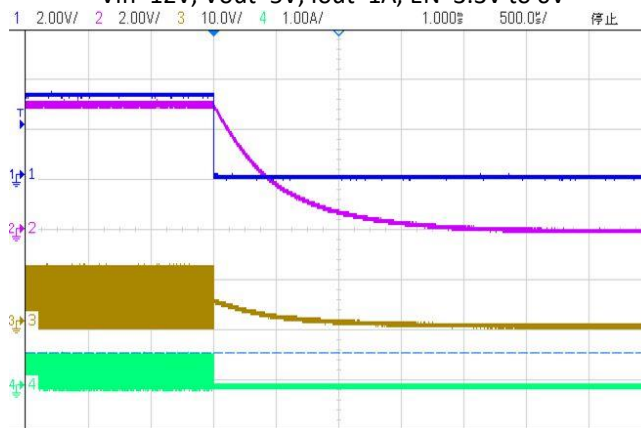
Vin=12V, Vout=5V, Iout=1A, EN=0V to 3.3V



Ch1—EN, Ch2—Vout, Ch3—Vsw, Ch4—I_L

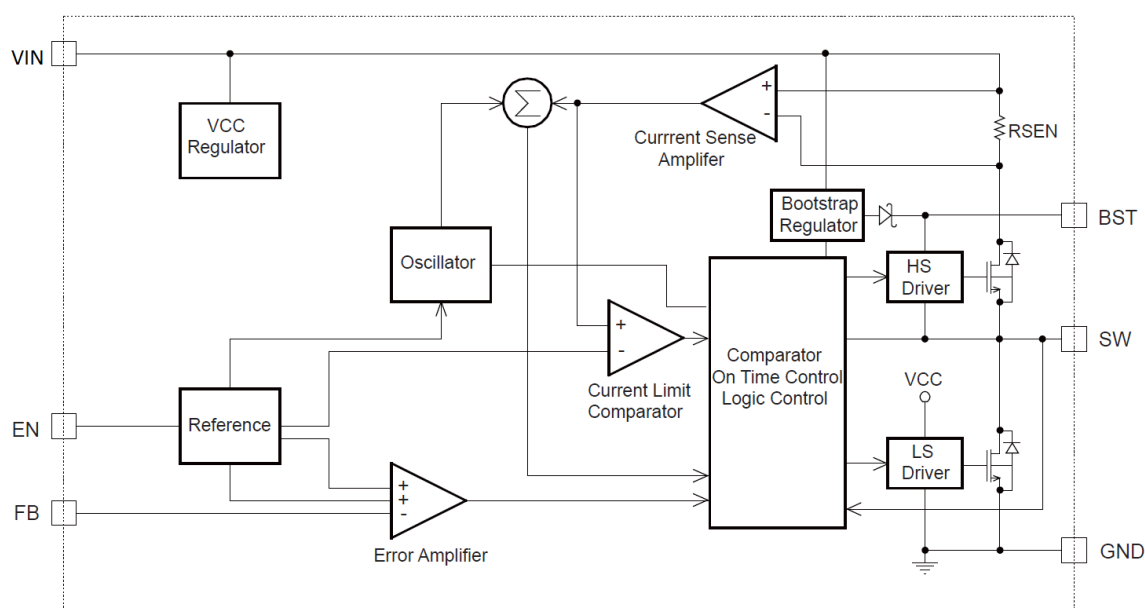
EN Power Off

Vin=12V, Vout=5V, Iout=1A, EN=3.3V to 0V



Ch1—EN, Ch2—Vout, Ch3—Vsw, Ch4—I_L

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

Loop operation

The BL8036 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current, integrated with a 150/90mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Internal soft-start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-current-protection and hiccup

The BL8036 has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 300mV) to trigger a UV event, the BL8036 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. This greatly reduces the

average short-circuit current to alleviate thermal issues and to protect the regulator. The BL8036 exits hiccup mode once the overcurrent condition is removed.

Light load operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite RDSOns of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. BL8036 employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power save mode during light load, thereby extending the range of high efficiency operation.

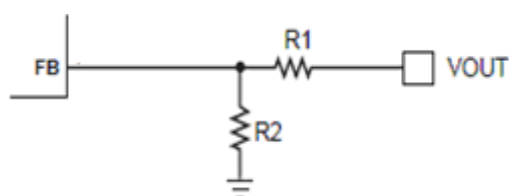
Startup and shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting output voltage

The external resistor divider is used to set the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$


Selecting the inductor

Use a 2.2μH-to-6.8μH inductor with a DC current rating of at least 25% higher than the maximum load current for most applications. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the output capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right] \times \left[R_{ESR} + \frac{1}{8 \times f_s \times C_2} \right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

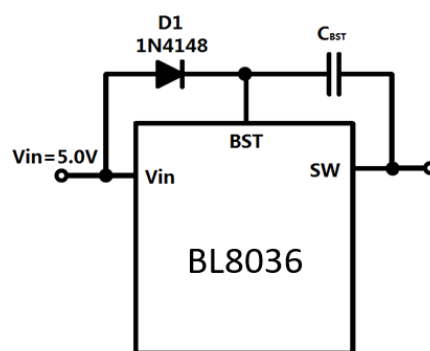
For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The BL8036 can be optimized for a wide range of capacitance and ESR values.

Selecting the external boost diode

It is recommended to add an external Boost Diode to improve efficiency and stability in these situations when the input voltage is fixed at 5.0V. Any a readily and cheap diode can meet the need of these application such as 1N4148.



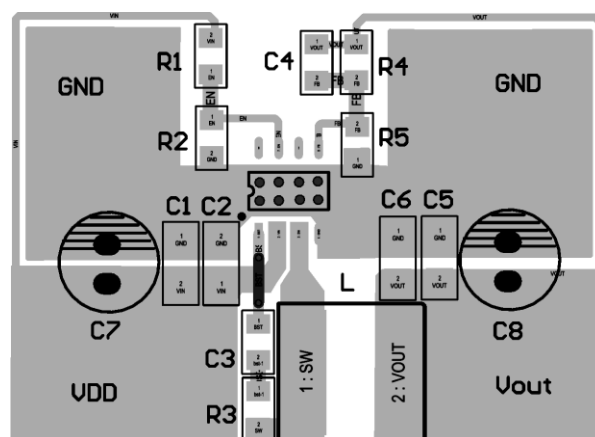
PCB LAYOUT RECOMMENDATION

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (SW).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the

PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.

5. Multi-layer PCB design is recommended.



PACKAGE OUTLINE

Package

ESOP-8

Devices per reel

2500pcs

Package dimension:

The image displays three technical drawings of an ESOP-8 package. The top view shows a rectangular package with pins on all four sides. Dimensions labeled include E (total width), E1 (width excluding pins), E2 (inner width), D1 (inner height), and b (pin thickness). The side view shows the package profile with dimensions D (total height), e (pin pitch), A1 (lead length), A2 (lead width), and A (total lead length). The cross-section view shows the package body with dimensions c (lead thickness), theta (lead angle), and L (package length).

字符	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.70	0.053	0.067
A1	0.00	0.120	0.00	0.005
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°